JUNE 24, 1981

A CAHNERS PUBLICATION

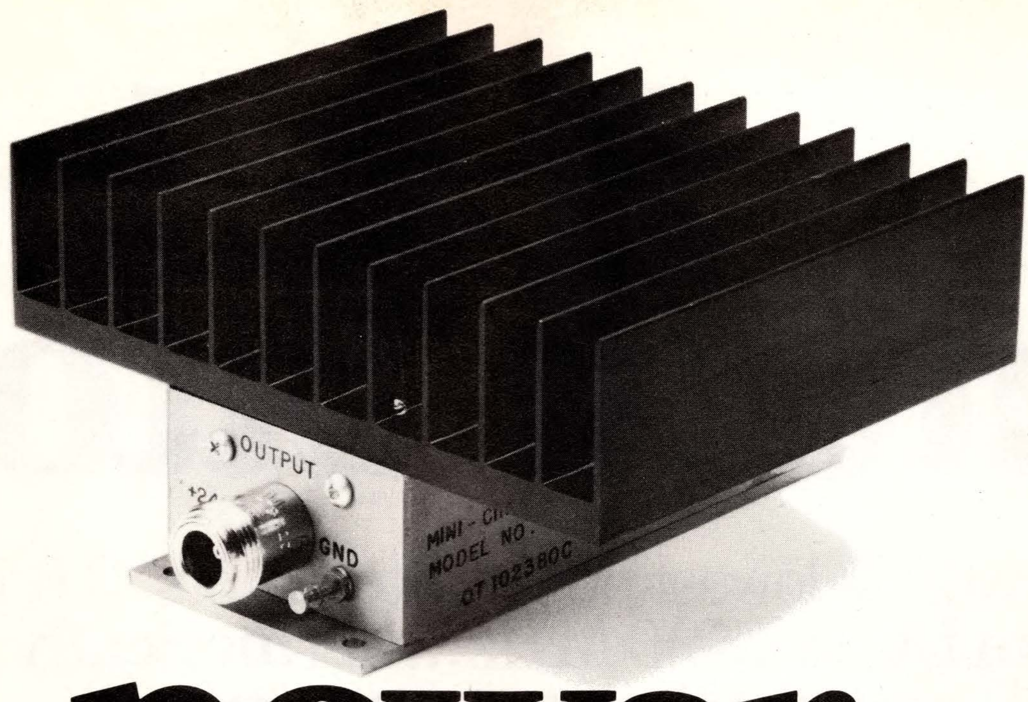
EDN

EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

Current-mirror ICs aid current handling

Understand the basics of a color-graphics processor

Amended patent law could affect innovation



power amplifiers

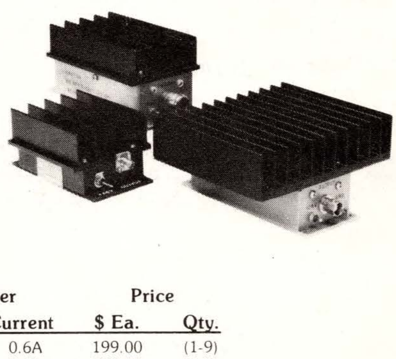
1 Watt and now... 2 Watts linear output from 50KHz to 1200 MHz from $199

If your application requires up to 2 watts for intermodulation testing of components... broadband isolation... flat gain over a wide bandwidth... or much higher output from your frequency synthesizer or signal/sweep generator... Mini-Circuits' ZHL power amplifiers will meet your needs, at surprisingly low prices. Seven models are available, offering a selection of bandwidth and gain.

Using an ultra-linear Class A design, the ZHL is unconditionally stable and can be connected to any load impedance without amplifier damage or oscillation. The ZHL is housed in a rugged 1/8 inch thick aluminum case, with a self-contained hefty heat sink.

Of course, our one-year guarantee applies to each amplifier.

So from the table below, select the ZHL model for your particular application ...we'll ship within one week!



* Model No.	Freq. MHz	Gain dB	Gain Flatness dB	Max. Power Output dBm 1-dB Compression	Noise Figure dB	Intercept Point 3rd Order dBm	DC Power Voltage	DC Power Current	Price $ Ea.	Price Qty.
ZHL-32A	0.05-130	25 Min.	±1.0 Max.	+29 Min.	10 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-3A	0.4-150	24 Min.	±1.0 Max.	+29.5 Min.	11 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 Min.	11 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
ZHL-2	10-1000	15 Min.	±1.0 Max.	+29 Min.	18 Typ.	+38 Typ.	+24V	0.6A	349.00	(1-9)
ZHL-2-8	10-1000	27 Min.	±1.0 Max.	+29 Min.	10 Typ.	+38 Typ.	+24V	0.65A	449.00	(1-9)
ZHL-2-12	10-1200	24 Min.	±1.0 Max.	+29 Min.*	10 Typ.	+38 Typ.	+24V	0.75A	524.00	(1-9)
ZHL-1-2W	5-500	29 Min.	±1.0 Max.	+33 Min.	12 Typ.	+44 Typ.	+24V	0.9A	495.00	(1-9)

Total safe input power +20 dBm, operating temperature 0° C to +60° C, storage temperature −55° C to +100° C, 50 ohm impedance, input and output VSWR 2.1 max.

+28.5 dBm from 1000-1200 MHZ

For detailed specs and curves, refer to 1980/81 MicroWaves Product Data Directory, Gold Book, or EEM.

* BNC connectors are supplied; however, SMA, TNC and Type N connectors are also available.

CIRCLE NO 2

Mini-Circuits
A Division of Scientific Components Corporation
World's largest manufacturer of Double Balanced Mixers
2625 East 14th Street, Brooklyn, New York 11235 (212)769-0200
Domestic and International Telex 125460 International Telex 620156

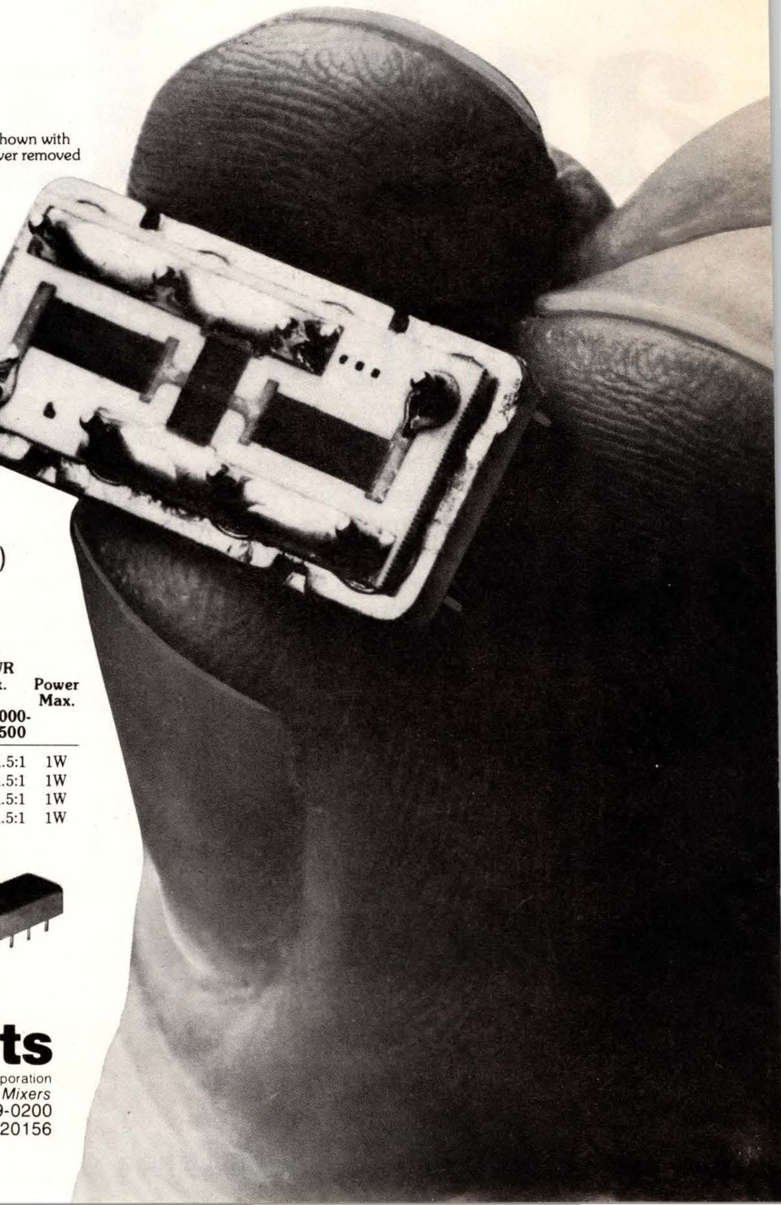
fixed attenuators

the world's lowest priced attenuators 3,6,10 or 20dB

from DC to 1500 MHz...hermetically sealed

The AT Series from Mini-Circuits **$1.95**

1000 Quantity
$3.95 (10-49)

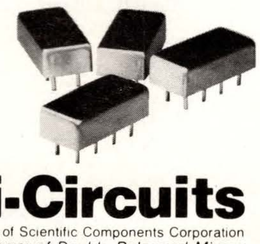


shown with
cover removed

Check these features:

- √ High stability; thick film construction in a hermetically sealed case
- √ Rugged construction: Meets requirements of MIL STD 202
- √ Miniature Size: 0.4" by 0.8" by 0.2" high
- √ Flat frequency response: Typically ±0.3 dB
- √ Excellent VSWR: typically less than 1.2:1
- √ Low cost: $1.95 (1,000 quantity), $3.95 (1-49)
- √ Delivery: From stock

Model	Attenuation, dB Nominal Value	Attenuation Tolerance from Nominal	Frequency Range MHz	Attenuation Change From Nominal Over Frequency Range, MHz		VSWR Max.		Power Max.
				DC-1000	1000-1500	DC-1000	1000-1500	
AT-3	3	±0.2dB	DC-1500	0.6dB	1.0dB	1.3:1	1.5:1	1W
AT-6	6	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-10	10	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-20	20	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W



Mini-Circuits

A Division of Scientific Components Corporation

World's largest manufacturer of Double Balanced Mixers

2625 East 14th Street, Brooklyn, New York 11235 (212)769-0200

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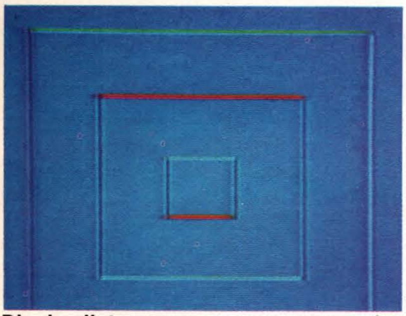
CIRCLE NO 3

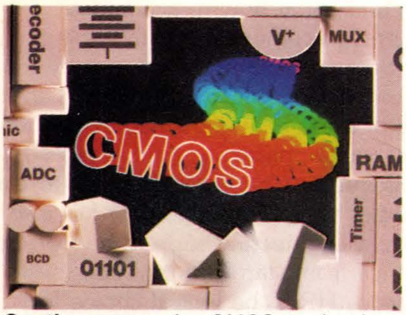
EDN

JUNE 24, 1981 • VOLUME 26, NUMBER 13 • EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

4-color graphics printers *use tiny pens to draw images (pg 82).*



Display-list processor *generates color graphics (pg 139).*



On the cover: *As CMOS technology explodes into a host of new applications, EDN documents the developments. Turn to pg 88. (Photo by Mike DeCastro, courtesy Intersil Inc)*

CP ∇BPA ☆ABP

DESIGN FEATURES

TECHNOLOGY UPDATE

NEW PRODUCTS

DEPARTMENTS

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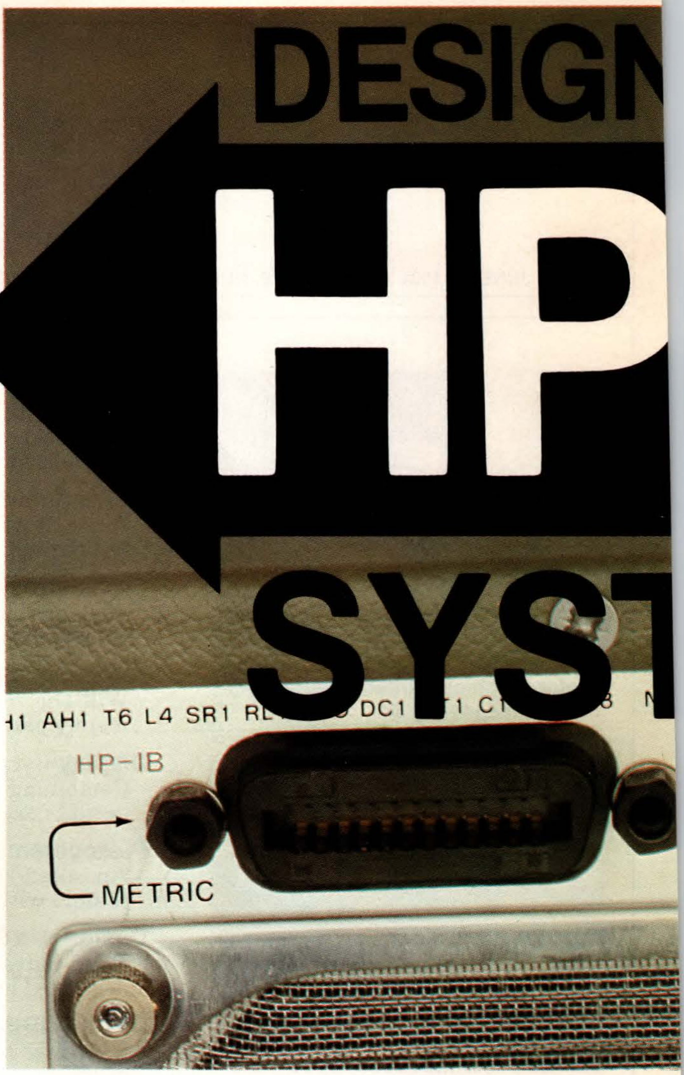
This symbol means faster measurement system development. . .



The familiar HP-IB (Hewlett-Packard Interface Bus) symbol is HP's way of identifying instruments and computers that conform to the IEEE-488 standard. But it means much more than just bus architecture and system compatibility. The HP-IB symbol also stands for the documentation and support that helps you get a measurement system operational in weeks instead of months.

Five reasons why you'll save time and effort.

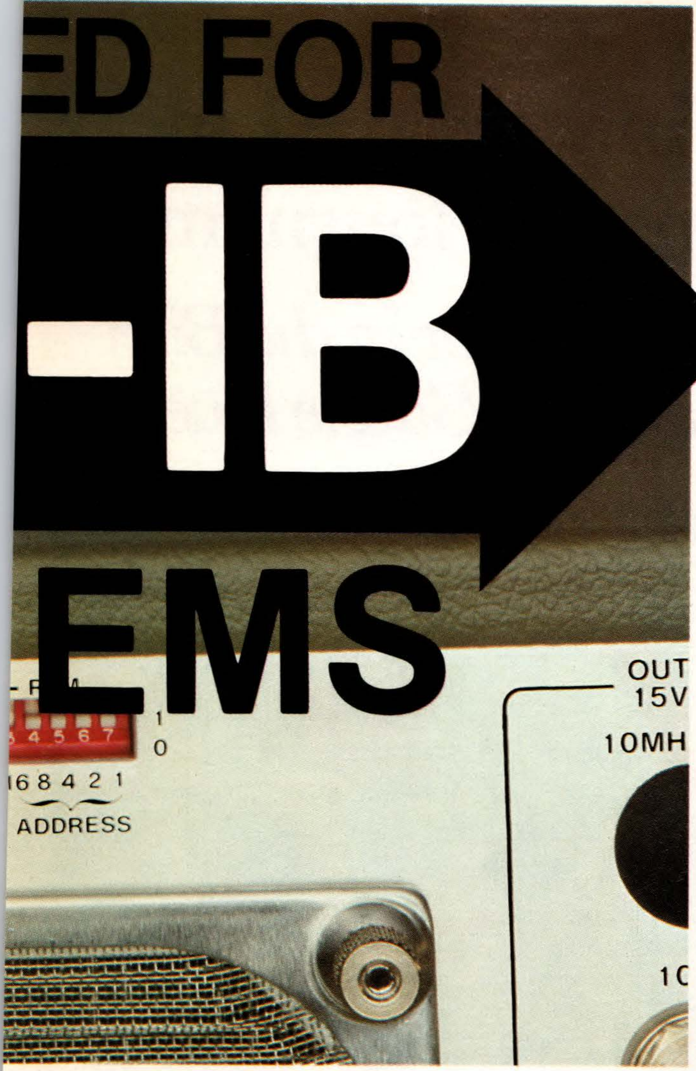
Choose HP when you need a measurement system and you get these advantages: 1) All devices and all documentation come from a single source which means consistency in design and documentation. 2) Every member of the HP-IB family of instruments and computers — over 140 in all — is designed for and tested to rigid HP-IB standards of compatibility. 3) Just as important, every HP-IB device comes with complete and comprehensive documentation that's easy to follow and consistent in its approach to implementation. You'll receive service manuals and operating manuals that typically include a guide to the implementation of computer based systems. 4) You can choose from more than 100 HP application notes. Many of these will teach you how to accomplish specific measurements in conjunction with the controlling computer. Software examples are included in a number of these to help you get to a solution even faster. In fact, one of these examples may be just what you need for your exact application. And many HP application notes list the results of performance tests to help you verify proper system operation. 5) HP also offers training, system engineering support and on-site service . . . assistance from start to finish. But these aren't the only reasons HP is the logical choice for measurement system development.

Over ten years of experience to call on.

When you design and build a measurement system, you can have the confidence of working with the company that was there when the need for a standard was realized. HP invented the 3-wire handshake technique and ever since then we've been designing and building HP-IB compatible components. By choosing an HP instrument or computer, you get the benefit of over 10 years experience in interface bus architecture, and how it can best be implemented.

Choose from a wide variety of computers.

With more than 140 different HP-IB instruments and computers to choose from, you can configure the measurement system that's just right for your application.



because it stands for system documentation and support on more than 140 HP-IB instruments and computers.

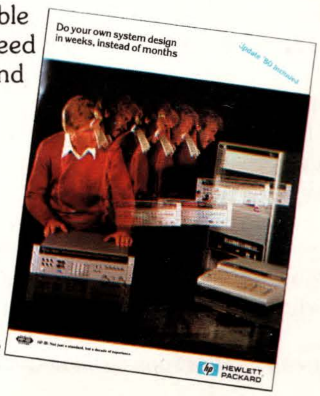
For your computing controller, you can choose from among the seven members of HP's powerful, flexible 1000 series family. Or you can select one of five friendly and flexible desktop computers. All HP computers have powerful, high-level languages that make it easy for you to write application programs.

Sticking with you.

HP offers all "Designed for Systems" devices with post-warranty support you can count on. You can continue this beyond the normal warranty period with an HP Maintenance Agreement. That means you'll enjoy yearly fixed cost, regularly scheduled preventive maintenance, priority response, and even more.

Meet the HP-IB family.

To find out how HP-IB compatible instruments and controllers can speed you to a faster system solution, send for our free brochure, "Do your own system design in weeks, instead of months." Just write: Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.



DESIGNED FOR HP-IB SYSTEMS

HP-IB: Not just a standard, but a decade of experience.

HEWLETT PACKARD

080/21

CIRCLE NO 4

Announcing the Winner of the Linear Wonderland Bifet Op Amp Tournament

PMI Declares Itself *the Winner in the Bifet Op Amp Dual Duel–and the Single Duel*

In Alice's Wonderland, the race was always over when someone declared himself the winner. In Linear Wonderland, PMI has been the big winner for a long time with its high-performance single bifet op amps, the OP-15, OP-16, and OP-17.

And now we declare a new winner in the growing dual bifet op amp duel—the OP-215, a dual precision JFET input op amp with proven BIFET performance advantages of high-speed and low input current in a variety of popular pinouts.

One of the "secret weapons" is our patented bias current cancellation (Patent #4,068,254), which assures low I_B at high temperatures as well as at 25°C, and already warmed up and operating the way you *use* them (instead of the way our competitors *test* them). Another is our thermally balanced chip layout, which results in a well-behaved TCV_{os} distribution centered at zero, with over 75% yield to 5μV/°C.

Bifet winners have a lot of other improvements over ordinary bifets. To increase speed we've improved biasing and frequency compensation. And to lower TCV_{os} at high temperatures, we balanced the second stage design and improved the first stage design to hold the gain constant over the temperature range.

And, of course, as with all PMI precision op amps, you get the on-chip zener zap trimming of V_{os}, the improved

BIFET CHAMPION SELECTION GUIDE
MIN/MAX SPECS—Best Grade

	OP17	OP16	OP15	OP215
Slew Rate (V/μs)	45	18	10	10
GBW Product (MHz)	20	6.0	4.0	3.5
Supply Current (mA)	7.0	7.0	4.0	8.5
CMRR and PSRR (dB)	86	86	86	86
Gain (V/mV)	100	100	100	150
Offset Voltage (mV)	0.5	0.5	0.5	1.0
TCV_{OS} (μV/°C)	5.0	5.0	5.0	10.0
*BIASED CURRENT WARMED UP AND OPERATING AT 125°C (nA)	11.0	11.0	9.0	18.0

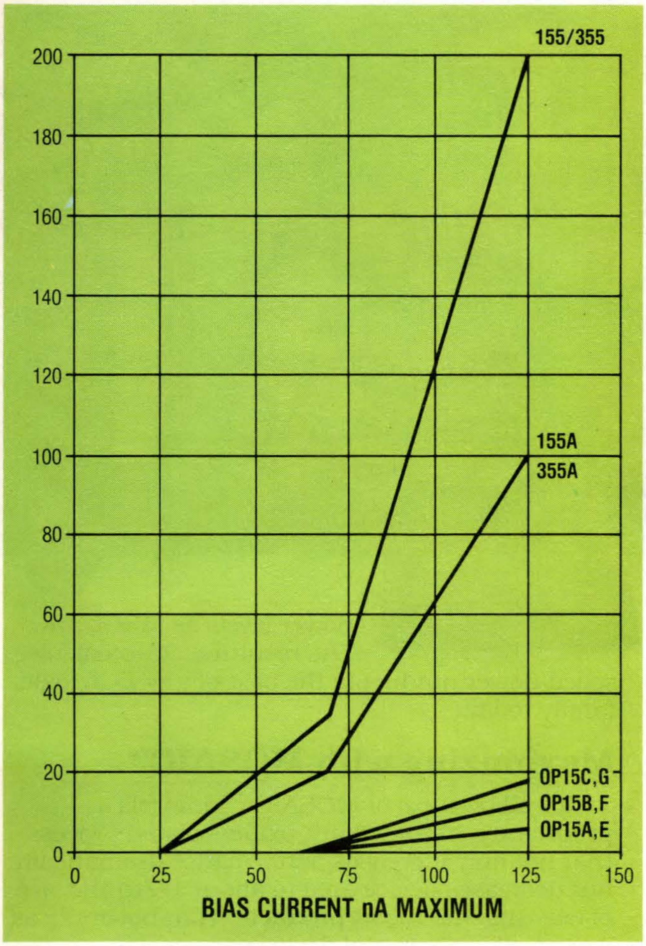
**The competition doesn't tell you that theirs are over 100 nA! They leave this discovery to the poor user.*

isolation and radiation hardening of our famous triple passivation, and the confidence that you got them from PMI, the unchallenged QUALITY LEADER in LICs.

YOU BE THE JUDGE

If you *don't* believe us (or even if you do), why not test our champion bifets yourself. We're truly proud of their noble performance in all competitive battles. Just fill out the coupon to get a sample of any of our bifet warriors. Be sure to test them at 70°C or 125°C, *fully warmed up* and operating the way your system will use them. Test any other available bifet op amp the same way. You'll see that there's really no contest.

If someone beat you to the coupon, write to us or circle **#250** for literature.



Precision Monolithics, Incorporated
1500 Space Park Drive
Santa Clara, California 95050
(408) 727-9222 TWX: 910-338-0218 Cable: MONO

In Europe contact:
Precision Monolithics, Incorporated
c/o BOURNS AG
ZUGERSTRASSE 74, 6340 Baar, Switzerland
Phone: 042/33 33 33 Telex 78722

OK, Alice. Send me a sample. All contests must have a judge. I have to see the results myself.

SAMPLE REQUESTED

☐ OP 15 (Fast, lowest power) ☐ OP 16 (Faster)
☐ OP 17 (Fastest; A_{VO} ≥5) ☐ OP 215 NEW DUAL

I'M ALSO CONSIDERING

Model ______________________

Mfgr ______________________

Application ______________________

____

Est. Need ____________ per year

Mail to: **Precision Monolithics, Inc.** 1525 Comstock Avenue, Santa Clara, CA 95050

or **Precision Monolithics, Inc.** c/o BOURNS AG Zugerstrasse 74, 6340 Baar, Switzerland

Name ______________________

Title ______________________

Company ______________________

Department ______________________

Address ______________________

____

Phone (________) ______________________

6 EDN5313

For 880-page Full-Line Product Catalog Circle no. 204

Technological leadership.

Motorola presents The first, fast logic family

Now Motorola, first to introduce high-speed logic and the industry's acknowledged ECL expert, announces MECL10KH — substantially boosting performance of your SSI/MSI functions — and making immediately available many of the circuits you'll need for upgrading those designs in standard, 16-pin packaging.

Speed X 2.

MECL10KH increases the speed of industry-standard MECL10K by a factor of 2. System clock rates increase as much as 40%, parasitic capacitance drops 50% and half the propagation delay, now just 1 ns, occurs at the same, 25 mW power levels as MECL10K.

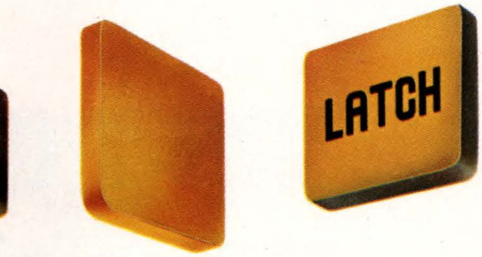
The resulting, 25 picojoule, speed-power product is the best of any ECL logic family today.

Maximizing with MOSAIC™.

It's all because of MOSAIC... Motorola's proprietary, high-density, oxide-isolated process that not only increases performance dramatically but decreases device area to about 1/7th the size of existing MECL10K products. That boosts f_T as well as all other initial device parameters.

Further, 10KH circuits are voltage-compensated and offer noise margins typically 20% better than

1 ns MECL10KH.
that's available fast, first.



MECL10KH INTRODUCTION LIST

Function	Part Number	Samples Available
Quad Or/Nor Gate	MC10H101	Now
Quad Nor Gate	MC10H102	Now
Quad And Gate	MC10H104	Now
Triple 2-3-2 Or/Nor Gate	MC10H105	Now
Triple Exclusive Or/Nor Gate	MC10H107	Now
Dual 4-5 Input Or/Nor Gate	MC10H109	Now
Triple Line Receiver	MC10H116	Now
Dual 2-Wide Or-And/ Or-And Invert Gate	MC10H117	Now
Dual 2-Wide 3 Input Or-And	MC10H118	June 1981
4 Wide 4-3-3-3 Input Or-And	MC10H119	June 1981
4 Wide Or-And/ Or-And-Invert Gate	MC10H121	June 1981
Dual D Latch	MC10H130	Now
Dual D Flip-Flop	MC10H131	Now
Universal Binary Counter	MC10H136	2nd Half 1981

Function	Part Number	Samples Available
4 Bit Universal Shift Register	MC10H141	2nd Half 1981
16 × 4 Bit Register File	MC10H145	2nd Half 1981
12 Bit Parity Generator/Checker	MC10H160	2nd Half 1981
Binary to 1–8 Line Decoder (Low)	MC10H161	June 1981
Binary to 1–8 Line Decoder (High)	MC10H162	June 1981
8 Line Multiplexer	MC10H164	June 1981
Quad 2 Input Mux W/Latch	MC10H173	June 1981
Dual 4 to 1 Multiplexer	MC10H174	June 1981
Quint Latch	MC10H175	June 1981
Hex D Flip Flop	MC10H176	June 1981
Look Ahead Carry Block	MC10H179	2nd Half 1981
Dual High-Speed Adder/Subtracter	MC10H180	2nd Half 1981
4 Bit ALU	MC10H181	2nd Half 1981
Dual 3-Input Or Gate	MC10H210	June 1981
Dual 3-Input Nor Gate	MC10H211	June 1981

10K devices. And, higher density functions that couldn't be manufactured economically in MECL10K technology are planned with MOSAIC... Motorola's own process.

10K-compatible.

The family is specified at the –5.2 V level for compatibility with MECL10K logic and memories and with the MC10800 bit-slice family, the MC10900 LSIs and the MECL MACROCELL™ array. Its 0° to 75° C range also matches constraints established by these products.

All MECL10KH specs have guaranteed minimums and maximums for extremes of both temperature and supply.

Additional products are imminent.

Fast delivery, low price.

You wouldn't expect a product like this to be slow — in any way. So we've made them immediately available from your distributor or factory in evaluation quantities. And at prices only about 30% above slower MECL10K...but 4 to 5 times lower than the less-available comparables.

Contact Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036...first to make MECL10KH available for your fast

Innovative systems
through silicon.

MOTOROLA INC.

TO: Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

Please send me information on MECL10KH.

95 EDN 6/24/81

Name ______________________

Title ______________ Tel.: (____) __________

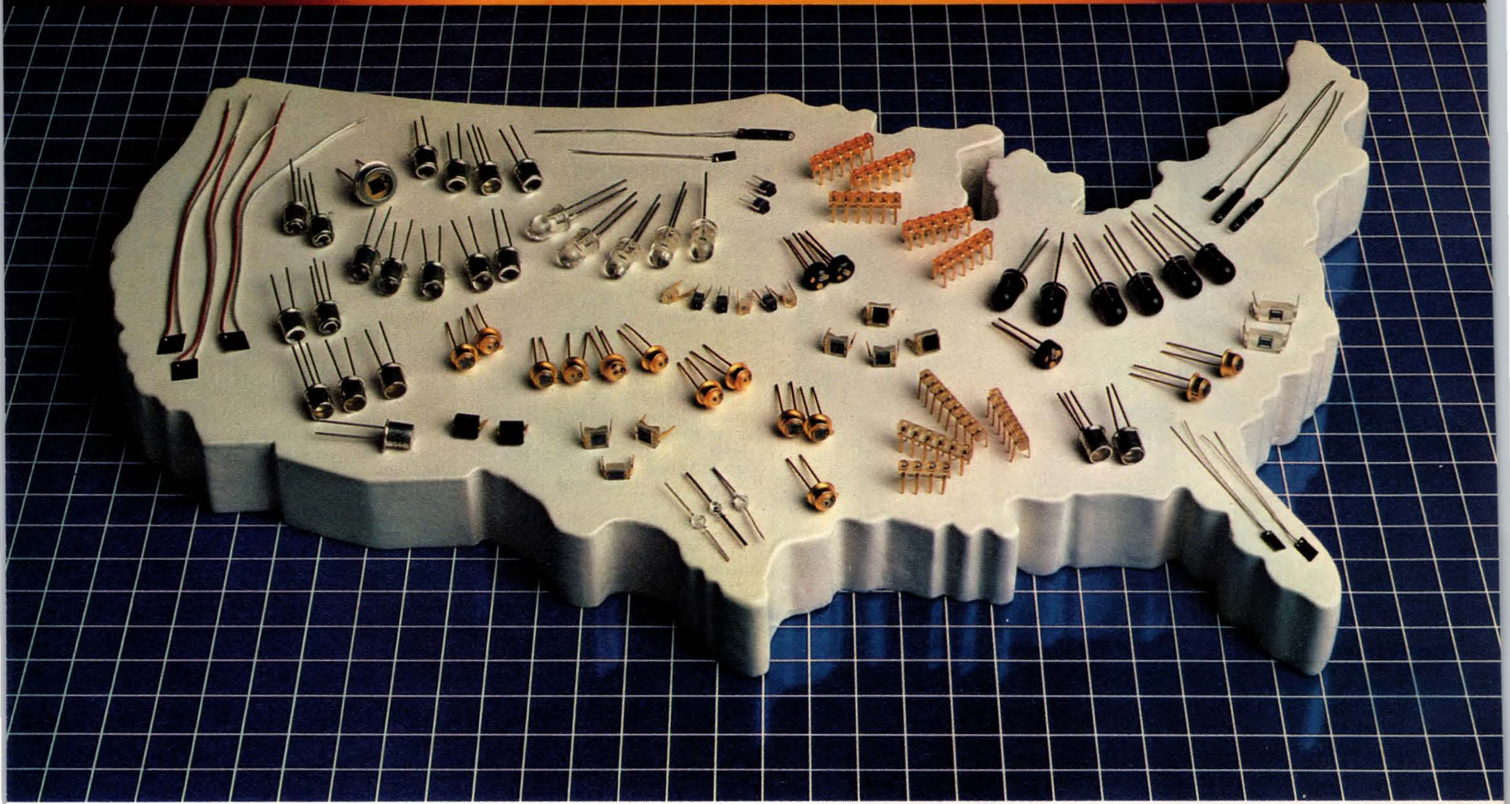
Company ______________________

Address/Mail Drop ______________________

City ______________________

State ______________ ZIP __________

Siemens infrared products now visible in the U.S.



Introducing the world's broadest infrared/photodetector product line

In Europe, Siemens IR/PD products are rated number one for quality and dependability.

So when we got the go-ahead to begin distributing the Siemens infrared/photodetector product line in the U.S., we were naturally excited.

Siemens makes over 200 different IR/PD products. These include: IR emitters, photodiodes, and phototransistors.

They range from high reliability, hermetically sealed products for military applications to low cost products in plastic packages for commercial uses.

Siemens offers many different sizes and shapes. Single packages to 10-unit arrays. Production volume is huge. Certain miniature types are produced in the millions of units per month.

The Siemens IR/PD product line is now available through the extensive Litronix distributor network in whatever supply you require...and at highly competitive prices.

So welcome, Siemens. We are pleased to assist you in becoming the most visible "non-visible" product line in America.

IR/PD Product Selector Guide available from Litronix, 19000 Homestead Road, Cupertino, CA 95014. (408) 257-7910, or the following distributors.

U.S. Distributors: Advent, Almac-Stroum, Arrow, Component Specialties, Gerber, Hamilton Avnet, Harvey, Kirkman, Lionex, Marshall, Moltronics, Pioneer-Standard, Summit and Zeus.

litronix A Siemens Company

CIRCLE NO 5

News Breaks

Edited by Joan Morrow

MULTILINGUAL DESKTOP μC EMPLOYS 68000 μP

The HP 9826A μC system from Hewlett-Packard Co (Palo Alto, CA) uses the Motorola 68000 μP operating at 8 MHz and supports HP-enhanced BASIC, HPL and PASCAL. In addition, the desktop unit is expandable to 512k bytes of user RAM. Other features include a 7-in. CRT display with graphics (400 × 300 resolution), an integrated 264k-byte, 5¼-in. floppy-disk drive and a full typewriter-style keyboard with numeric keypad and 10 programmable soft keys. Price and delivery dates have not yet been set.—CW

SOFTWARE PACKAGES EASE ATE-PROGRAM WRITING

Two software packages for device test systems make it easier for you to write and debug programs for complex parts.

One, from Megatest Corp, allows you to disassemble the ONEs and ZEROs you feed to a unit under test into high-level statements. Part of the operating system for the Santa Clara, CA company's Q2 testers, the package allows you to change the test program, run the test and save the original test and the edited version. Another part of the package, which is available as an upgrade to current Q2-tester users, lets you strip the μP part of the test program out of μC programs with on-board ROM. As a result, you don't need completely different tests for each ROM pattern, saving time when designing a new product or making a change in an old one.

The second package, from Fairchild Test Systems Group, is scheduled for delivery in September. The SAGE real-time test-program debugging tool will work with the San Jose, CA firm's Series 20 and Sentry LSI/VLSI testers. It will combine interactive software with a color graphics terminal to let you see how your test program is set up. The $50,000 SAGE will also simulate system operation, display both the stimulus and expected results and let you modify the program stimulus interactively.—AS

ADD SPEECH, DISK CONTROL AND UPPER-, LOWER-CASE CAPABILITY TO μC

Look for three Apple-oriented products from Vista Computer (Santa Ana, CA) next month. The first gives a voice to your Apple. Based on the National Semiconductor DT-1050 speech-processor chip, this Vista Vocalizer board is designed to plug into any open slot on the Apple backplane and use the μC's on-board speaker. It should cost less than $200 in OEM quantities.

In addition to the hardware voice box, expect a $595 8-in. double-sided, double-density disk controller for the Apple. Finally, the Vision-80 80-column upper- and lower-case board will add still more versatility to the micro. This $350 board will provide a threefold increase in display speed compared with similar units.—CW

4-PLATTER 5¼-IN. DRIVE WILL FEATURE 60M-BYTE CAPACITY

Aimed for first-quarter 1982 introduction, a 4-platter, high-capacity 5¼-in. Winchester from Rotating Memories (Sunnyvale, CA) will sport a 60M-byte capacity. The drive, an extension of the company's RMS-500 Series, will employ a voice-coil actuator, feature 700-tpi track density, use a dedicated servo surface and employ the RMS Data Express interface/encoding technique to obtain its high recording densities.—CW

COMPUTER MATCHES STD BUS TO IEEE-488

Based on an 8085A μP, the ZT7805 from Ziatech Corp (San Luis Obispo, CA) lets you combine the convenience of the STD Bus with the IEEE-488 I/O bus. The $650 board comes with 1k bytes of static RAM and as much as 8k bytes of EPROM/EEPROM. You also get an RS-232C port that supports communication at up to 56k baud.—ET

News Breaks

PERSONAL COMPUTER DESIGNED FOR MULTIPLE APPLICATIONS

Code-named "Worm" because it uses Apple Computer software and because it might affect Apple's market share, Xerox Corp's (Webster, NY) personal computer is expected to be introduced this month—2 months earlier than previous estimates.

The Worm is essentially an engine that through software can serve as a word processor, personal computer or small-business computer for accounts receivable. Based on a Z80 μP, it's expected to house 64k to 128k bytes of memory and include 8-in. floppy-disk drives.

Priced at $2500 to $5000, the Worm will be sold through Xerox retail stores. Software is CP/M based, and a program such as VisiCalc could run on the system.—JM

WINCHESTER-BACKUP FLOPPIES USE DISKETTE CARTRIDGES

Models 5850 and A506 Mini-Pac floppy drives from Amlyn (San Jose, CA) will keep your Winchester from forgetting valuable data. The floppies will employ a Mini-Pac cartridge that holds five minidiskettes, each with the same capacity as a double-density 8-in. unit. Diskettes get plucked from the Pac by a simple mechanism that places them gently on the spindle. The firm should sell the drives for less than $1000 in the fourth quarter.—CW

MORE HIGHLIGHTS FROM NCC '81

At NCC '81 last month, manufacturers not only introduced new products, but also displayed already introduced units that offer some new twists.

For example, the 10M-byte Alpha 10 storage subsystem employs a removable flexible-medium cartridge and achieves a 1.13M-bps data rate and a 35-msec average access time. Iomega Corp (Ogden, UT) designed the high-performance unit around a floating-medium concept; it also uses an embedded servo for track following. Alpha 10 costs $925 (1000); add another $37.50 (1000) for the cartridge.

Persci Inc (West Los Angeles, CA) put its $1650 Model 899 in the high-capacity-drive arena. When ready for fourth-quarter deliveries, this dual 8-in. disk drive will use a standard off-the-shelf medium, employ a track-following embedded servo and feature 150-tpi track density, giving it an unformatted capacity of 8.4M bytes.

Lear Siegler and Interstate Electronics, both based in Anaheim, CA, combined efforts to add speech recognition to Lear Sielger's ADM-3A and ADM-5 CRT terminals with the VRT200 speech board. The $2000 board recognizes as many as 100 words or short phrases with more than 99% accuracy. It fits easily into either terminal and combines an on-board editor with available host-resident software to provide immediate access to speech-recognition functions. The VRT200 should be available in August.

In printers, Qume Corp's less-than-$2100 Sprint 9/35 daisy-wheel unit prints at 35 cps and comes in RO and KSR versions. The single-board system is compatible with the San Jose, CA company's other Sprint printers.

Finally, Model MVP2 impact matrix line printer from Printronix Inc (Irvine, CA) is planned for fourth-quarter deliveries. Printing at 80 to 200 lpm, the 65-lb desktop unit will feature correspondence-quality printing fonts and plot density of 100 × 100 dots/in. in high-resolution mode. The unit's standard interface is Centronics and Dataproducts compatible; an RS-232C interface is optional. The Z80A-μP-controlled printer will cost less than $2000.—CW

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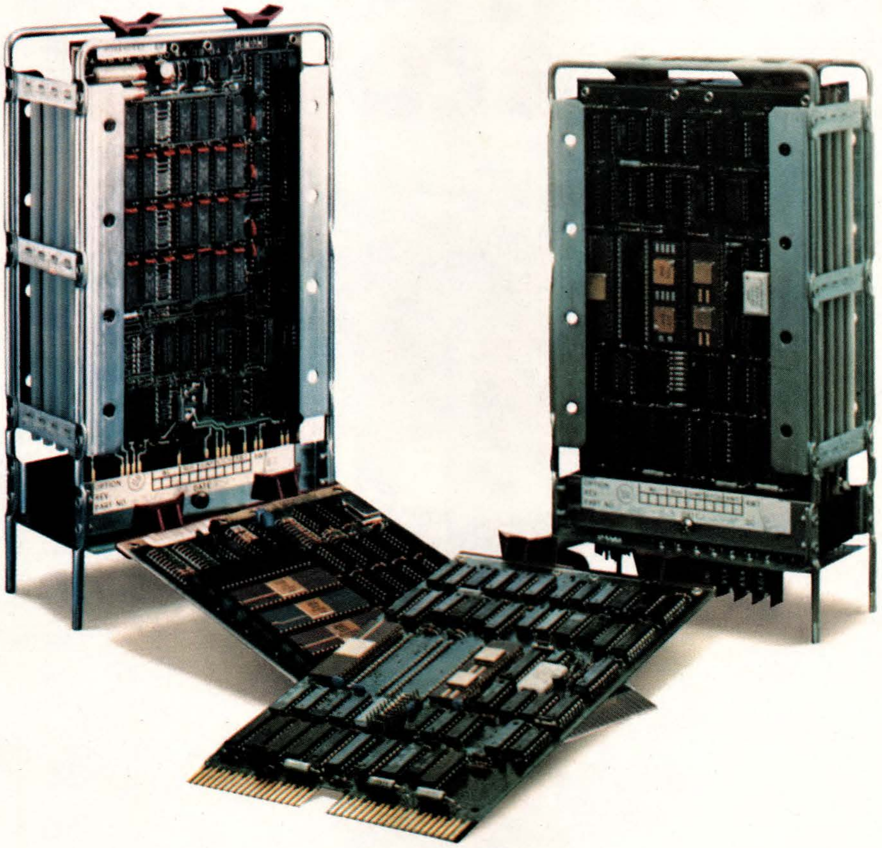
COMPONENT PRODUCTS



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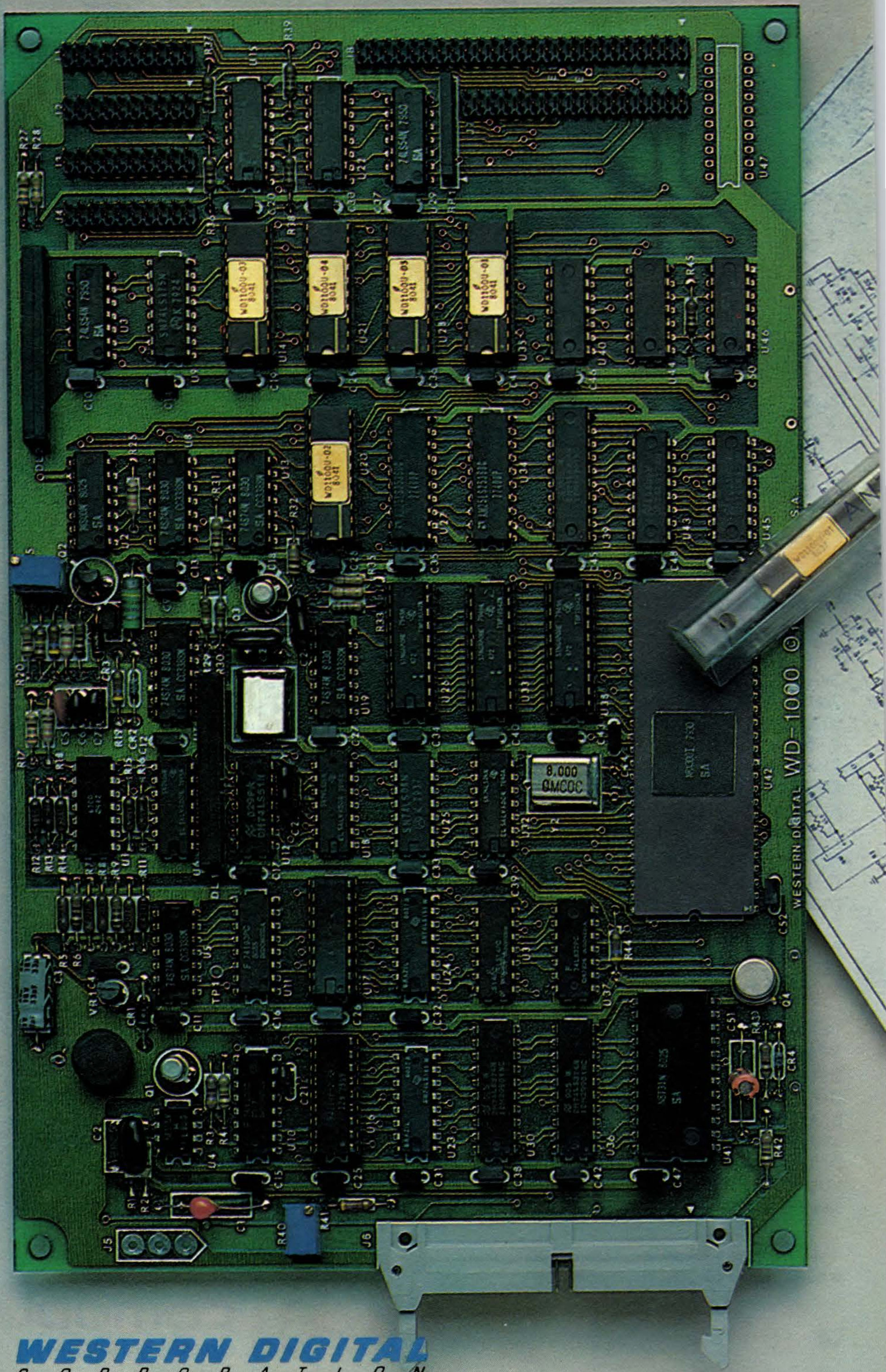
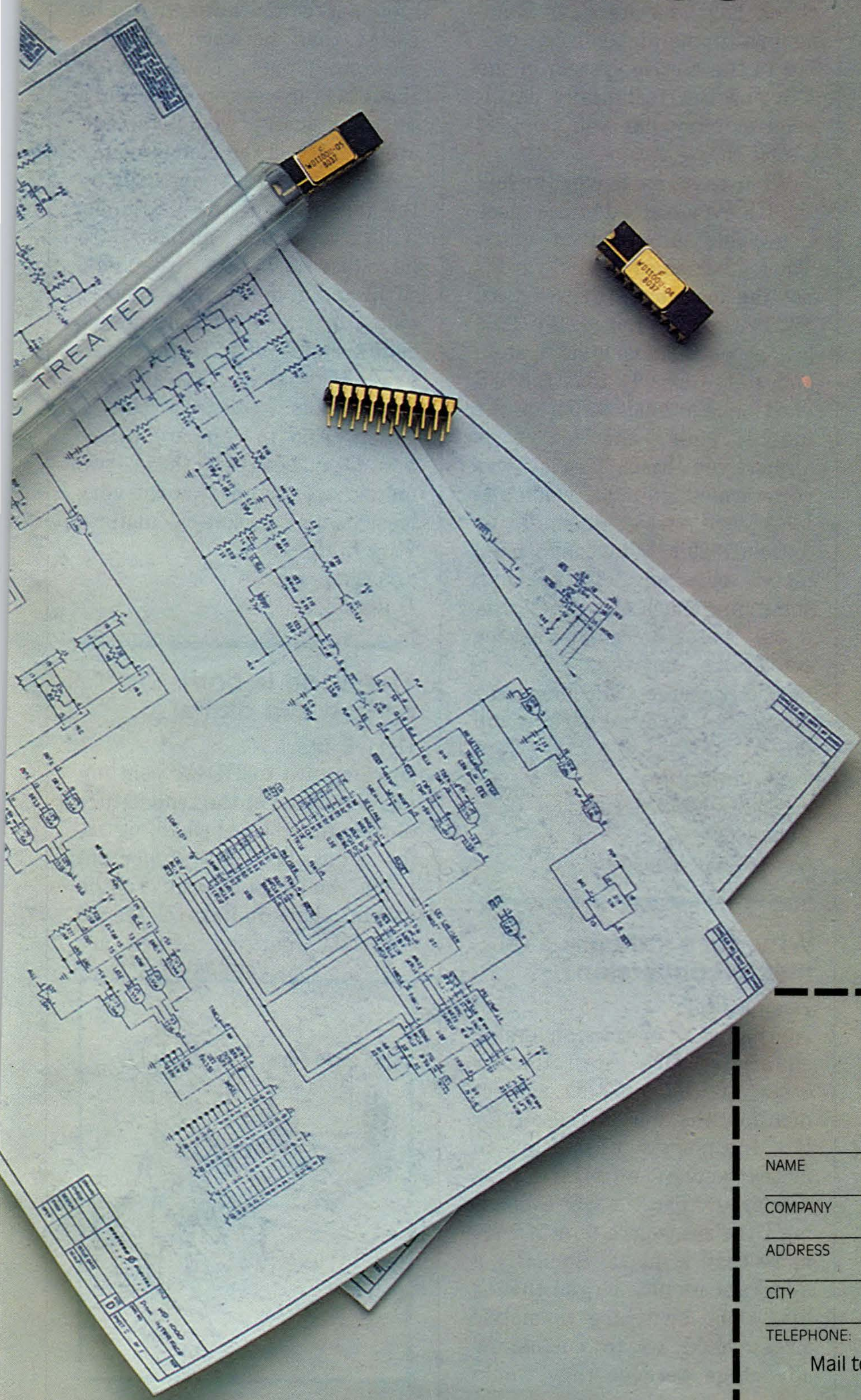


WESTERN DIGITAL WD-1000

OFF-THE-SHELF, THE $48* OEM DO-IT-YOURSELF WINCHESTER CONTROLLER.



Until now Winchester controllers had to be big, complex and very expensive.

SMALL WONDER. We've taken 75 discrete components from the usual Winchester controller and replaced them with 5 MSI chips (address mark detecter, CRC generator/checker, MFM generator, serial/parallel converter, parallel/serial converter) that can fit on a single board. And cost $48 per set.

Think what that means to you.

SMALL PACKAGE. An ST500/SA1000 interface for your system that's small, inexpensive, a lot less complicated and very reliable.

When you order the WD1100 5-chip set, we include complete instructions on how to design your controller board to make it work the way you want it too.

So not only will you save cold hard cash and months of development time, you'll be able to design a more compact, more reliable product. And get it into production while it's still new and exciting.

For more information, including specifications on the WD1100 chip set, call (714) 557-3550 or mail in our coupon today.

And it won't be long before you're in the chips.

Yes, I'm interested in saving money on my next Winchester controller.

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2445 McCabe Way
Irvine, CA 92714

Telephone: (714) 557-3550

CIRCLE NO 7

Signals & Noise

Impractical to delay metric conversion

Dear Editor:

European engineers should thank EDN for its clear stand against further delay in converting to the metric system in the US, the last technically developed country not yet using it (April 15, pg 43).

What beats me is why the hell the US ever started to use those impossible Anglo-Saxon units. The legal basis of the US yard is not the inaccurate British yard but instead the metre. An 1866 law accepts the metric system and states clearly that the US yard equals 3600/3937th of the metre; thus, the metre is already your basis. This law was reconfirmed in 1893, when the US yard was defined as 0.914401829m. Why convert the metric base for daily use into something much less practical?

As the US cannot escape conversion anyway, EDN is perfectly correct: The longer the US waits, the more harm it will do.

Yours sincerely,
Albert G Nymeyer
Centrelco
Geneva, Switzerland

Why does industry stall metric conversion?

Dear Editor:

Neither your metric-conversion editorial (EDN, April 15) nor other articles on this subject mention the major reason for US industry's objection to metric conversion: Metric sizes are larger than the corresponding US sizes—eg, a liter is 5.7% more than a quart. Similarly a kilogram is 10% larger than 2 lbs. Thus, switching to metric sizes would be to customers' advantage because they would be getting a larger package size, and a corresponding price increase wouldn't be popular.

Price comparisons between metric-sized units would also be easier than between odd English-sized ones. I am certain that if a liter were smaller than a quart, industry would immediately embrace the conversion.

We should all be impressed by the ingenuity of the US liquor industry, which managed to introduce 0.75-liter (the new fifth) and 1.75-liter (the new ½ gallon) bottles during its metric conversion. The 0.75 liter measures 1% less than a fifth and 1.75 liter equals 7.5% less than ½ gallon. And to compare prices per liter between these two metric sizes requires at the very least using a pocket calculator.

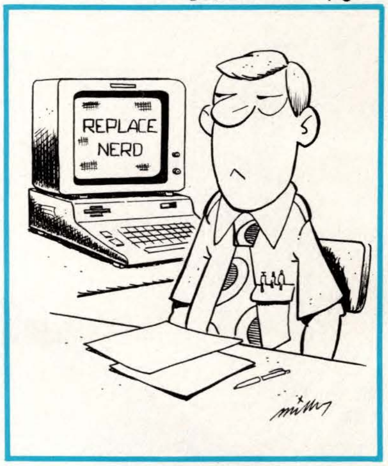
Very truly yours,
Cass R Lewart
Holmdel, NJ

The world is *both* analog and digital

Dear Editor:

In reference to EDN's continuing discussion of the true nature of the universe (April 15, pg 18, for example), one important point should be heard: To the extent that digital relates to particular entities, which are

Continued on pg 27

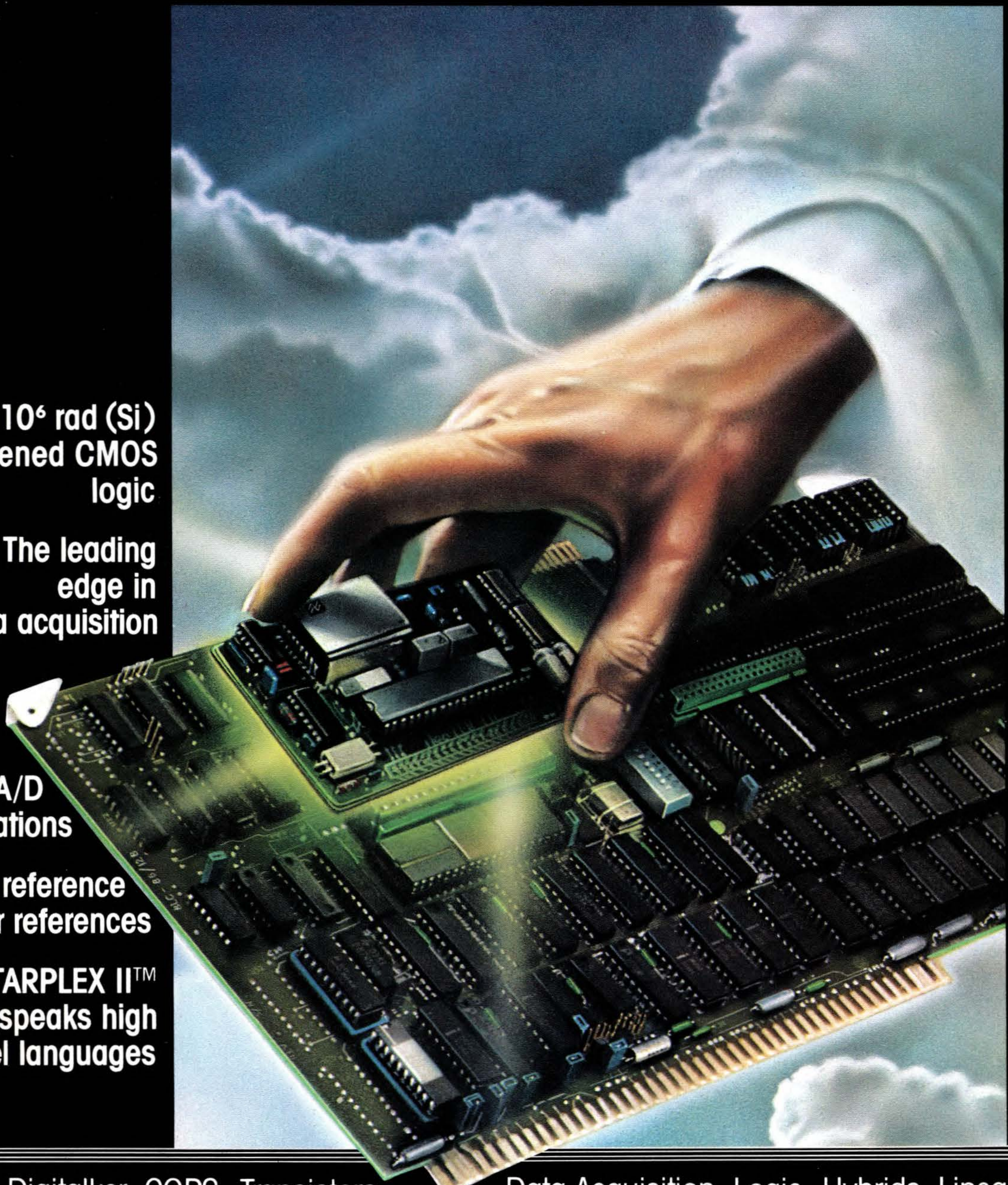


NATIONAL ANTHEM®

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY.

Cost-effective bubble memory arrives.

NATIONAL'S 1/4MBIT BLX-9252— THE SMALLEST BUBBLE MEMORY SUBSYSTEM EVER.



10^6 rad (Si) ardened CMOS logic

The leading edge in ata acquisition

bit A/D plications

he reference for references

STARPLEX II™ speaks high evel languages

COP400-PDS development system

New COP452 frequency generator and counter

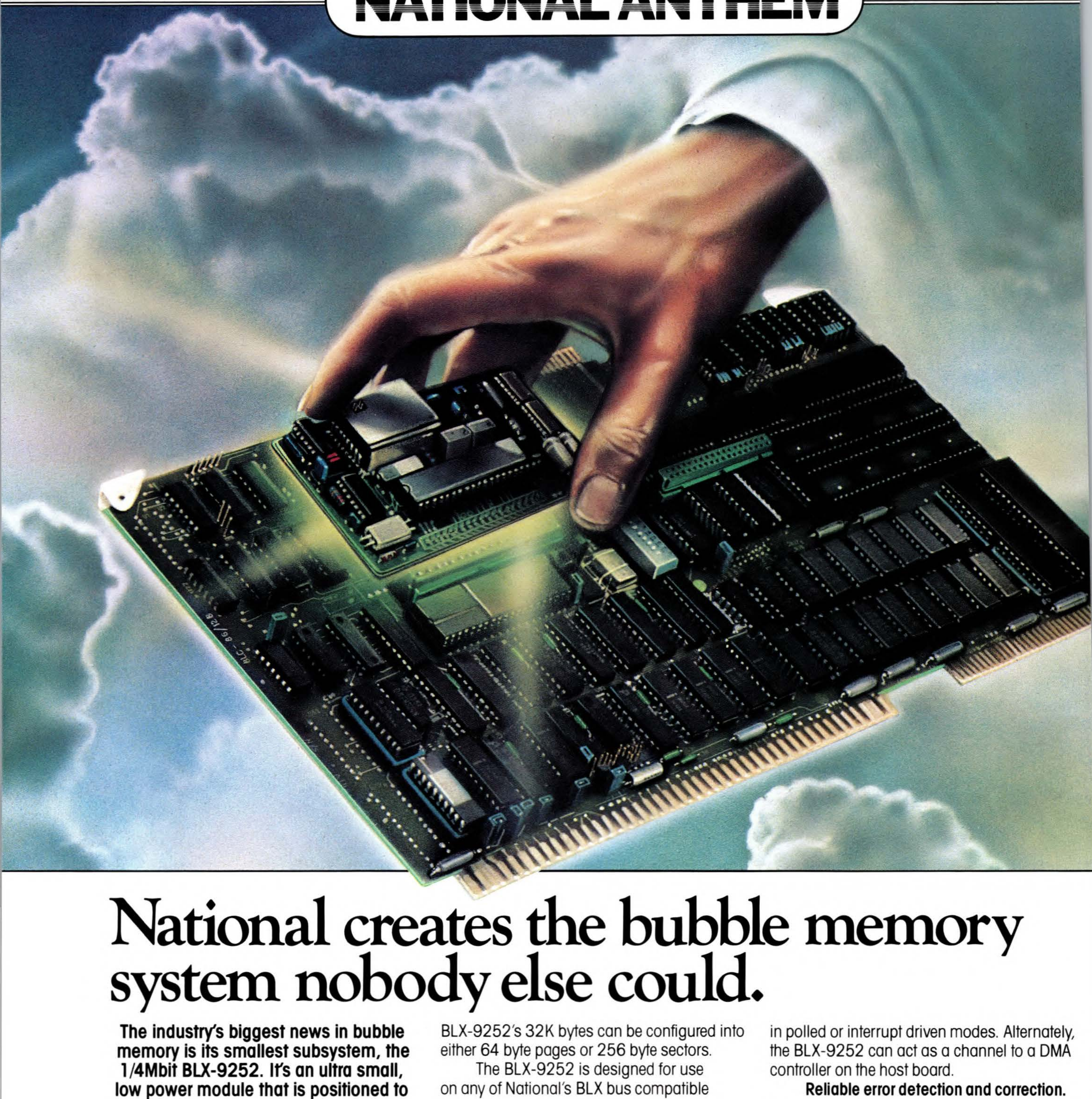
BLX modules expand board level versatility

New PCM filter for digital switching systems

Free literature— details inside

Digitalker COPS Transistors Data Acquisition Logic Hybrids Linear Interface Bubble Memory RAMS/ROMS/PROMs Transducer Displays Custom Circuits Optoelectronics Memory Boards Microprocessors Development Systems Microcomputers Modules Mil/Aero

NATIONAL ANTHEM



National creates the bubble memory system nobody else could.

The industry's biggest news in bubble memory is its smallest subsystem, the 1/4Mbit BLX-9252. It's an ultra small, low power module that is positioned to be the industry standard.

The BLX-9252 is a member of National's new line of BLX (board level expansion) modules.

As a low power (under 5 watts operating) expansion module, it plugs directly into any BLX bus compatible host board to add 32K bytes of non-volatile fast access storage capacity (under 7ms typical).

As a low cost (under $1000* in volume), ultra dense bubble memory subsystem, it's the new cost-effective standard for the industry.

1/4Mbit in eleven square inches. Built onto a 2.8" x 3.7" BLX module, the BLX-9252's 32K bytes can be configured into either 64 byte pages or 256 byte sectors.

The BLX-9252 is designed for use on any of National's BLX bus compatible boards, such as the BLC-86 12B, BLC-80 11A/12A/14A and BLC-80 116.

But for non-BLX bus compatible systems its signals are duplicated into a standard 50-pin PC card edge connector. This offers maximum on-board performance and frees the host's bus traffic for other resources.

The subsystem's subsystems. The BLX-9252 incorporates an NBM2256 bubble memory, timed and driven by the NBC82851 bubble memory controller.

The system software communicates with the BLX-9252 across the BLX interface with I/O read/write commands to the controller's eight user accessable registers.

Additionally, data transfer can take place in polled or interrupt driven modes. Alternately, the BLX-9252 can act as a channel to a DMA controller on the host board.

Reliable error detection and correction. Its data reliability is reinforced with a 12 bit Fire Code that will detect up to three random errors or an error burst up to 12 bits in length.

In turn, it will correct any error burst up to three bits in length.

The bottom line however, is that the BLX-9252 is the most dense and cost-effective bubble memory subsystem available today.

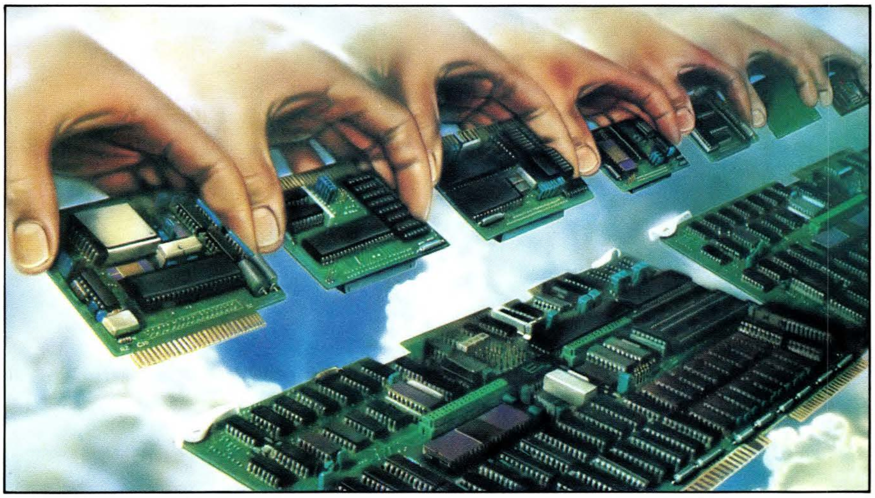
For data sheets and application notes on the BLX-9252, check box number 086 on the National Anthem coupon.

And start saving space, power and money on memories from National.

*U.S. prices only.

BLX modules create expanding board level versatility.

National puts the industry's broadest line of semiconductors on modules for Multibus™ board level expansion.



It's the BLX solution—National's low cost board level expansion for BLC users that the competition can't even begin to match. And it brings total versatility to SuperChips™ board system designs. Cost-and space-saving configurations are now just a matter of choosing which modules provide the best approach.

On-board expansion is accomplished by plugging any of National's BLX modules directly into sockets on their BLX-compatible host boards. Each of the BLC-80/11A, BLC-86/12B and BLC-80/116 host boards can accept any two expansion modules.

At present, modules are available to expand board level capabilities with speech synthesis, analog output, fixed or floating point math, parallel I/O, serial I/O, bubble memory and prototyping.

Soon, however, the growing BLX line will expand to cover National's entire line of semiconductors—the industry's broadest.

National's established manufacturing capabilities and technical innovation make them the logical choice for board level leadership from the chip up—with a full 12-month warranty.

For example, everyone has boards that compute and remember. There's no trick to that. But National has boards that translate (BLC-8488 Intelligent GPIB Controller), talk (BLX-281 Speech Synthesis Module) and measure (BLC-8737 & BLC-8715 Analog I/O Boards). The fact is, no one else can touch them in board technology.

Modules and SuperChips. Because man cannot live by chips alone.

For more information, just check box 088 on this Anthem's coupon.

SuperChip is a trademark of National Semiconductor Corporation.
Multibus is a trademark of Intel Corporation.

High performance PCM filter gets digital telecom systems off hold.

The TP3040 is pin and function interchangeable with the 2912 and 2912A with significant performance advantages.

National's new TP3040 PCM filter is a lot more than just a pin-for-pin, function-for-function replacement for the industry standard 2912.

The TP3040 surpasses both the 2912 and the 2912A filters with low power, noise, crosstalk and better low frequency rejection. So it brings new levels of cost-efficiency and performance to telecom applications.

Plus its unique monolithic design incorporates pre- and post-filtering in both the transmit and receive sides.

The TP3040 offers clear performance advantages over its pin-compatible counterparts, particularly in terms of power consumption. The TP3040 uses up to 85% less power than the competition.

This kind of performance is a direct result of NSC's innovative double-poly silicon gate P²CMOS technology. National brought together the most advanced fabrication techniques to perfect P²CMOS. It will allow them to create an entire line of problem-solving devices for the telecom marketplace.

The Practical Wizards are already turning TP3040s out in high volume. So now telecom design engineers can get their switching systems off hold with a truly superior 2912 and 2912A replacement filter from National Semiconductor.

For complete details on the TP3040, check box number 089 on this issue's National Archives coupon.

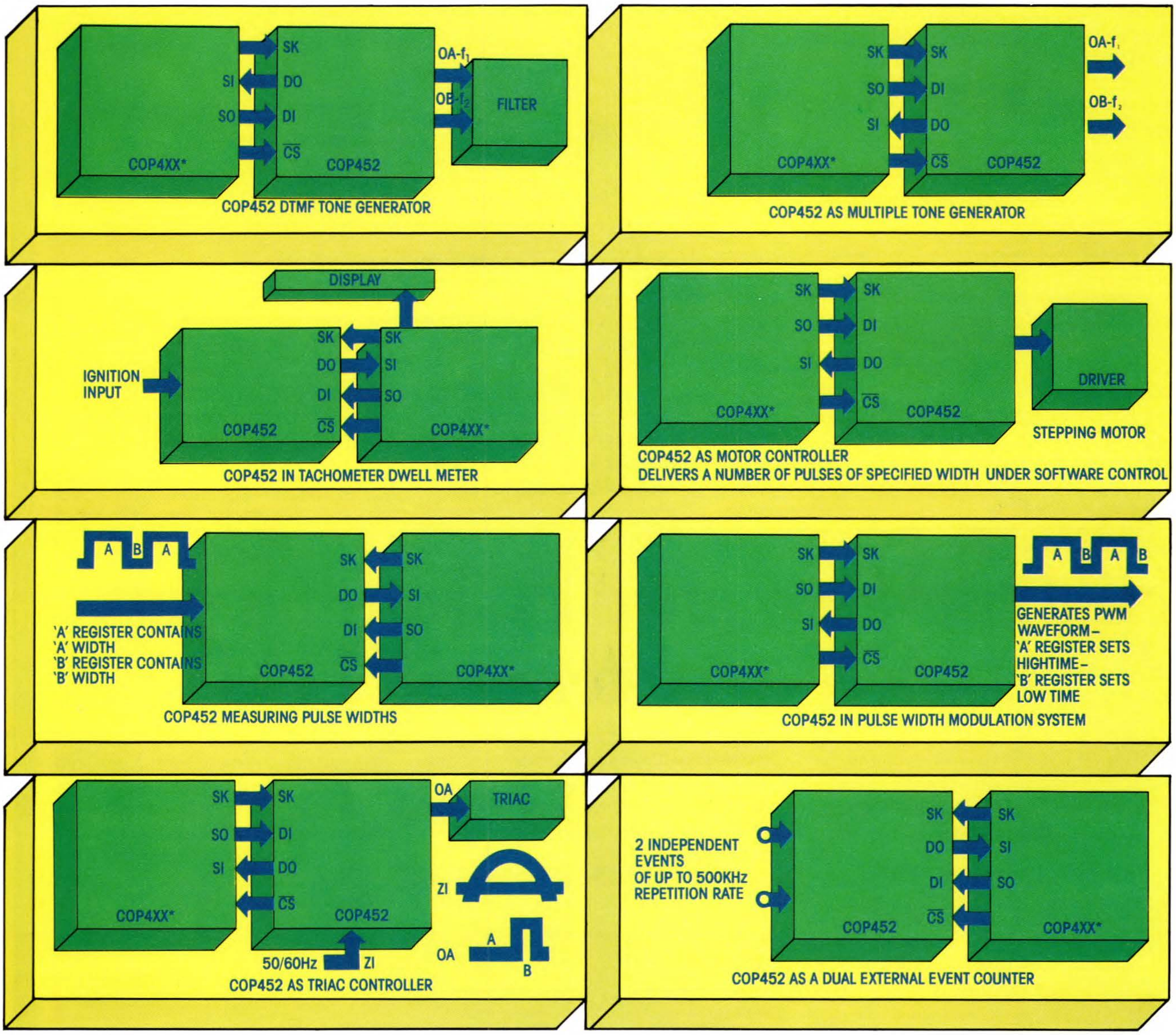
PCM FILTER COMPARISON TABLE

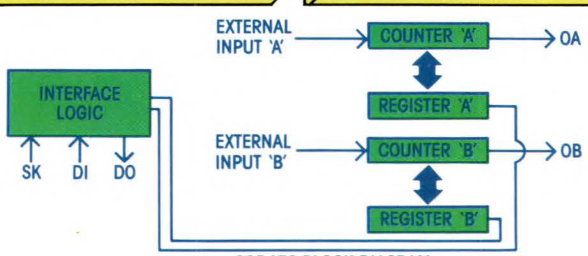
	2912		2912A		**TP3040**	
	Typ	Max	Typ	Max	**Typ**	**Max**
Power Consumption						
With power amps (mW)	280	440	80	N/A*	**46**	**64**
Without power amps (mW)	210	340	50	N/A*	**30**	**40**
Power down mode (mW)	55	90	0.4	N/A*	**0.5**	**1.0**
Idle Channel Noise						
Receive (dBrnCO)	9	12	3	N/A*	**2.5**	**5**
Transmit (dBrnCO)	10	13	9	N/A*	**2.5**	**6**
Crosstalk						
(dB; over 200-3400 Hz range)	N/A*	N/A*	N/A*	N/A*	**−80**	**−70**

*Data Unavailable

Eight more ways to use a COPS™ peripheral that a microcontroller can count on.

The COP452 time machine frees processors of most time-dependent tasks. With multiple tones, precise duty cycles, event counting, waveform measurement, "white noise" generation, and A/D–D/A conversions, it produces a wide variety of well-timed events.





COP452 BLOCK DIAGRAM

*Any COPS Microcontroller

For additional information on the COP452 check box 087 on this Anthem's coupon.

The low cost, easy-to-use development system for COPS™ microcontrollers.

It's the COP400-PDS, with a host of features for microcontroller software and hardware development.

The COP400-PDS product development system is the most cost-effective way to edit, assemble and debug hardware and software for COPS microcontrollers.

The COP (Controller Oriented Processor) family is National's complete line of single-chip microcontrollers. Each contains all the necessary system timing, internal logic, ROM, RAM and I/O to implement dedicated control functions in a variety of applications.

Disk storage eases the effort. The user interacts with the COP400 via a front panel keypad or an optional CRT and printer. Programs are edited and stored on the COP400's floppy disk.

Disk storage allows users to perform edit-assemble-test cycles much easier than on paper tape systems. And it's the most convenient means of providing National with the program data necessary for the mask-making process.

An important feature of the COP400-PDS is its debugging capability. It enables users to single step through a program, breakpoint to an address, trace program execution and dump out internal COP400 registers. The ability to execute these types of commands significantly reduces development time.

An emulator card attachment allows the execution of object code under the system's control. And an additional QUIKLOOK™ test module provides GO, NO GO inspection testing of incoming COPS devices.

This is, after all, National's way of providing an integrated concept support for their line of COPS microcontrollers.

For more information on the COP400-PDS and QUIKLOOK tester check box number 070 on the National Archives coupon.

COPS and QUIKLOOK are trademarks of the National Semiconductor Corporation.

STARPLEX II™ is fluent in PASCAL, PL/M, BASIC, FORTRAN and ordinary English.

National's highly interactive, easy to use development system now supports high level languages and speeds the overall development effort.

STARPLEX II is the perfect system for designers developing systems using high level languages. It incorporates full compilers for both PL/M and PASCAL with code generators for the 8080/8085 and NSC800/Z80.

BASIC and FORTRAN also come standard on STARPLEX II.

New features speed development. The new STARPLEX II has enhanced features designed in for high throughput and vast performance improvements. With its high level language support and 128K bytes of RAM, STARPLEX II offers an increase of performance up to three times that of STARPLEX.

The man/machine interface is greatly simplified by using menus to access desired software modules. Plus, a complete on-line library of the system's operating commands and procedures is maintained for instantaneous referencing. And it's all in plain, ordinary English.

STARPLEX II features two Z-80A processors in a master/slave configuration. Its operating system and user programs are segregated to offer system integrity not offered in any other development system.

Its slave processor has its own 64K bytes of RAM dedicated to user programs while the system incorporates 128K bytes of total RAM.

With its easy to use, time saving features, STARPLEX II becomes the logical choice for system developers of all of National's programmable devices, including processors, boards, PROMs, PALs and bubble memory.

STARPLEX II offers support for National's own BLMX real-time operating systems and the industry standard CP/M operating systems.

Also, a spooled printer capability allows a decrease in development time by allowing users to print out on-screen information, from file listing to compiler output.

User definable function keys (16 total) allow new versatility in both command mode and application runs on the system.

ISE™ has microprocessor emulation down cold. With ISE, engineers can now develop, test, analyze and debug prototype software/hardware for 8080, INS8048, INS8049, INS8050, INS8070 family μPs, Z-80, COPS™ microcontrollers, NSC800 and 8085 microprocessors plus National's Series/80 board level computers.

ISE's powerful debugging capability allows simultaneous software and hardware debugging of single or multiple processors for faster, more efficient system integration.

And since the symbol table is available during emulation, the same symbols are used in debugging that are used in writing the program being examined.

STARPLEX's symbolic debugging capability provides not only the usual breakpoint conditions, but also a "coast" command which allows you to continue executing a program after the breakpoint combination has been satisfied.

Also, with ISE's in-line assembler and disassembler, programmers can modify object code and display it in assembly language without having to leave the debug and emulation environment. And without editing and re-assembly of the entire source program, thus eliminating many tedious manual steps.

National's easy-to-learn ISE software comes completely integrated into the STARPLEX II system, including the unique Automatic Testing mode called "In File." In-File implements a predefined sequence of tests based on user-selected system and emulation commands. ISE can also record those results to show exactly how each part of the system performs during the tests.

STARPLEX II means a more powerful STARPLEX. Since STARPLEX II support packages are upward compatible with those of STARPLEX, it's a simple procedure to upgrade the original version.

For this purpose, National offers a special kit consisting of two master/slave CPU boards, the new keyboard with user definable keys, and the new STARPLEX II operating system.

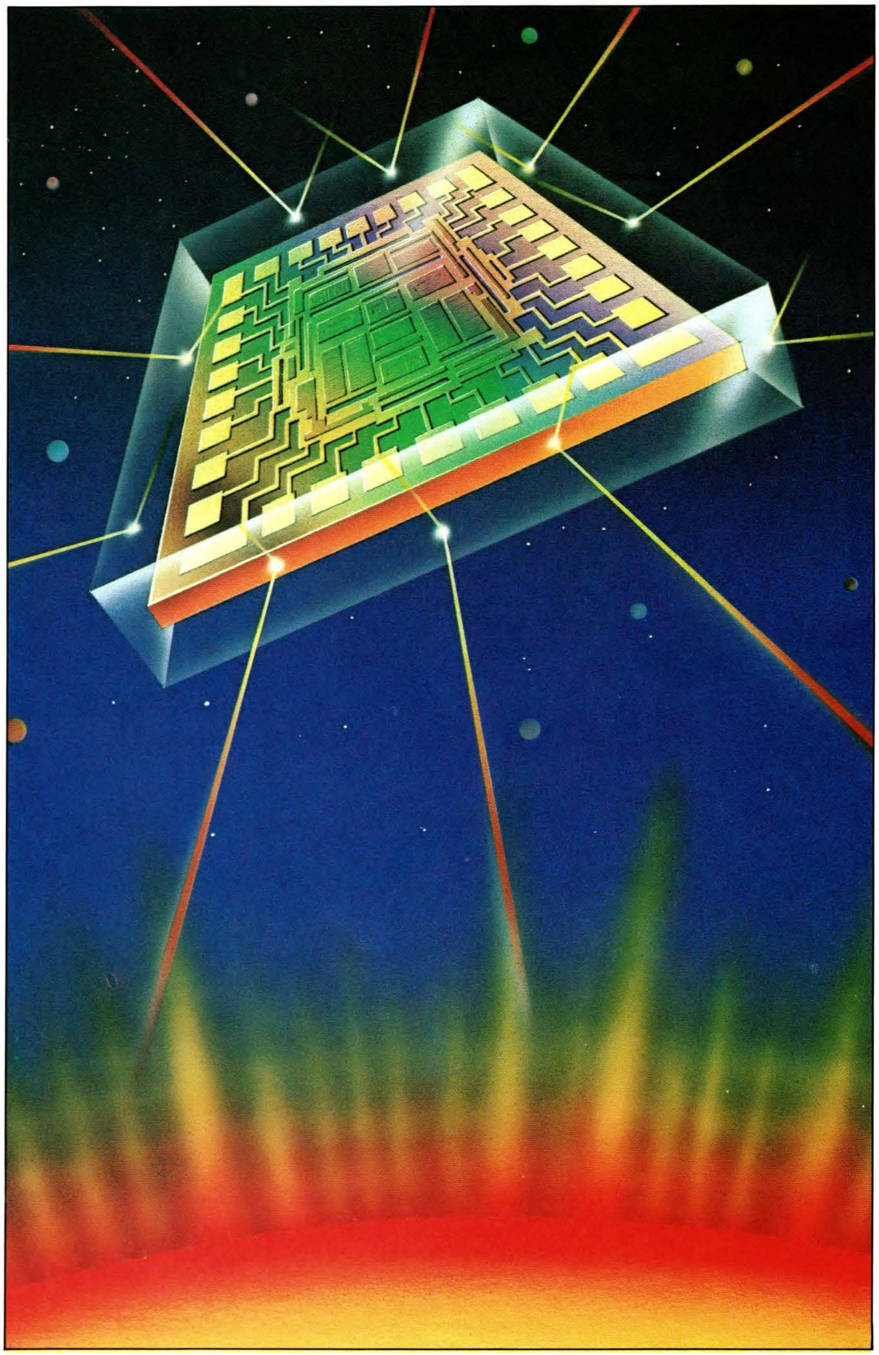
All STARPLEX peripherals and options—including ISE modules—also remain compatible with STARPLEX II.

To get the full story on STARPLEX II and its fully developed capabilities, check box 037 on this Anthem's coupon. And hear about a major development in efficiency.

STARPLEX, STARPLEX II and ISE are trademarks of National Semiconductor Corporation.

National conquers space with Megarad CMOS logic.

Presenting the industry's broadest line of metal gate CMOS devices capable of withstanding radiation levels in excess of 10^6 rads (Si).



Military and aerospace design engineers have long needed a dependable source of low power radiation-hardened logic devices. Bipolar components were radiation resistant, but required current supplies of several milliamps per gate. And although traditional CMOS operated at microamps per gate, they began to degrade at radiation levels well below 10^4 rads (Si).

But the Practical Wizards solved these problems with a full line of megarad hardened CMOS logic and memory circuits. In fact, National's intensive two-year research and development program has resulted in the industry's broadest line of metal gate CMOS products hardened to 10^6 rads (Si).*

So they're ideal for use in satellites and similarly demanding Mil/Aero applications.

The CMOS megarad line consists of devices ranging in complexity from simple gates to flip-flops to RAMs, all available with 883S/RETS™ or 883B/RETS™ processing.

What does rad hard really mean? National has insured the radiation tolerance of their rad hard devices through several methods.

The radiation-induced oxide charge and the formation of Si-SiO_2 interface states were minimized by converting from a wet to a dry oxidation process, with the gate oxide thermally grown in a pure oxygen atmosphere rather than in steam.

This gate oxidation is processed through a nitrogen annealling cycle, thus producing oxides highly resistant to ionizing radiation effects as well as having excellent pre-radiation MOS characteristics.

Since the E-beam aluminum evaporation process normally used on commercial CMOS ICs emits a soft X-radiation—which produces positive charge threshold shifts in the gate oxide and interface states similar to those seen during radiation—National uses induction heated evaporation of the aluminum rather than E-beam aluminum evaporation.

To minimize the effect of threshold voltage shifts, the Practical Wizards significantly raised the negative threshold voltage and brought the positive threshold voltage closer to zero. This was accomplished with absolutely no sacrifice in performance, even on such complex components as the MM54C200 256-bit RAM.

Megarad for maxisystems. The result of all this Practical Wizardry is the industry's broadest line of reliable and readily available CMOS logic and memory devices capable of withstanding the rigors of a radiation-filled environment.

For more on National's rad hardened line of CMOS devices, check boxes 062 and 079 in this Anthem's coupon.

*One rad (Si) is the quantity of any type of ionizing radiation which imparts 100 ergs of energy per gram of silicon.

Six tricks with low-cost 8-bit A/Ds.

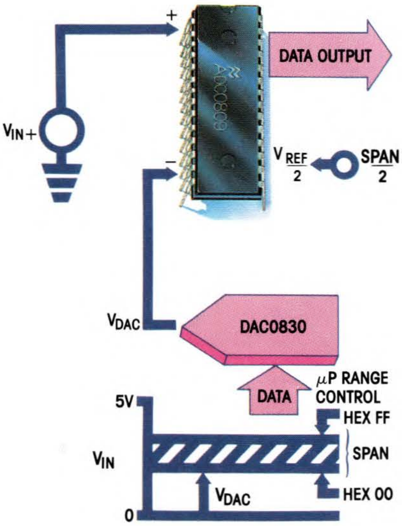
National Semiconductor's line of 8-bit A/D converters with differential input and span adjust—the ADC0801/02/03/04—are finding their way into all sorts of interesting applications. Here are just a few to stimulate the imagination.

1. Analog Self-Testing. More and more digital systems perform a self-test. To take this concept one step further, NSC's low-cost 8-bit A/Ds can be used to encode the analog voltages in a system—power supply voltages, comparator set points, reference voltages, etc.

This way, the microprocessor can ensure that all of the components are operating properly.

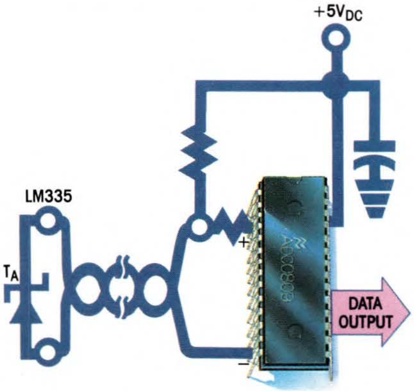
2. A μP-Compatible Comparator. Need a comparator that interfaces directly with the data bus? The differential input on the A/Ds allows the comparison of the input signal to a reference voltage.

3. High Resolution μP Ranging A/D



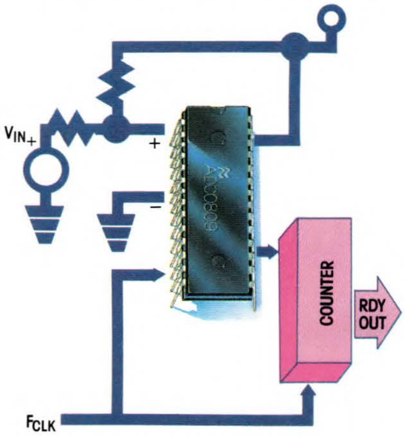
By increasing the apparent sensitivity of the 8-bit A/D, the effective resolution can be increased to give the same performance as more expensive 10- and 12-bit A/Ds.

4. Temperature Sensing



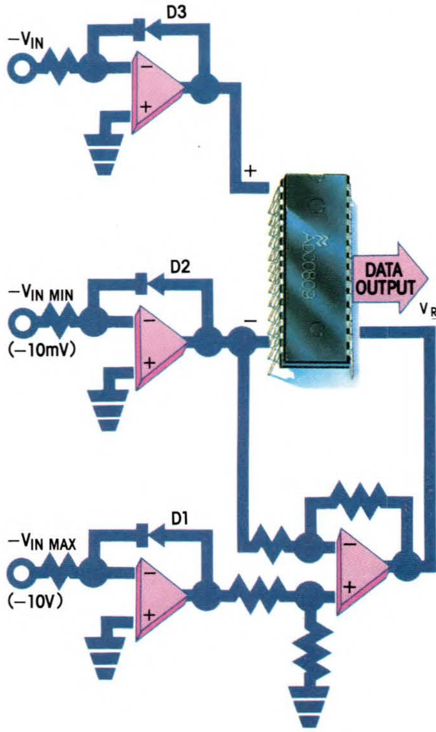
Since μPs are now used to control environmental and system temperatures, the combination of the LM335 and the A/D digitizes temperatures accurately and easily.

5. High-Speed A/D with Bipolar Input



To reduce the apparent conversion time to only a few μsecs, the A/D is operated in free-running mode. Two resistors are added enabling conversion of bipolar input signals (±5V, ±10V).

6. Three Decade Logarithmic A/D



When conversion of a wide dynamic signal range is required, this log A/D converts a three decade range.

ADC0801/02/03/04

- Total error ± ¼ LSB, ± ½ LSB, ± 1 LSB
- 100 μsec conversion time
- μP compatible
- Prices start at $2.95* @ 100 pieces

For more ideas and information on ways to use these versatile A/Ds, be sure to check boxes 023 and 051 on this issue's coupon.

*Prices shown are U.S. prices only.

Worlds ahead in data acquisition technology.

National Semiconductor is the world's largest supplier of data acquisition components. In fact, they ship more A/Ds than anyone else. Over the last year, for example, they shipped over 5 million A/Ds.

The key to NSC's lead over the rest of the pack is their high volume production capabilities and extensively broad line, and their commitment to high performance at a low cost. With all of their transducers, amplifiers, filters, MUXs, sample and hold circuits, references, A/Ds and D/As, there's an NSC part for every application.

In addition, they're the only supplier utilizing technologies of bipolar, CMOS, NMOS, and hybrid along with thin-film resistors and laser trim.

This is just a glimpse into what they're up to—designing high technologies into practical high performance data acquisition components.

National Semiconductor, the dedicated leader in data acquisition technology and components.

National Semiconductor–the best reference for references.

2.5V micropower and low cost 5.0V references join the industry's broadest line of high performance IC voltage references.

The Practical Wizards at National have a linear IC voltage reference for every application. No one else can offer it all:

- Broadest line—over 35 references to choose from
- Lowest power—12μW (LM385-1.2V)
- Lowest drift—.5ppM/°C (LM199AH)
- Lowest prices—$.45* @ 100 pcs. (LM329DZ)
- Widest range of voltages—1.2V to 10.24V
- Tight tolerance—±0.01% (LH0070)

That's why National is the industry's best reference for references.

The LM385-2.5V micropower reference. The LM385-2.5's low power drain (50μW) enables battery life to actually approach shelf life.

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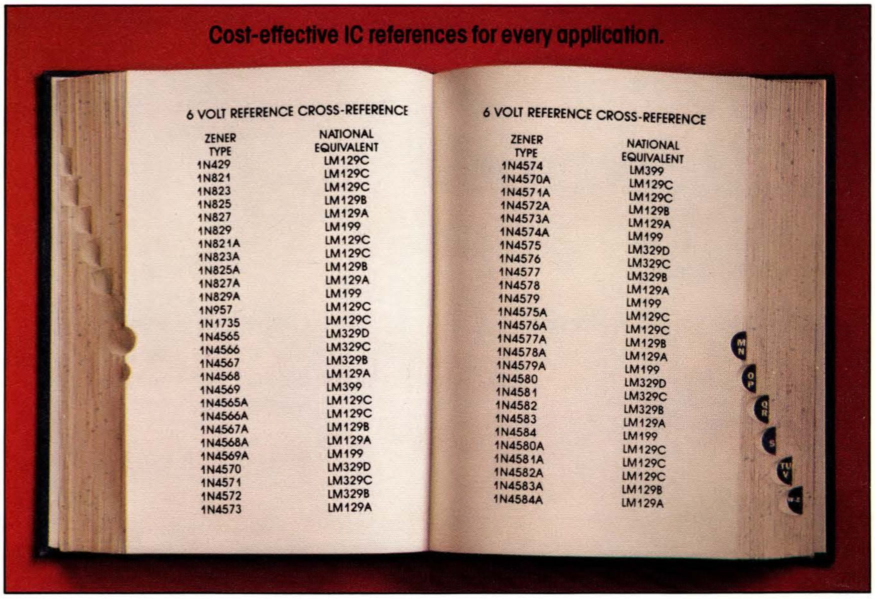
Be sure to check boxes 053 and 058 on this issue's National Archives coupon for complete details on the new LM385-2.5, LM336-5.0 and all the rest of the superior linear references.

*Prices shown are U.S. prices only.



What's new from the National Archives?

- 023 ☐ ADC0801-4/ ADC0808-9/ ADC0816-17 A/D Converter Data Sheets
- 037 ☐ STARPLEX™ and ISE™ Information
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- 052 ☐ Free Subscription to the Data Update
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NA 29

countable, and analog involves aggregates (eg, rms values that must somehow be measured because they can't be counted), the world is necessarily *both analog and digital.*

I find this thought philosophically quite comforting. It harmonizes with the dual outlook on the nature of radiant energy (wave vs particle) that challenged natural philosophers for centuries and was solved only by Planck's quantum theory, relating the discrete and the continuous.

Perhaps the analog/digital argument will be resolved if someone invents a device that quantizes aggregates to produce a digital measurement of an analog quantity, and a corresponding device to produce an aggregate in response to a count. We would call them A/D and D/A converters.

Now that I've proposed a concept, do you suppose it's possible for someone to invent devices that incorporate it?

Sincerely,
Dan Sheingold
Analog Devices
Norwood, MA

Note correct number

The phone number listed for Viking Connectors Inc in EDN's April 1 issue (pg 91) was incorrect. The correct number is (213) 341-4330.

Debating IC-IQ-quiz answers

Dear Editor:

Mr Anonymous made some valid points concerning the IC IQ quiz (EDN, May 27, pg 18). Admittedly, some quiz answers are debatable; therefore, I allowed for a range of correct answers in determining IC IQ. However, if Mr Anonymous flunked the quiz, he has a problem with more than he's debating.

In response to the Question 1 comment, I agree that throwing away parts at final test is expensive. In fact, Mr Anonymous argues that he'll reduce wafer-probe yield to improve final test yield. If so, wafer-probe yield becomes the major yield factor, as my answer indicates. This will normally be the case for mature IC products.

Not being able to use all the components on a semicustom IC results in the user's paying for

Signals & Noise

unused silicon real estate. Worse yet, two or more semicustom ICs, and perhaps additional discrete components, are usually required to do the job of one custom IC. System costs are almost always higher with semicustom ICs because of the larger number of parts, increased circuit-board area and additional assembly labor, testing and inventory. These disadvantages must be weighed against the higher development cost and increased turnaround time for a fully customized design.

In debating Question 5, Mr Anonymous states that the LM709 has an input equivalent noise voltage of 5 $nV/\sqrt{Hz}$. I'd like to see the data sheet that contains this spec. I checked with the LM people at National Semiconductor, and they don't specify noise parameters for this part. Neither is it on the data sheet from Fairchild, the originator of the 709.

In all fairness, though, I'm also in error. BiFET and BiMOS op amps generate much lower low-frequency noise current (not voltage) and have noise voltage comparable to that of conventional op amps. Total noise performance is far superior for the BiFET and BiMOS units in high-impedance applications, however. *(Ed Note: For a review of the latest advances in op amps, see EDN, April 15, pg 49.)*

Finally, the jury is still out deciding whether CMOS is the premier processing technology of the decade. In the meantime, I'm continuing to combine linear and digital functions on one chip using bipolar I^2L techniques. Perhaps by 1990, CMOS will be the correct answer to the question, but it's not today.

Sincerely yours,
Wesley A Vincent
Delco Electronics
Kokomo, IN

(Ed Note: For a different opinion on the potential of CMOS, see the Special Report beginning on pg 88.

(Additionally, the 709's low noise is indeed a well-kept secret, but it's a fact because of the rich bias for the emitters of the device's first-stage transistors.)

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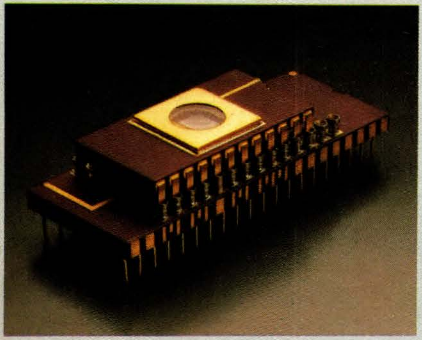

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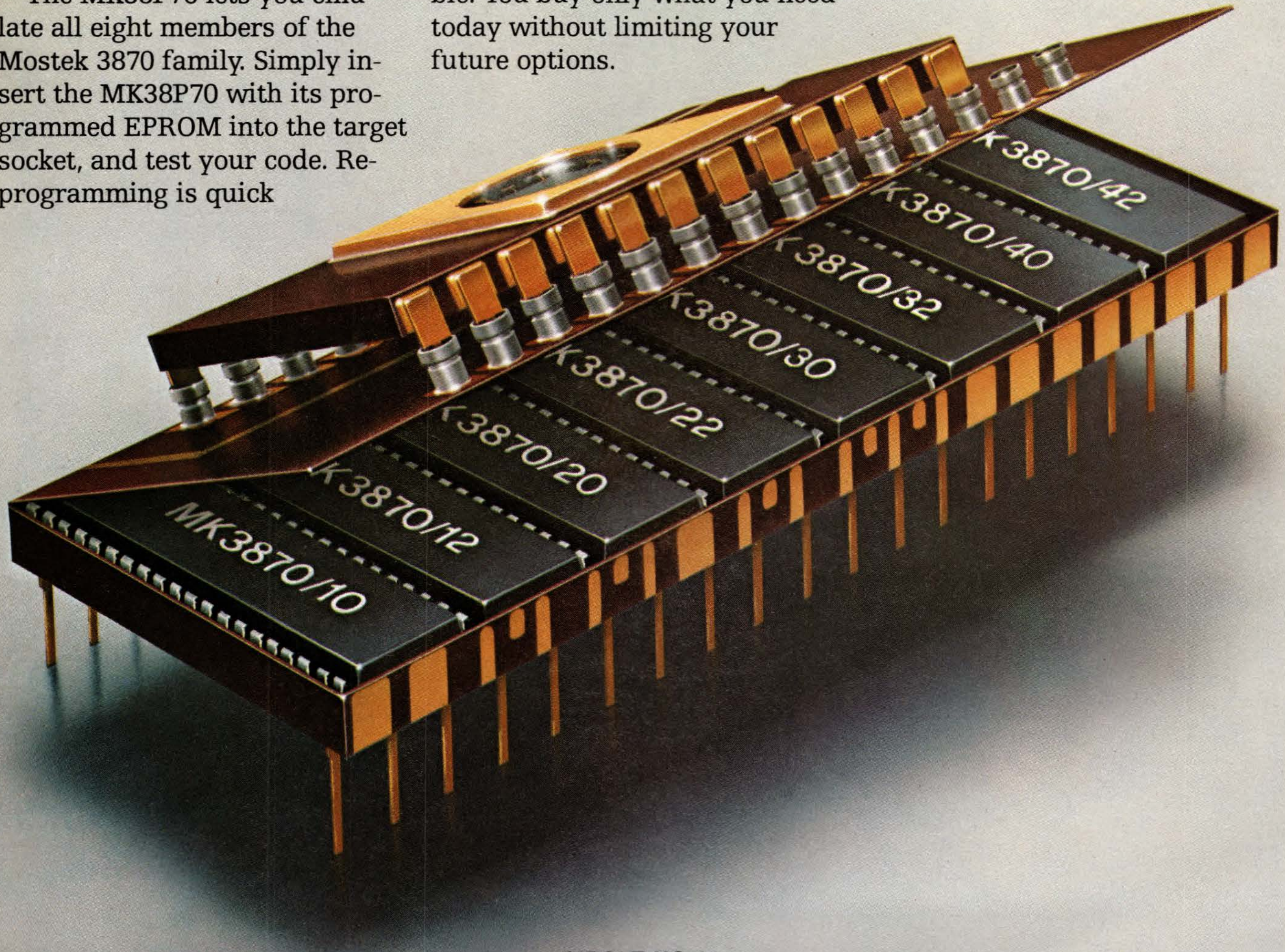

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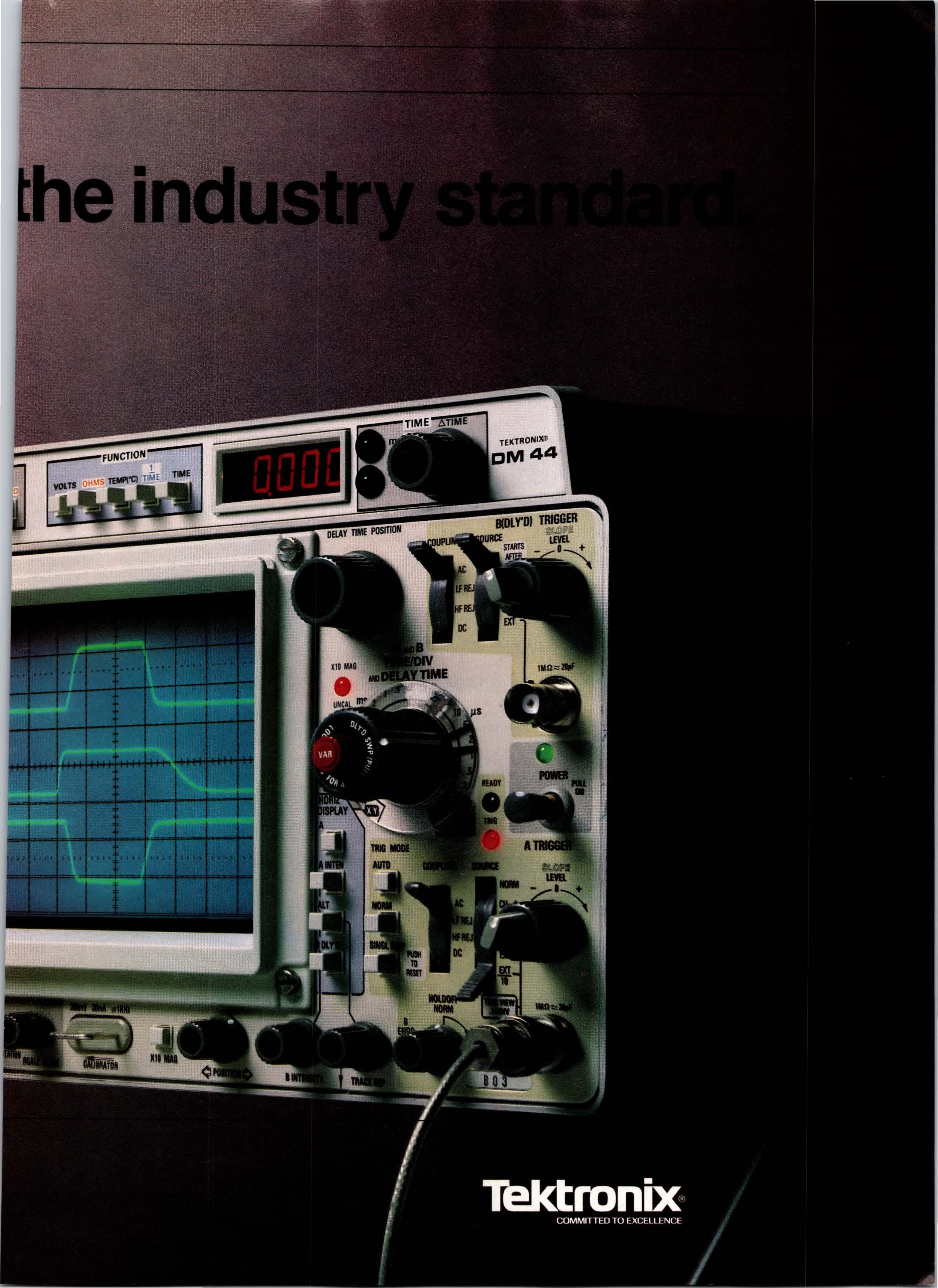
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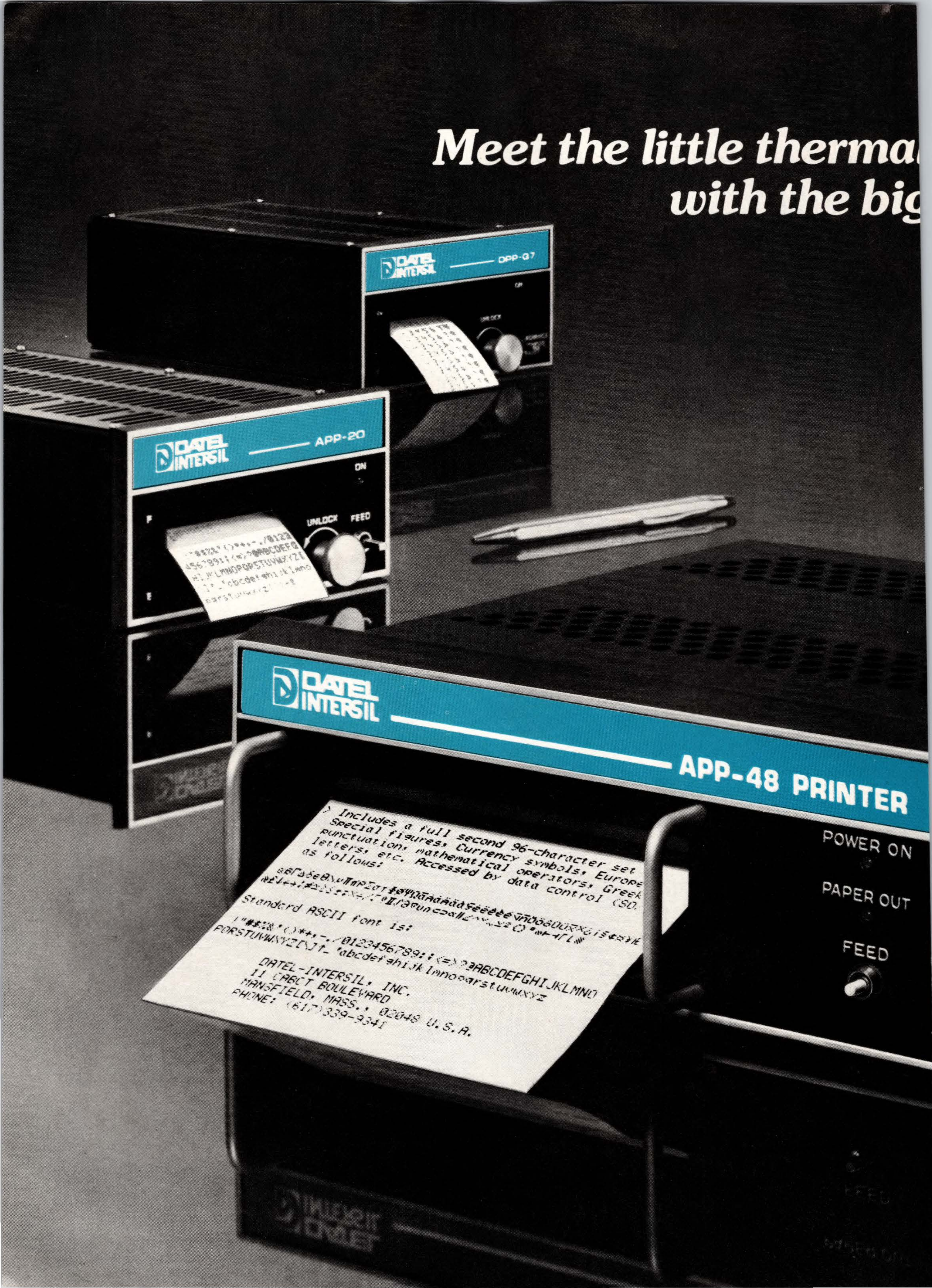
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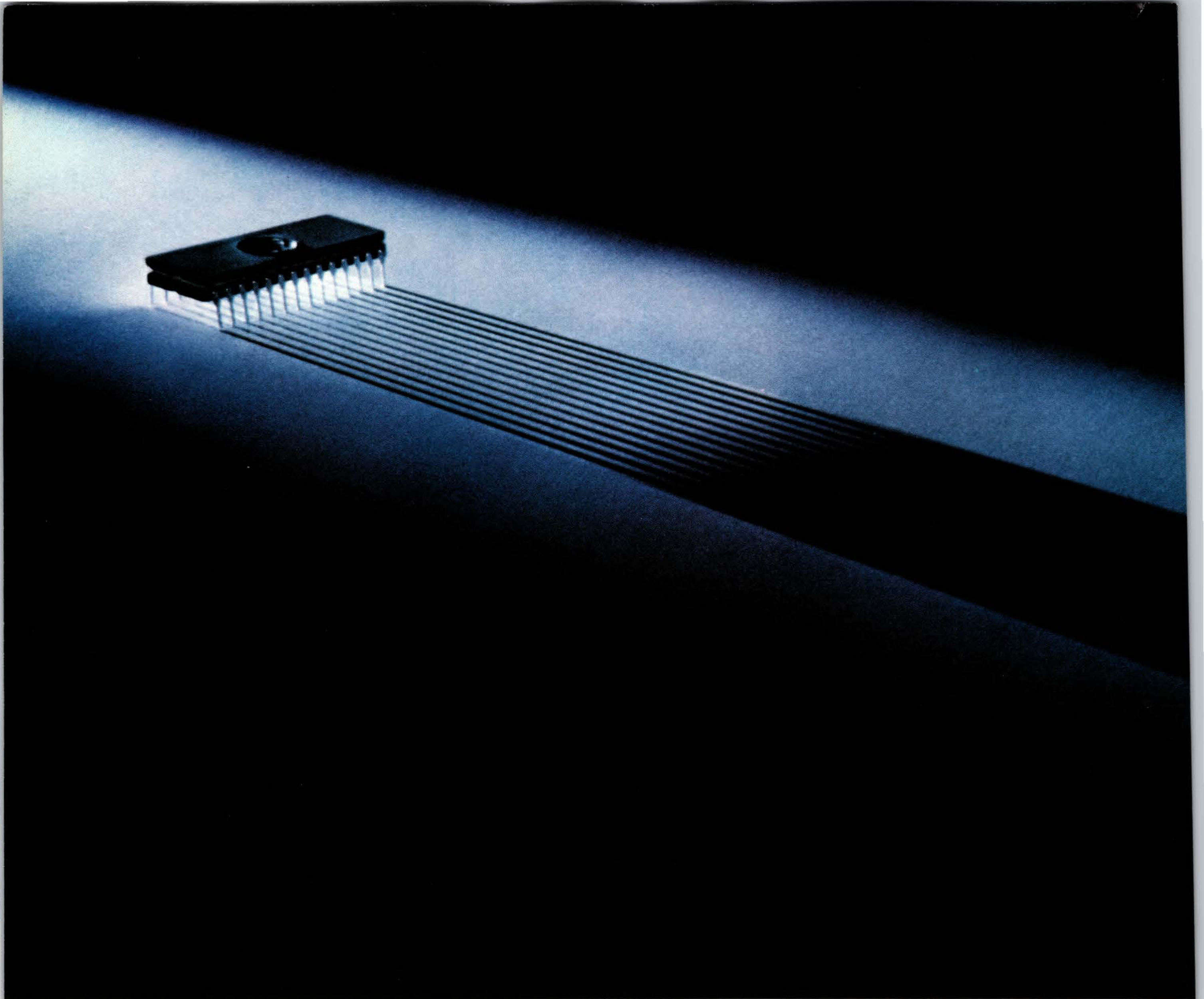

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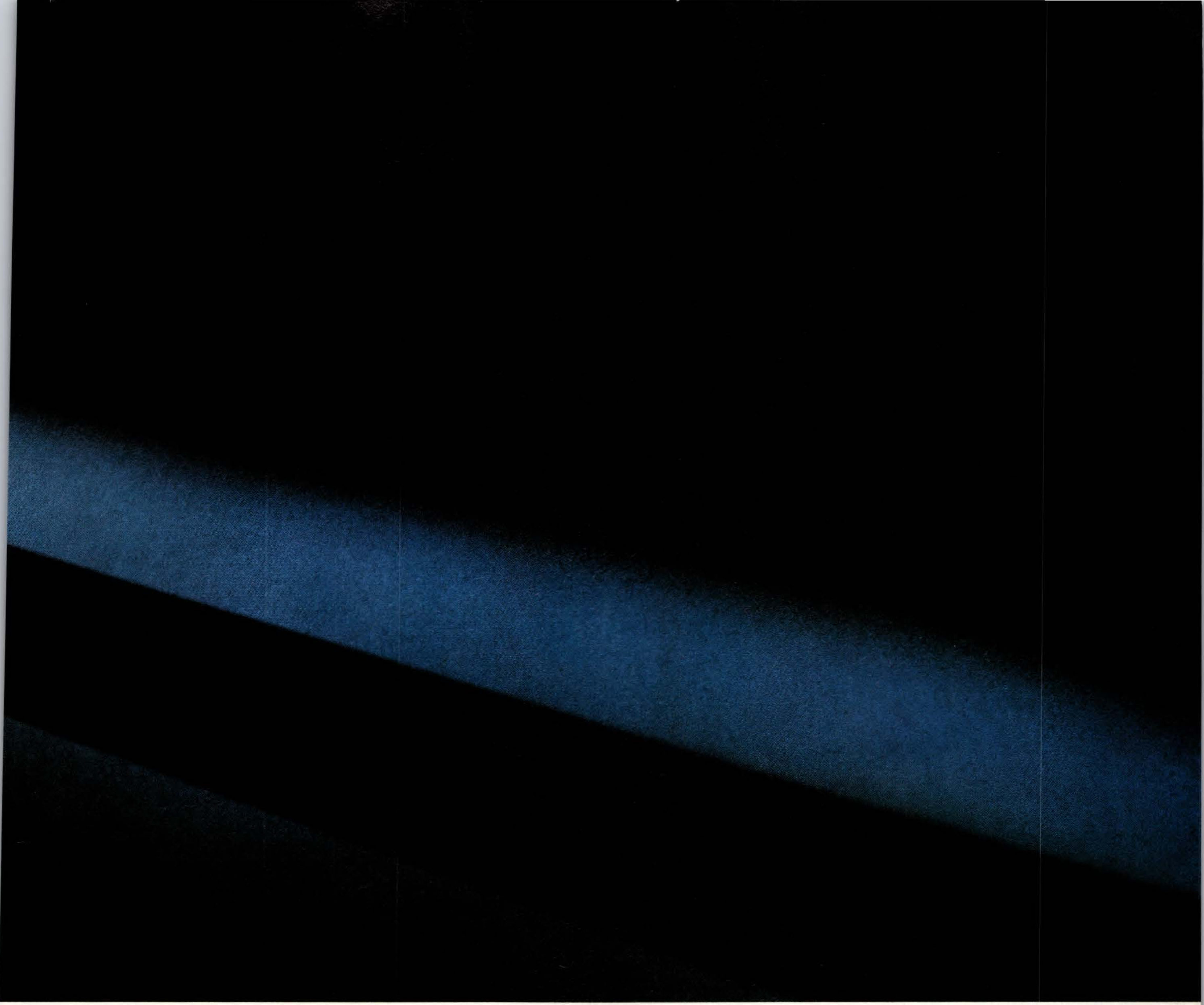

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CIRCLE NO 16

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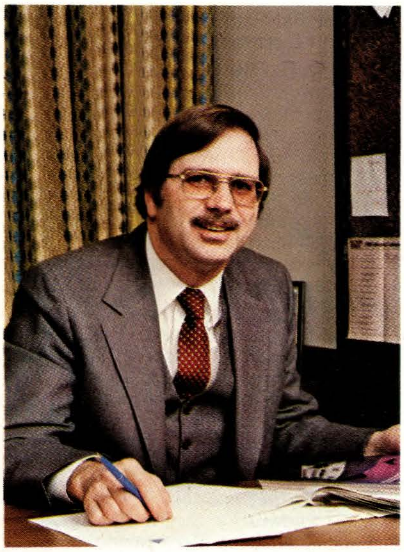
Editorial



Unfair competition?

Promotional literature from the Applied Technology Center, Dept of Engineering, University of Massachusetts that actively solicits contract R&D work raises some interesting questions. Mailed at taxpayer expense, this brochure and its accompanying cover letter from the ATC director state that the ATC "utilizes the combined experience and expertise of all the faculty members, graduate students (300) and facilities of our engineering school." Moreover, it boasts that "the price for this work is often less than internal company engineering costs."

Irwin Feerst, chairman of the Committee of Concerned EEs, who passed this information along to us, decries the fact that university officials are using a taxpayer-supported, tax-exempt organization to do industrial work. He further speculates that the graduate students might well be recruited to work for free under the familiar guise of obtaining a "learning experience." Thus, he concludes that the ATC's activities are akin to wage busting and that they represent "a blatant attempt by the university to grab off some of the work that is typically done by industrially employed engineers or private consultants."

Perhaps you believe that Mr Feerst has a valid criticism, but EDN does not, for three reasons. First, Massachusetts currently enjoys a very low unemployment rate among EEs, as pages upon pages of professional help-wanted ads continually attest. And we believe that a critical shortage of EEs will exist in the entire United States for the foreseeable future.

Second, and even more to the point, we believe that interplay between the academic community and private industry is a healthy and indeed vital activity; it should be encouraged, not discouraged. All too often, college faculties—and thus their student populations—remain blissfully unaware of the actual requirements of the fast-changing electronics industry. The unnecessarily long times companies spend to bring recently graduated students up to speed is outrageously wasteful.

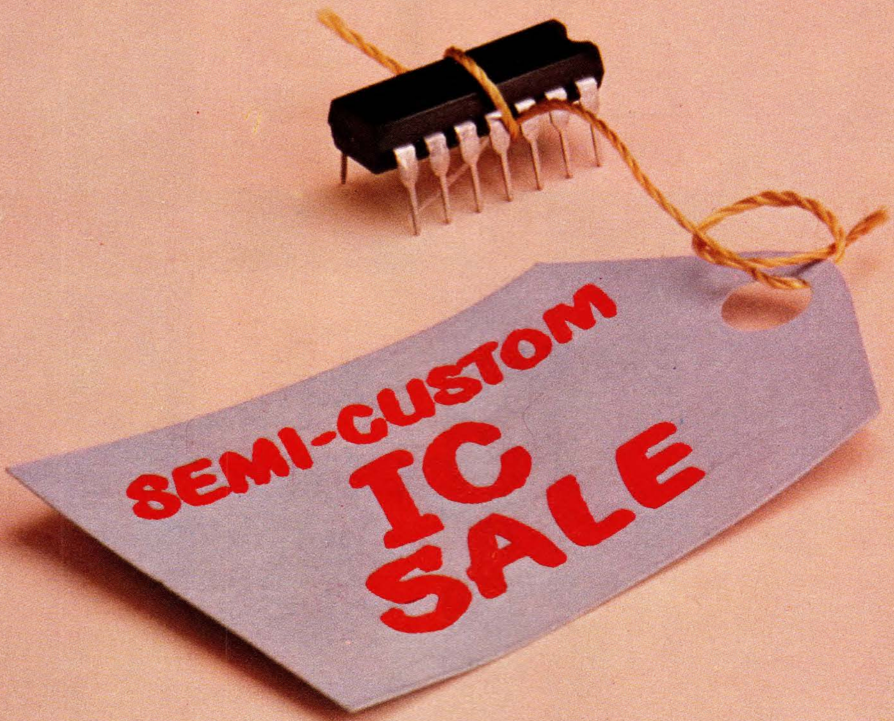
Third, the many valuable contributions made by researchers at colleges and universities under contract to electronics-industry firms are legion. Many extremely productive relationships exist in the Silicon Valley area—and indeed, throughout the rest of the US and the world.

The more the academic community can learn from and (especially) contribute to commercial R&D efforts, the better off EEs as a group will be. The benefits of university "competition" clearly outweigh the disadvantages.

Walt Patstone

Walt Patstone
Editor

Staff



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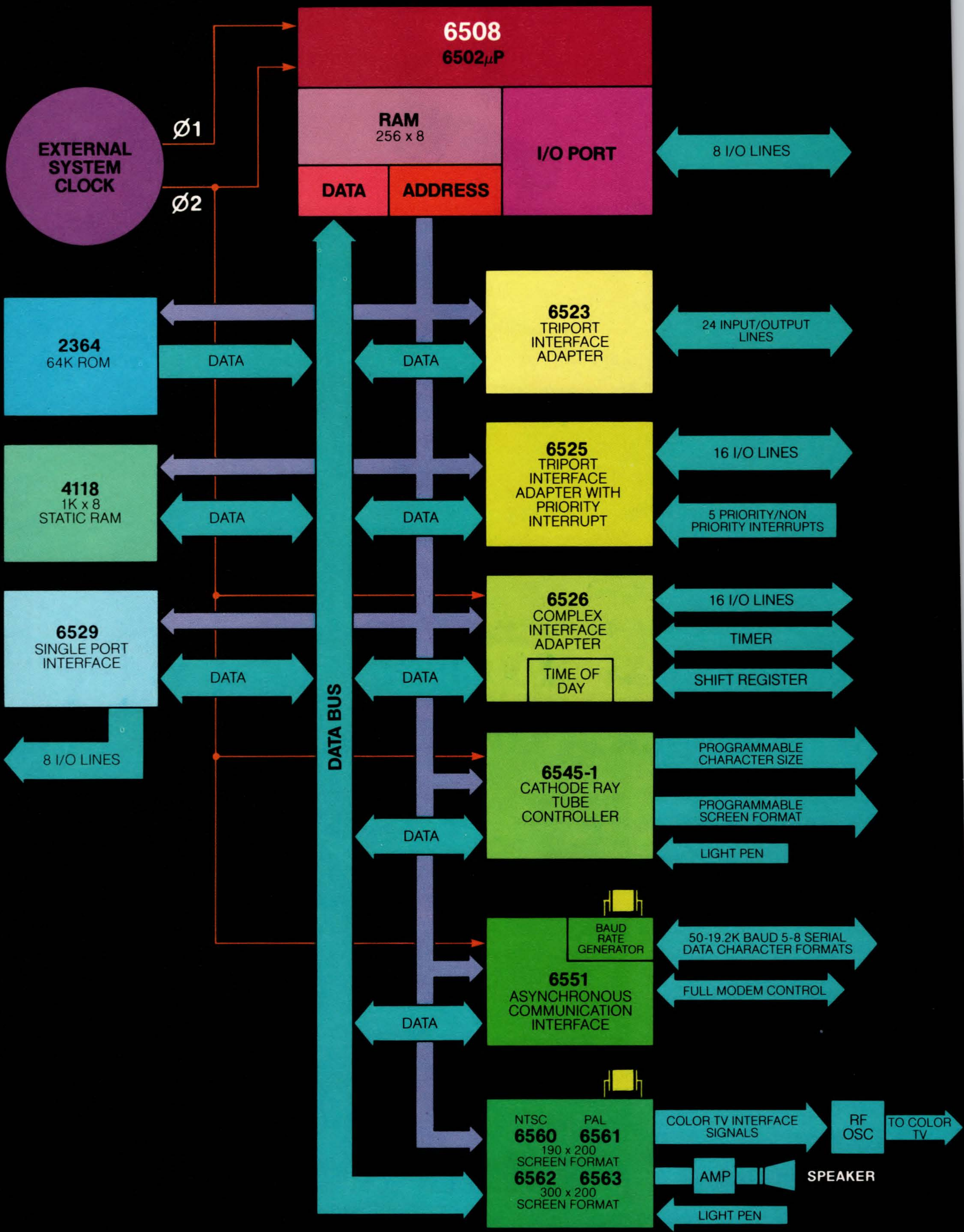

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CIRCLE NO 19

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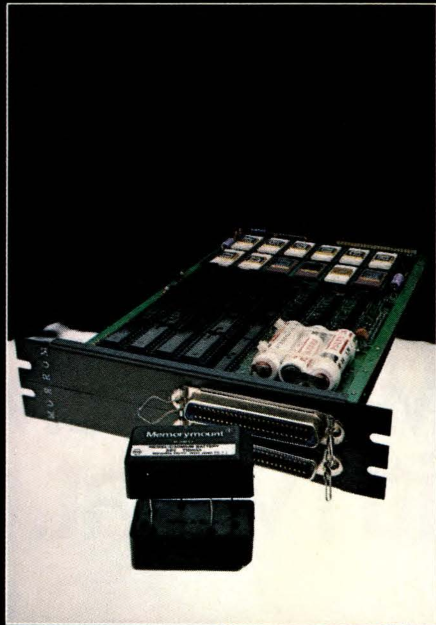

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CIRCLE NO 20

Semiconductor lasers shine, thanks to improved performance, reliability

Dale Zeskind, Contributing Editor

Semiconductor lasers are finding increased use in a variety of communications and instrumentation applications as manufacturers continue to make great strides in improving performance and reliability and reducing costs. No longer must you be an optical-system specialist to use or afford these versatile components.

Readily available

A wide variety of domestic and foreign firms currently manufacture and stock semiconductor lasers. Although the growth of fiber-optic communications has provided the major impetus in these devices' development, additional emerging applications include optical recording and playback, laser printers, character and bar-code readers, distance-measuring equipment, proximity detectors, target illuminators and a host of medical instruments.

Conveniently packaged in dual-in-line, TO-8 and other industry-standard enclosures, semiconductor lasers can readily adapt to your needs (EDN, May 13, pg 78). For guided-wave applications, for example, devices come with fiber-optic pigtails that allow simple interconnection to communications data links. And for free-space applications, you can purchase the lasers packaged with optical windows or lenses. Alternatively, you can obtain the laser chip mounted on a heat sink but otherwise unpackaged **(Fig 1).**

Some manufacturers offer lasers prepackaged with integral light-level detectors for external feedback control of light-level output. Still others offer integral thermoelectric coolers to stabilize device performance over widely varying ambient temperatures. And, of course, manufacturers furnish complete transmitter modules requiring only power and signal inputs **(Fig 2).**

Multimode lasers communicate

You can purchase three main types of semiconductor lasers: cw (continuous wave) multimode, cw single mode and pulsed (see **box,** "Semiconductor-laser fundamentals"). CW multimode lasers (multiple longitudinal or frequency modes, with a single transverse or spatial mode) currently find wide use in fiber-optic communications applications (EDN, May 13, pg 226). They readily couple to standard graded-index multimode fiber cable (50-μm core diameter) with coupling efficiencies approaching 50 to 60%. Similarly, they couple to single-mode fiber (whose core diameter ranges from 4 to 9 μm), but in that case coupling efficiency is only 10 to 15%.

With 0.8- to 0.9-μm output wavelengths, the devices generate up to 10 mW of cw light output at the chip. And multimode devices with 1.3-μm outputs are just now becoming commercially available. Here, too, maximum cw power outputs are approaching 10 mW. Cost of the shorter wavelength units approaches $100 in quantities of 1000.

You can modulate the lasers at rates exceeding 1 GHz. In practice, however, fiber-optic-cable dispersion limits acceptable data rates. (The laser's multiple longitudinal modes travel through the cable at slightly different velocities, thereby distorting the signal waveform.) System designers have achieved 45M-bps data rates over a 23-km link and 90M bps over an 18-km link.

Single-mode lasers record, read

The second commercially available laser type, cw single-mode

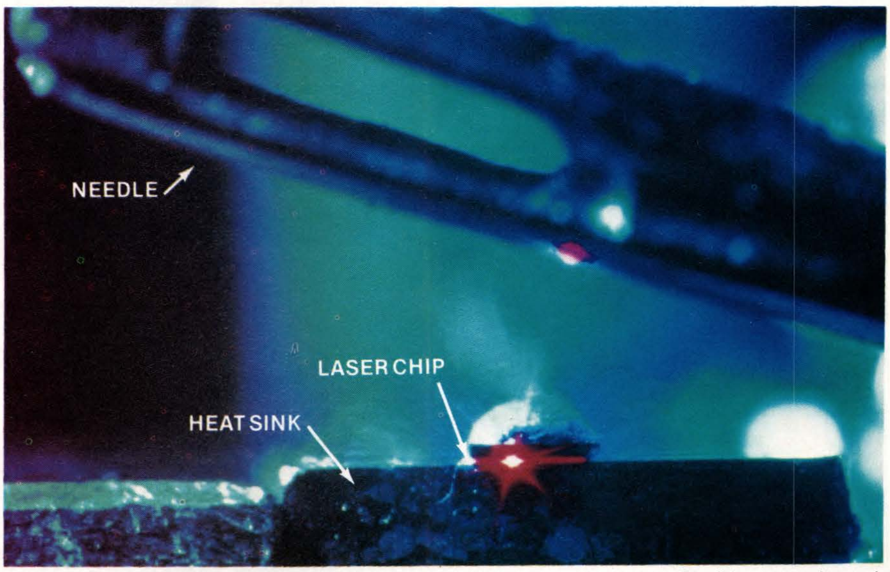

Fig 1—This AlGaAs semiconductor laser *measures 10×4×8 mils (it's seen here in comparison with the eye of a needle) and generates approximately 5 mW of 0.82-μm-wavelength light output. At the chip, the light-beam cross section measures 1.5×3 μm, corresponding to an optical power density of $1\times10^5 W/cm^2$. The photo was taken with infrared-sensitive film to capture the otherwise invisible beam. (Photo courtesy RCA Sarnoff Research Center)*

lasers (single longitudinal or frequency mode and single transverse or spatial mode) currently have limited application to fiber-optic communications. Their spectral purity makes them attractive only for special-purpose long-haul data links. However, even in this application they require single-mode cable for effective use.

Therein lies the difficulty: Mechanically aligning the laser's 1×3-μm beam cross section with a 4- to 9-μm-diameter single-mode cable proves a formidable task. Only a few manufacturers have developed interconnections that can survive the thermal and mechanical stresses a junction experiences.

Nevertheless, several manufacturers have active programs to perfect such single-mode devices for the optical-recording and -playback market—whose potential far exceeds that of fiber-optic communications (EDN, April 29, pg 244). Single-mode lasers' spectral purity and phase stability are critical features for many such recording and playback applications.

Currently, these devices are available with 2- to 10-mW light-power outputs at the chip. They connect to a single-mode cable with coupling efficiencies limited to 10 to 15%. Although currently more expensive than multimode lasers, single-mode units will soon match the costs of their multimode counterparts, according to several industry experts.

Pulsed lasers illuminate

In the third commercially available semiconductor-laser category, pulsed lasers exhibit both multiple transverse and multiple longitudinal modes. They achieve 1 to 90W peak pulse power and find use primarily as high-power illumination devices for rangefinders, battlefield target illuminators and proximity detectors. Prices range from $15 and up in quantity. Beware, however: Pulsed lasers have stringent duty-cycle requirements and can't operate as cw devices under any

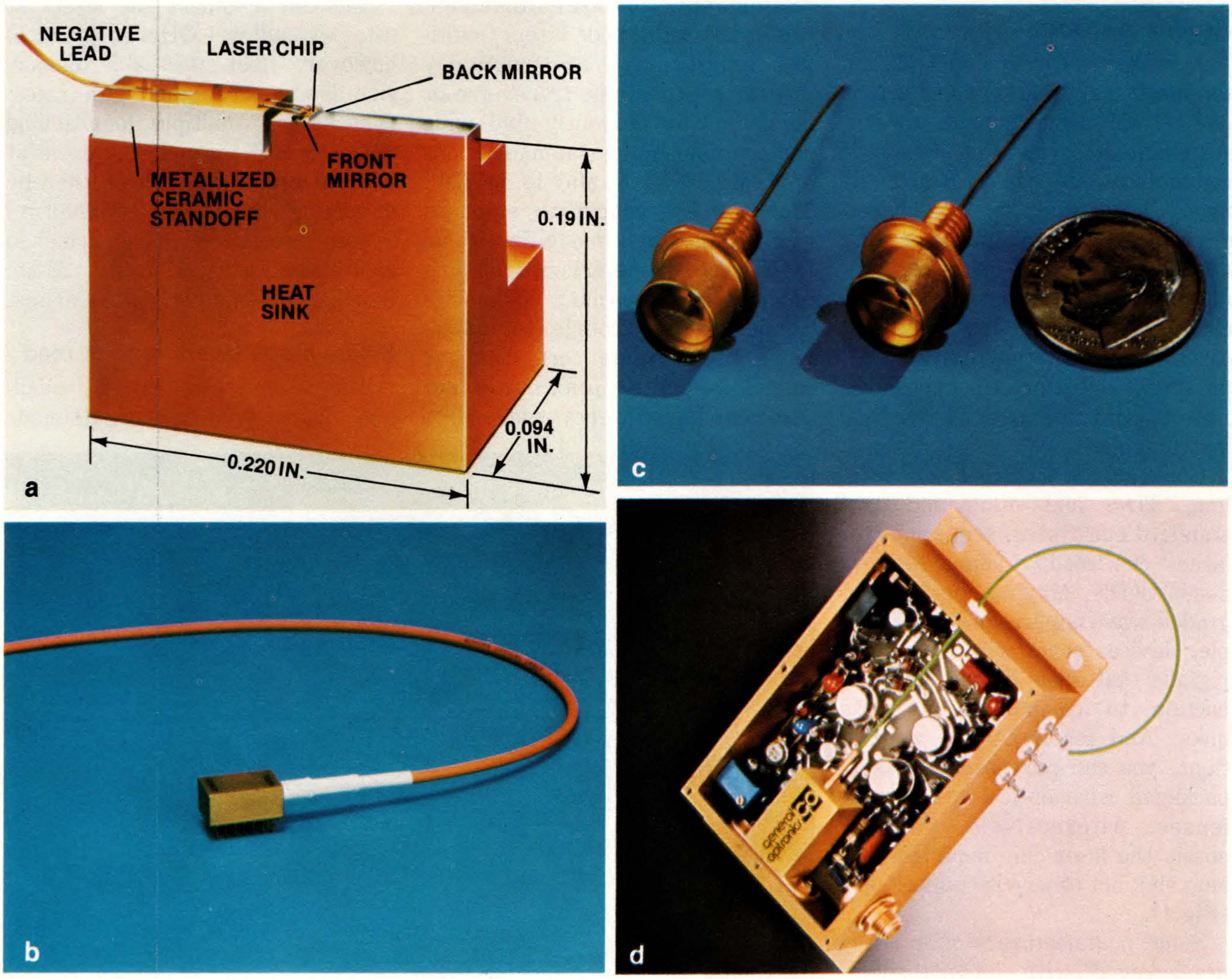

Fig 2—Extremely high optical power densities, *often exceeding $10^6 W/cm^2$, necessitate the use of relatively large heat sinks, such as in the General Optronics device shown in* **(a)**, *when mounting semiconductor-laser chips. The chips come in dual-in-line* **(b)**, *TO-8 and other convenient enclosures, including the RCA model shown in* **(c)**. *The device in* **(b)**, *from Optical Information Systems, includes an integral thermoelectric cooling element to help stabilize laser operation over widely varying ambient temperatures. You can also purchase modular laser trasmitters from manufacturers such as General Optronics* **(d)**; *they require nothing more than power and signal inputs.*

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circumstances.

Watch the trends

Semiconductor-laser technology remains an area of active research. Investigators around the world are studying ways to improve device power-handling capability, lifetime, linearity and temporal stability.

For cw multimode lasers, researchers place emphasis on developing longer wavelength (1.3 μm) devices to match conventional glass fibers' attenuation minima. But until recently, the lack of suitable detectors limited practical system operation at that wavelength.

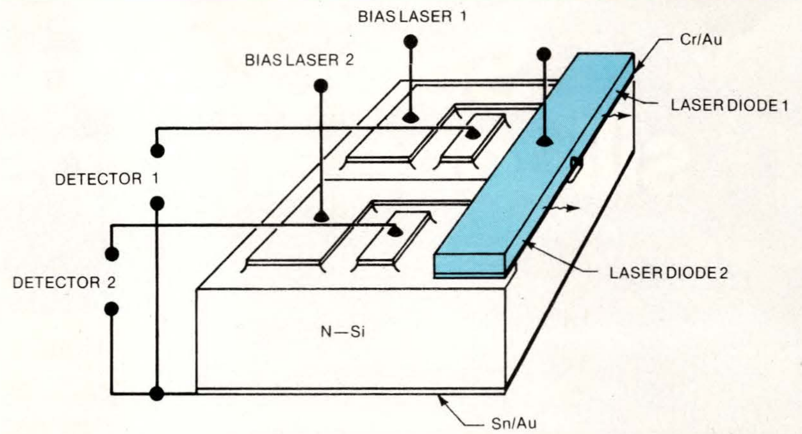

Fig 4—Integrated optics got a boost *when researchers at Xerox succeeded in integrating multiple lasers and optical power-level detectors onto one substrate.*

For both single-mode and multimode devices, work continues toward developing better techniques for aligning and bonding single-mode fibers to laser chips. Conventional epoxy techniques exhibit insufficient stability-vs-temperature characteristics for many applications. General Optronics, however, reports the development of a metal-based bonding technique that it claims significantly minimizes the problem.

For cw single-mode lasers, much of the research effort focuses on increasing the devices' optical-power output, again with optical-recording applications in mind. For example, a group at RCA's David Sarnoff Research Center (Princeton, NJ), led by researchers D Botez and J Connolly, has apparently achieved some success **(Fig 3).**

Experimenting with an innovative device structure termed constricted double heterostructure, this group has achieved single-longitudinal-mode cw-laser outputs of more than 40 mW. It has also recorded data directly onto a videodisk using a device similar to that shown in **Fig 3,** doing away with the need for bulky gas lasers.

The promise of integrated optics

If you've ever considered the possibility of integrating additional functions—both optical and electrical—onto a semiconductor laser's

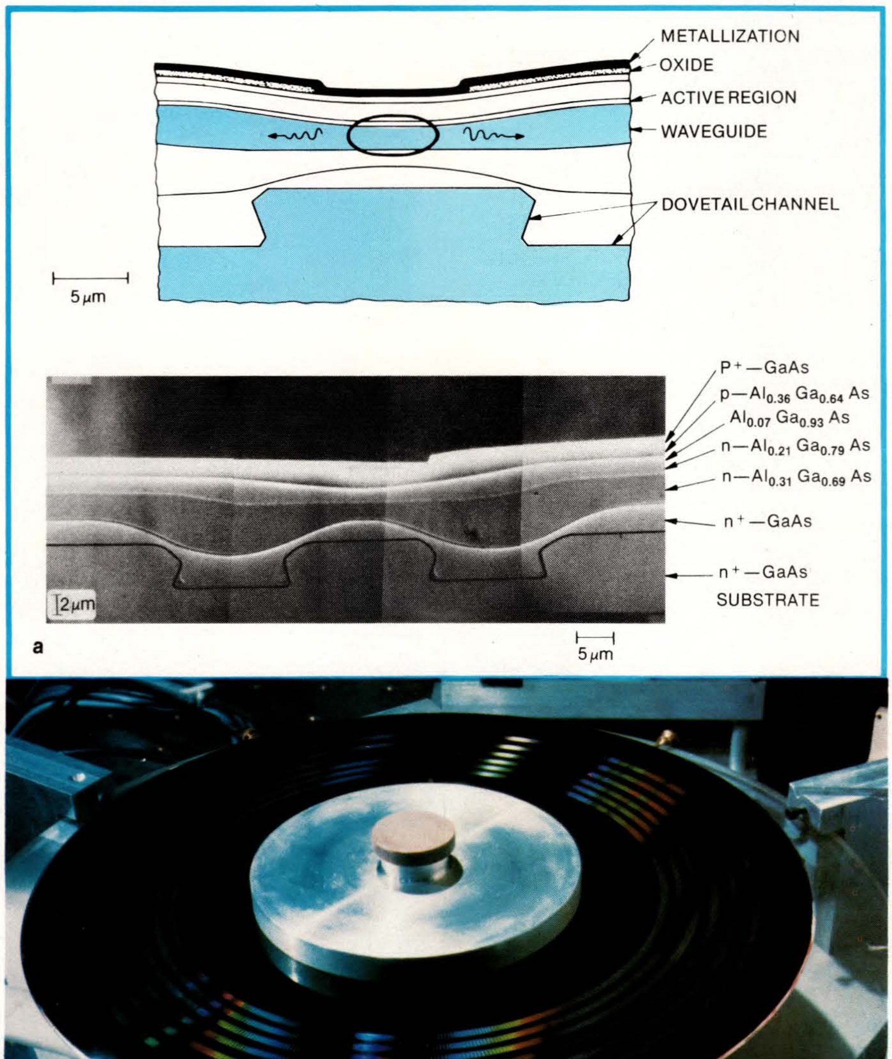

Fig 3—In hopes of increasing laser power output, *researchers experiment with new device structures such as this constricted-double-heterostructure device from RCA* ***(a).*** *Optical-disk recording and playback applications* ***(b)*** *serve as a major impetus for much current semiconductor-laser research.*

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substrate, you aren't alone. Researchers have pursued this concept, termed integrated optics, since the early 1970s. Several labs, for example, have succeeded in integrating several lasers onto a single substrate. And a group at the Xerox Palo Alto Research Center (Palo Alto, CA), led by D Scifres, has gone one step further by adding on-chip photodetectors to stabilize a 2-laser array's output power **(Fig 4).**

One objective of integrated-optics proponents is to develop a totally

Semiconductor-laser fundamentals

Fig A diagrams a basic semiconductor-laser structure. The device consists of three epitaxial layers deposited on a substrate along with appropriate metallizations.

The active-recombination layer (light-generating layer) is sandwiched between two oppositely doped cladding layers. When voltage is applied, electrons from the n-type cladding layer combine with holes from the p-type layer, producing a photon. The cladding layers' refractive indexes are lower than that of the recombination layer and therefore trap the photon within the recombination layer. Mirrored facets at each end of the device provide the optical feedback required to support lasing.

The two junctions formed between the two cladding layers and the recombination layer are termed heterojunctions. Device designers designate these junctions' combination as a double-heterojunction structure or double heterostructure (DH). Designers typically use GaAs-GaAlAs to fabricate 0.8- to 0.9-μm-wavelength lasers and InGaAsP-InP for units with output wavelengths of approximately 1.3 μm.

The lateral width of the laser's current distribution shown in **Fig A** determines the light-beam output, width and transverse-mode stability. Consequently, much device research focuses on ways to control this current distribution.

Fig B graphs the light-power output vs current input for a typical semiconductor laser. When the input current exceeds the threshold value, the device begins to lase. The slope of the curve (in milliwatts per milliamp) signifies the device's differential quantum efficiency—a parameter often included in manufacturers' spec sheets that helps you evaluate a

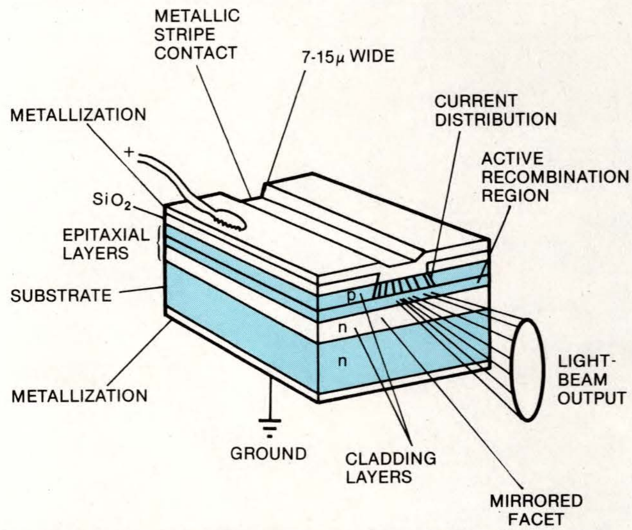

Fig A—Double-heterostructure semiconductor lasers *trap photons in an active recombination layer. Mirrored facets provide the optical feedback necessary to sustain lasing.*

DEFINITIONS OF SEMICONDUCTOR-LASER TYPES

COMMON LASER DESCRIPTIONS	FEATURES: TRANSVERSE MODE	FEATURES: LONGITUDINAL MODE	APPLICATIONS
cw MULTIMODE	SINGLE TRANSVERSE MODE (SINGLE SPOT)	MULTIPLE LONGITUDINAL MODES (MULTIPLE FREQUENCIES)	CAN BE OPERATED EITHER cw OR PULSED (ANALOG OR DIGITAL MODULATION) USED PRIMARILY FOR FIBER-OPTIC COMMUNICATION APPLICATIONS WITH EITHER MULTIMODE GRADED INDEX FIBER (50- μm CORE DIAMETER) OR SINGLE-MODE FIBER (9-μm CORE DIAMETER)
cw SINGLE MODE	SINGLE TRANSVERSE MODE (SINGLE SPOT)	SINGLE PREDOMINANT LONGITUDINAL MODE (SINGLE FREQUENCY)	CAN BE OPERATED EITHER cw OR PULSED (ANALOG OR DIGITAL MODULATION) USED MAINLY FOR OPTICAL RECORDING AND PLAYBACK APPLICATIONS. FINDS SOME LIMITED USE IN FIBER-OPTIC COMMUNICATIONS.
PULSED	MULTIPLE TRANSVERSE MODES (MULTIPLE SPOTS)	MULTIPLE LONGITUDINAL MODES (MULTIPLE FREQUENCIES)	CAN ONLY OPERATE PULSED. DEVICE WILL SELF DESTRUCT IF OPERATED cw. USED AS A HIGH-POWER PULSED LIGHT SOURCE FOR APPLICATIONS SUCH AS TARGET ILLUMINATORS AND RANGEFINDERS.

integrated fiber-optic communications repeater. Toward that end, researcher A Yariv and colleagues at the California Institute of Technology (Pasadena, CA) have experimented with the structure shown in **Fig 5.** They achieve optical gains (light output vs light input) exceeding 10 dB with devices similar to this one.

Some major new developments in integrated optics could soon appear. Several industry experts have observed a significant increase in such projects' in-house funding at

device's relative conversion efficiency.

The curves indicate that input currents below threshold cause the device to produce a small amount of incoherent spontaneous light output similar to that of an LED. Most applications call for minimizing this spontaneous emission.

Manufacturers' literature commonly refers to three types of lasers: cw (continuous wave) multimode, cw single mode and pulsed. Rarely, however does their literature clarify these terms.

To understand the classifications, consider that the mode structure of a semiconductor laser's light beam is characterized both transversely and longitudinally. The transverse mode pattern depicts the spatial distribution of light within the beam's cross section. Typical cw lasers produce a single transverse mode or single spot. You can observe the transverse-mode pattern through a microscope focused on the laser's output facet **(Fig C).**

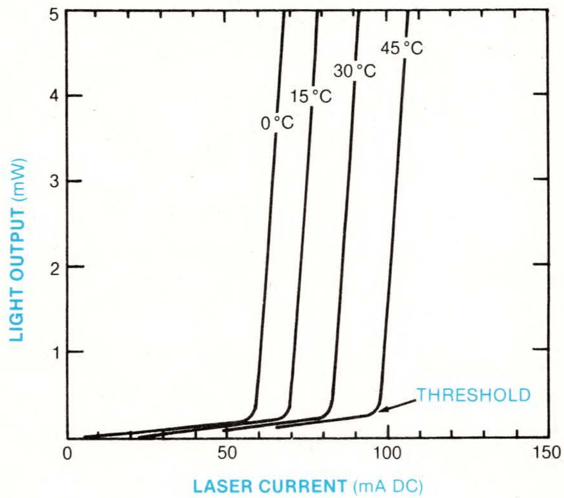

Fig B—A semiconductor laser's performance curves *illustrate the device's threshold effect. At currents exceeding threshold, the device lases. Below threshold, it emits incoherent light similar to that of an LED.*

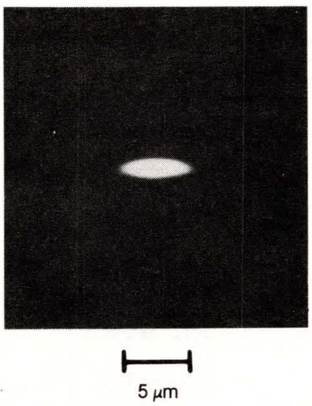

Fig C—A microscope focused on a laser's output facet *captures the light beam's transverse mode pattern.*

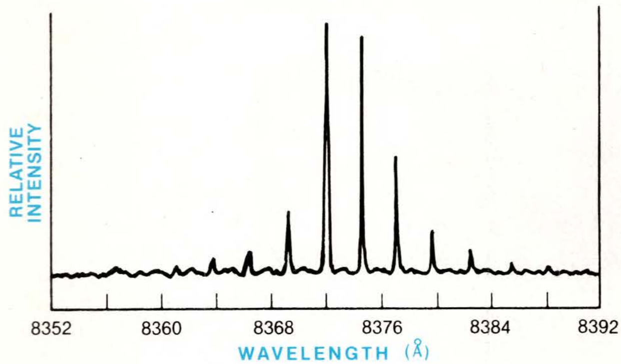

Fig D—A laser light beam's optical spectrum *represents its longitudinal mode pattern.*

Longitudinal modes, on the other hand, describe the light beam's spectral characteristics. A single-longitudinal-mode laser produces a light beam with a single predominant light frequency. **Fig D** graphs the longitudinal mode pattern or spectrum of a typical multiple-longitudinal-mode laser.

Almost universally, cw lasers exhibit a single transverse mode but can have either single or multiple longitudinal modes. In contrast, pulsed lasers simultaneously exhibit both multiple transverse and multiple longitudinal modes—thus generally making them unsuitable for fiber-optic applications.

Note that pulsed lasers typically achieve very high optical peak-power outputs (to 90W). However, they can't sustain cw operation without suffering thermally induced damage because their threshold currents are too high.

CW lasers operate with up to 10-mW continuous optical output, but they can also operate in pulsed mode with higher peak output power, depending on the duty cycle.

The **table** summarizes these common laser types' general characteristics.

Technology Update

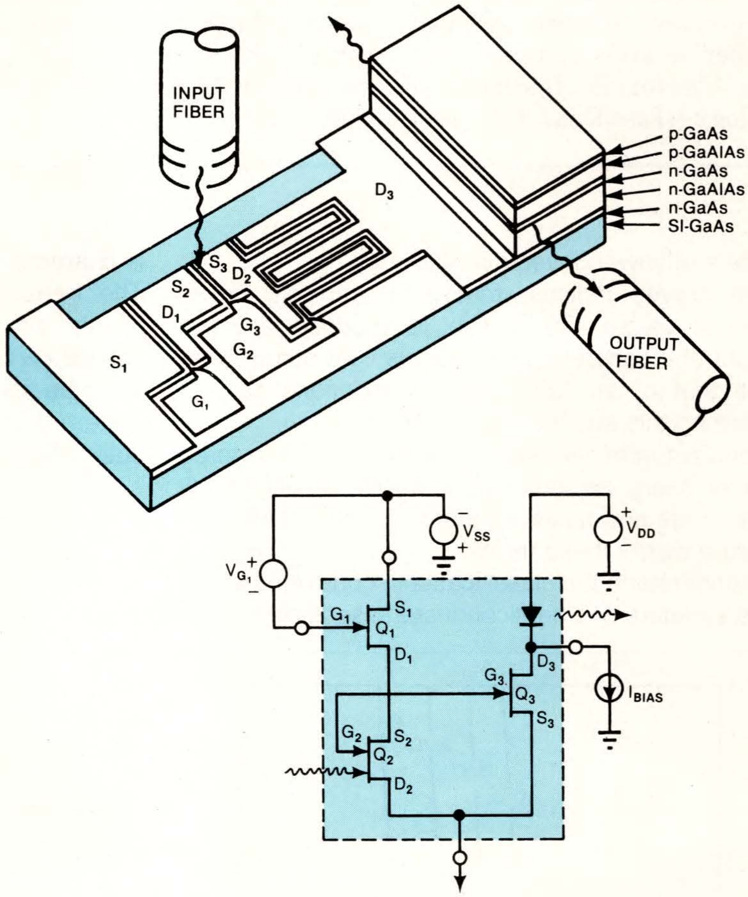

Fig 5—An entire optical repeater *integrated onto one substrate has resulted from work at the California Institute of Technology.*

laboratories around the country. Similarly, the Japanese government has reportedly funded a 5-yr, $20-million/yr cooperative development effort among several of that country's leading telecommunications firms. EDN

For more information...

For more information on semiconductor lasers such as those described in this article, contact the following manufacturers directly.

General Optronics
3005 Hadley Rd
South Plainfield, NJ 07080
(201) 753-6700

Hitachi America Ltd
1800 Bering Dr
San Jose, CA 95112
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ITT Components Group
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Semiconductor Div
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NEC/California Eastern Laboratories Inc
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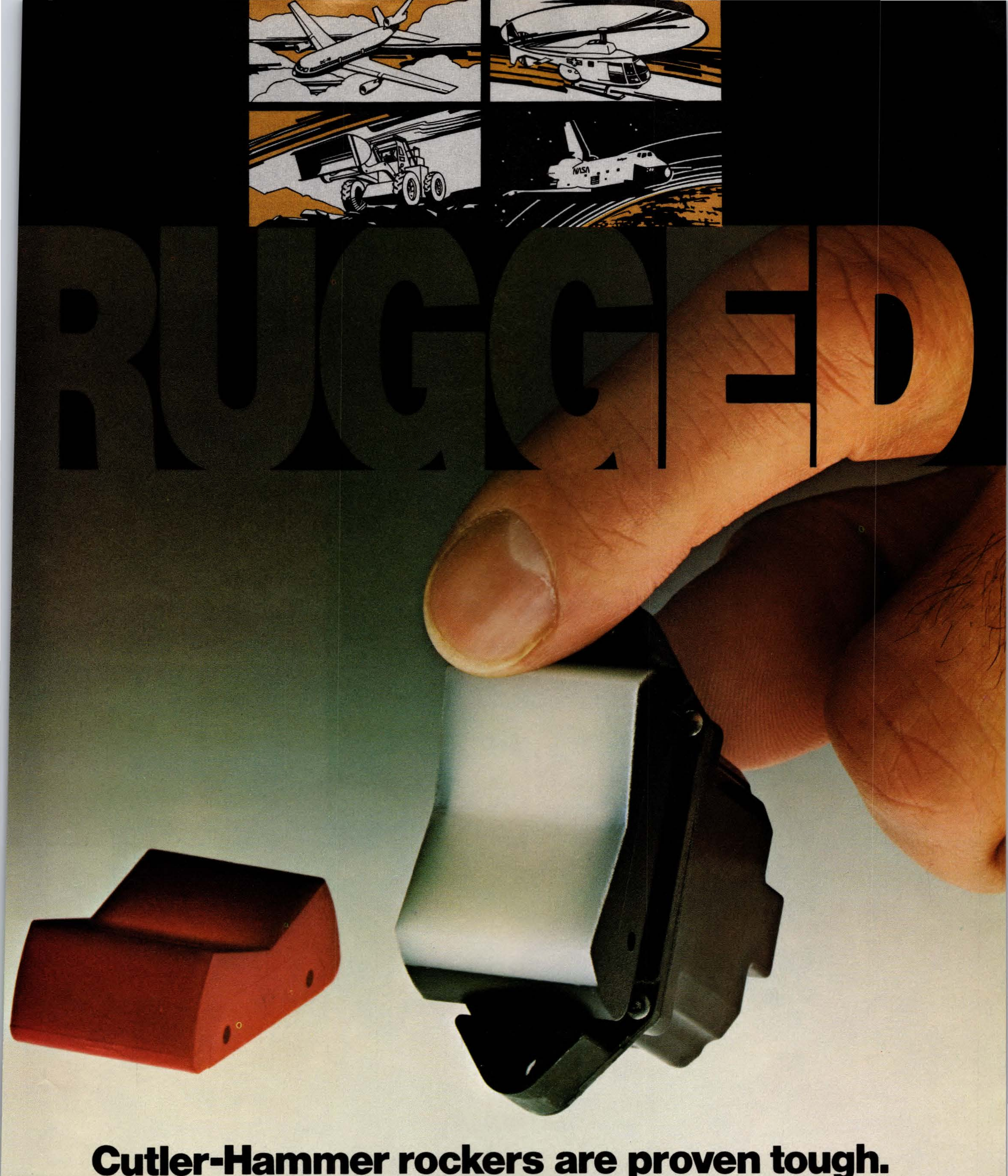
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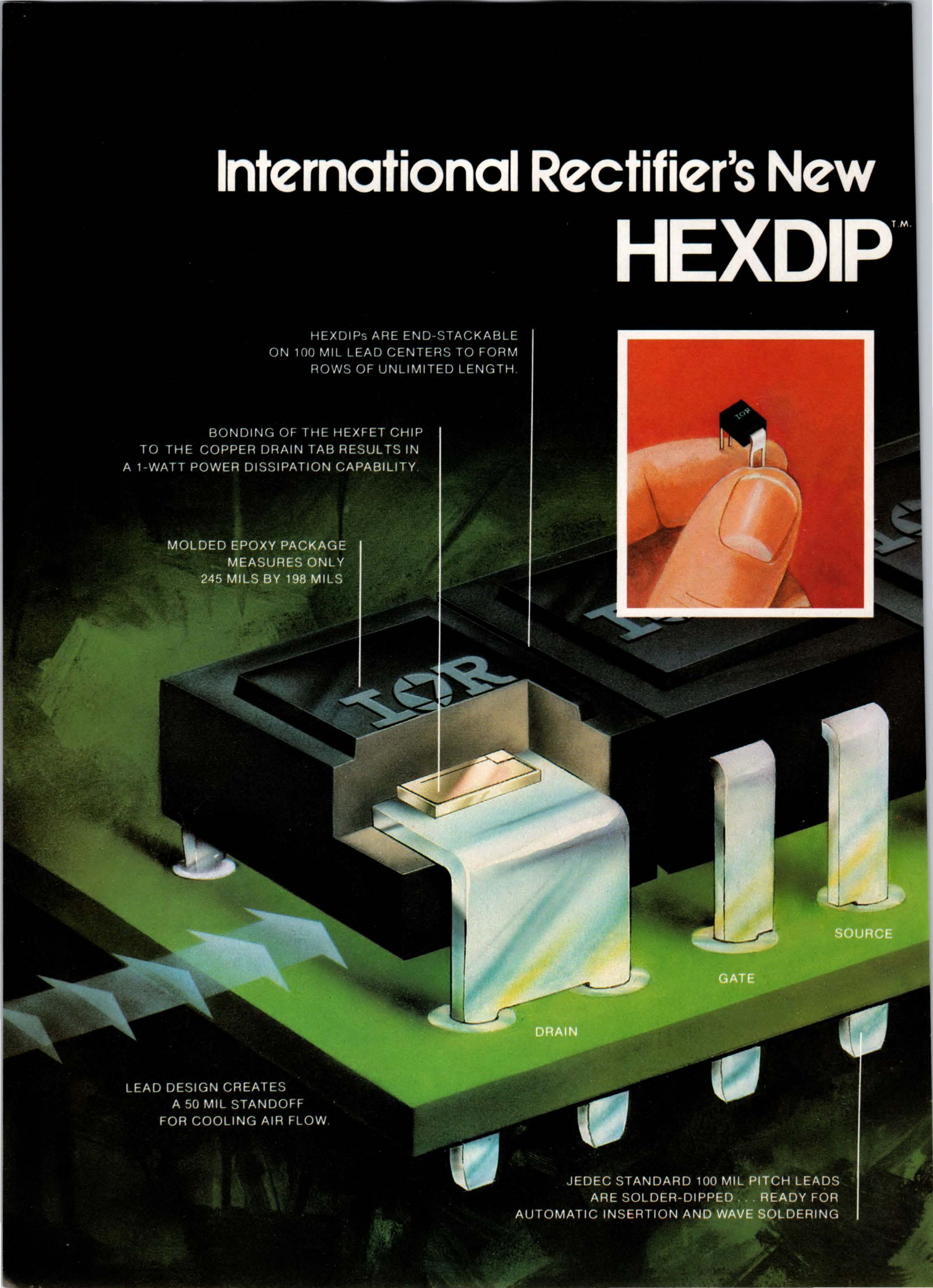
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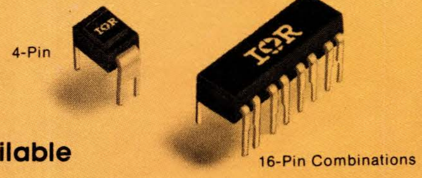

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	IRFD112	100V	0.8Ω	0.8A
	IRFD113	60V	0.8Ω	0.8A
P CHANNEL	IRFD9120	-100V	0.6Ω	-1.0A
	IRFD9121	-60V	0.6Ω	-1.0A
	IRFD9122	-100V	0.8Ω	-0.8A
	IRFD9123	-60V	0.8Ω	-0.8A

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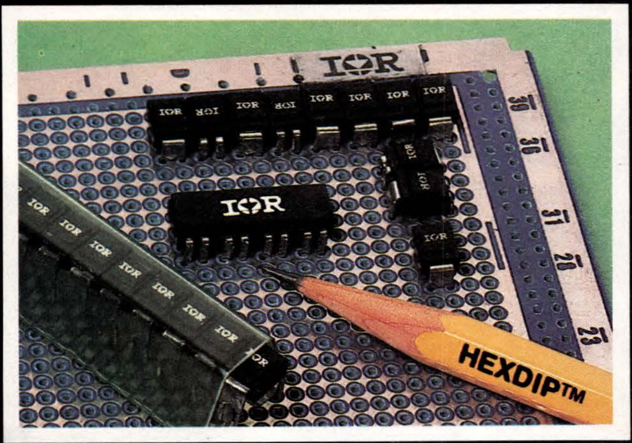
	IRFE111	FOUR IRFD111 4-PIN HEXDIPs
	IRFE112	FOUR IRED112 4-PIN HEXDIPs
	IRFE113	FOUR IRFD113 4-PIN HEXDIPs
P CHANNEL	IRFE9120	FOUR IRFD9120 4-PIN HEXDIPs
	IRFE9121	FOUR IRFD9121 4-PIN HEXDIPs
	IRFE9122	FOUR IRFD9122 4-PIN HEXDIPs
	IRFE9123	FOUR IRFD9123 4-PIN HEXDIPs
N AND P CHANNEL COMPLEMENTARY PAIRS	IRFE5110	TWO IRFD110 / TWO IRFD9120
	IRFE5111	TWO IRFD111 / TWO IRFD9121
	IRFE5112	TWO IRFD112 / TWO IRFD9122
	IRFE5113	TWO IRFD113 / TWO IRFD9123



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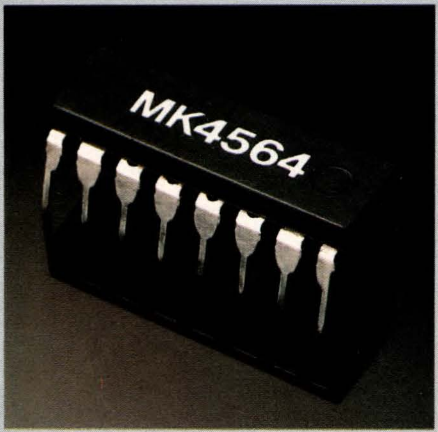

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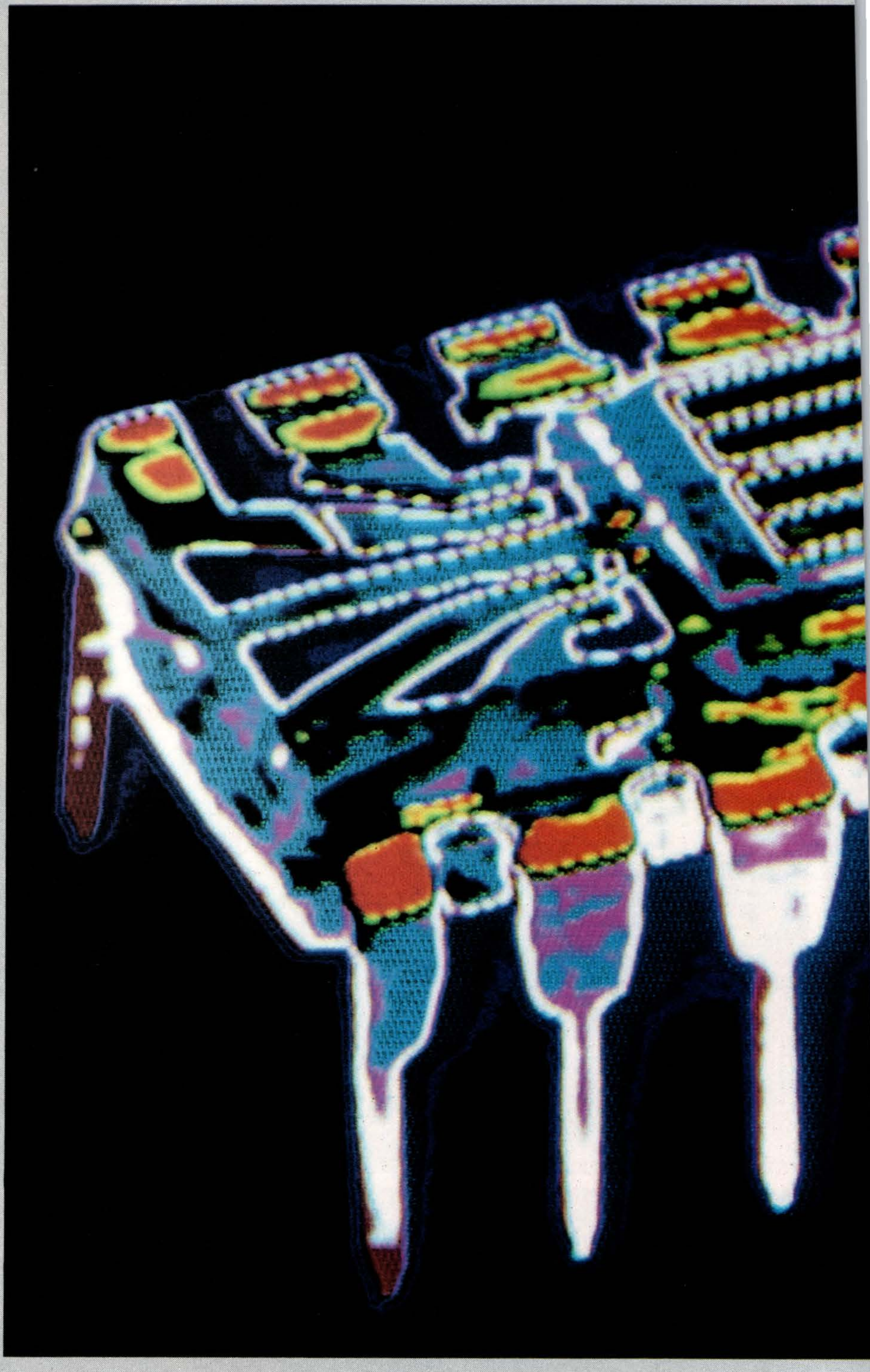

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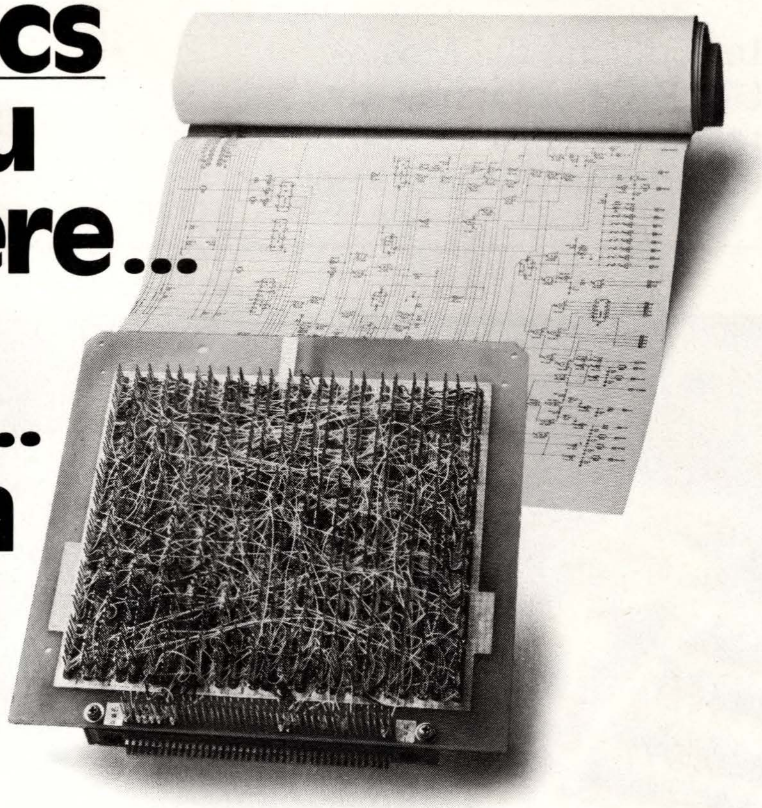

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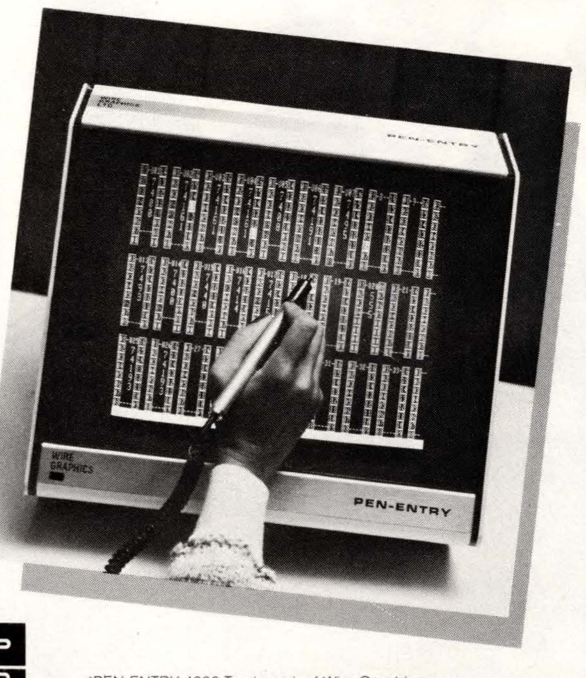

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CIRCLE NO 28

Ranging from simple to sophisticated, CAD/CAM systems increase productivity

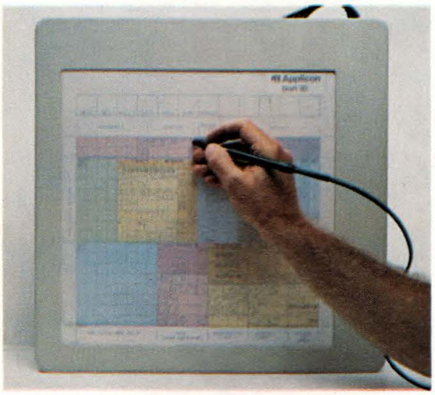
Leonard Marks

Computer-aided design/computer-aided manufacturing (CAD/CAM) systems and techniques are appearing in almost every area of electronic design, hardware fabrication and testing. The major reason for the explosive proliferation of this technology is the opportunity it affords to increase design and manufacturing productivity.

Most CAD systems available today provide engineers with the tools to solve highly complex design problems in a time- and cost-effective way. These systems combine the power of today's computers to perform real-time processing of large amounts of graphics data, the ability to store and retrieve that data instantaneously and the facility to easily display and interact with the data at an on-line graphics terminal. The result? Designers can create, simulate, optimize and document a broad variety of hardware designs.

Equally important to electronic-hardware manufacturers is the potential for directly using design data from CAD systems to drive automatic manufacturing and test equipment. Although the fully automated factory is still not totally feasible, many farsighted manufacturers have put elements of such a system in place in the form of numerical-control (N/C) assembly and test equipment interfaced to minicomputers and μCs. Invariably, companies that drive their automated equipment with outputs from a CAD system have determined that while fabrication costs decrease, the quality of the produced items increases.

CAD/CAM systems, however, really demonstrate their strength when used to implement design changes. Even a minor modification to a complex, manually prepared production assembly usually requires many weeks of work to change layout drawings, production documentation, tooling drawings, stock lists and manufacturing instructions, among other things. In contrast, data for a design previously captured on a CAD/CAM system can quickly be retrieved from archival memory, displayed and modified on a graphics terminal.

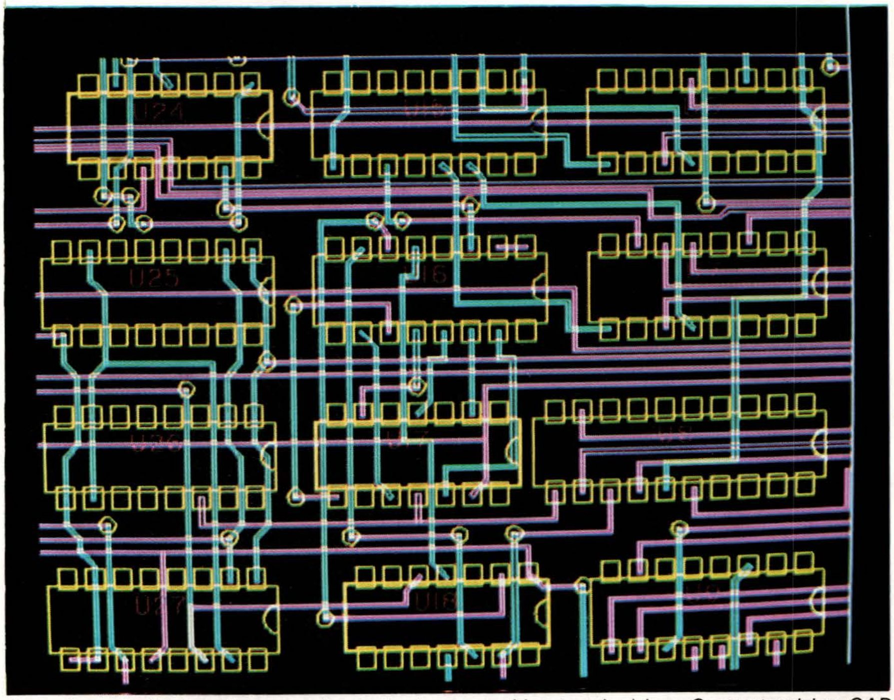


A CAD operator can use a tablet *in conjunction with a graphics terminal to manipulate data on a CRT. When the operator points a hand-held wand to one of the printed overlay's commands, the Applicon system's operating software executes a specific action. Different overlays can serve with the same tablet.*

Designers can then use the new data to revise all associated files containing documentation and manufacturing information. A relatively simple change can usually be completed this way in a matter of days.

Turnkey systems lower risk

Many choices are available to designers wishing to use CAD/CAM technology. You might want to take a low-risk approach by selecting an



A pc layout *displayed on a color raster-type graphics terminal in a Computervision CAD system illustrates color displays' ability to differentiate among pc traces on various board layers.*

Leonard Marks is managing editor of *Electronic Packaging and Production* magazine.

off-the-shelf turnkey system, for example—an alternative that offers uninitiated users the ability to enter the CAD/CAM arena by procuring a highly supported set of hardware and software, with predefined and demonstrable capabilities, from one vendor.

If you're more experienced, you might decide to build custom-designed CAD/CAM facilities, selecting from a host of computers, applications-software programs and peripheral equipment available from many different vendors. But

Accommodating a choice of color or monochrome displays, *Applicon Inc's Video Hybrid System also supports a full range of plotters.*

taking this approach requires integrating and interfacing all the pieces into a total system. And you also face the possibility of a lack of cohesive software and equipment support, plus the risk that the system won't meet performance requirements. However, if implemented properly, such a system will more closely meet your particular needs.

A sometimes confusing variety of options lie between these two extremes. For example, you can purchase small, special-purpose turnkey systems from different vendors and interface them together to form a larger, more general-purpose CAD/CAM facility. Alternatively, you can perform design functions through a remote-computer time-sharing service and input the resulting data to CAM equipment. Additionally, some companies provide CAD design services, convert manual designs to machine-readable language and perform many other related functions.

Turnkey systems

If you're in the market for a turnkey CAD system, you have a broad range of very mature or relatively new systems from which to choose. For example, Computervision Corp recently announced some major enhancements to its Designer V system, including a raster-type terminal capable of displaying as many as 64 colors. This feature aids operators who must discriminate among complex entities on different levels displayed concurrently at a workstation.

Another improvement to the Designer V's man/machine interface is the addition of a dynamic-menuing feature, which prompts an operator through a sequence of design functions. Once you select a command, the system displays a new series of command options on a screen, allowing quick movement from one set of operations to another without taking attention away from the display.

In the area of design applications, Computervision offers software enhancements for automatic placement of components and routing of interconnections on pc boards. The placement routines optimize gate and pin assignment to various ICs, handle different package sizes and allow preassigned and preplaced gates and components on both digital and analog circuitry.

In Graphics Editing mode, the system permits a pc designer to interactively move components to their optimum locations using a raster terminal that dynamically displays connectivity through a "rubberbanding" feature. (Rubberbanding is a software capability that continuously shows interconnections on a CRT between the parts being moved and the rest of the circuitry displayed.)

Another new feature provides the Designer V's users with the ability to lay out complex gate-array-IC chips. Embedded in this software is an automatic router that you can use to interconnect large arrays of standard circuit cells. The output

Color raster-type graphics terminals *such as Lexidata's (left) are typical of the large, high-resolution displays available for CAD/CAM applications.*

from this process can help create the masks needed to fabricate IC devices.

Hybrid-circuit aid

Another major supplier of multipurpose turnkey CAD systems, Applicon Inc offers the Video Hybrid System. This interactive graphics-based facility allows designers to automate design, checking and documentation functions and output the manufacturing data needed to produce hybrid circuits.

According to Dave Miller, an Applicon marketing manager, the system could help users achieve productivity levels 10 times greater than possible with manual operations. Claims Miller: "Hybrid circuit designs are steadily becoming denser and more complex and will soon defy traditional manual design and manufacturing techniques. New CAD/CAM products such as the Video Hybrid System will provide electronics companies with increased productivity and efficiency and enable them to get new product designs to market quickly to maintain that competitive edge."

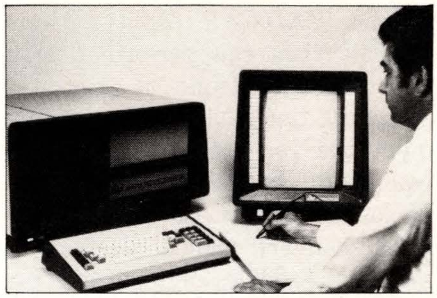
Based on Applicon's multiactivity IMAGE operating-software concept, the system features a choice of color or monochrome video-display terminals and a full range of peripheral plotters, including flatbed, drum-pen and high-speed electrostatic units. It can also serve in electromechanical packaging design and pc-board and IC-layout applications.

Much of Applicon's ongoing development efforts appear to center on improving user interfaces, as evidenced by a color-assisted symbolic layout (CASL) feature available as part of its Super VLSI Graphics System. CASL allows a chip designer to display simplified symbolic representations of complex circuit cells on a color graphics terminal. During layout of a chip that might contain as many as 100k transistors, using symbolic representations permits more rapid display of graphics data and requires less storage space, resulting in better system response and therefore in higher productivity.

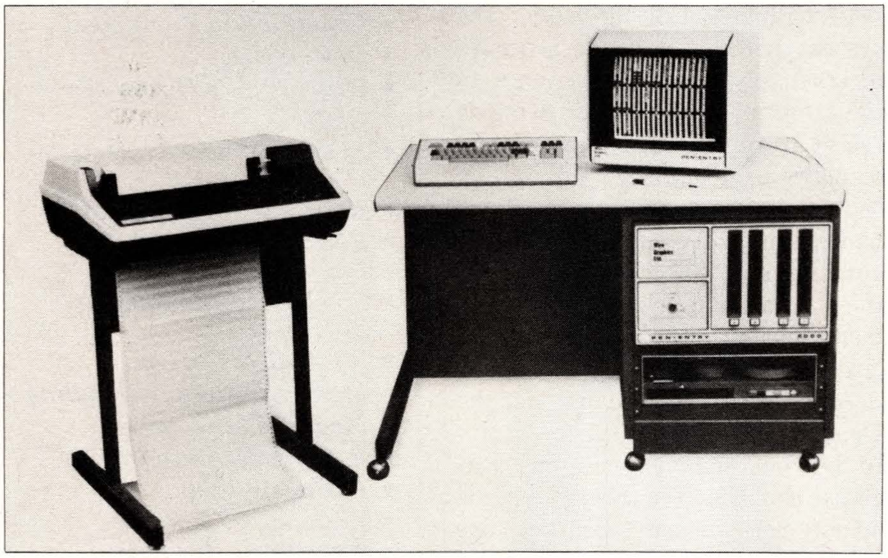
Voice-control graphics

Another manufacturer, Calma, markets an improved version of its interactive graphics-based system, the GDSII. This system incorporates both high-resolution black-and-white and color terminals.

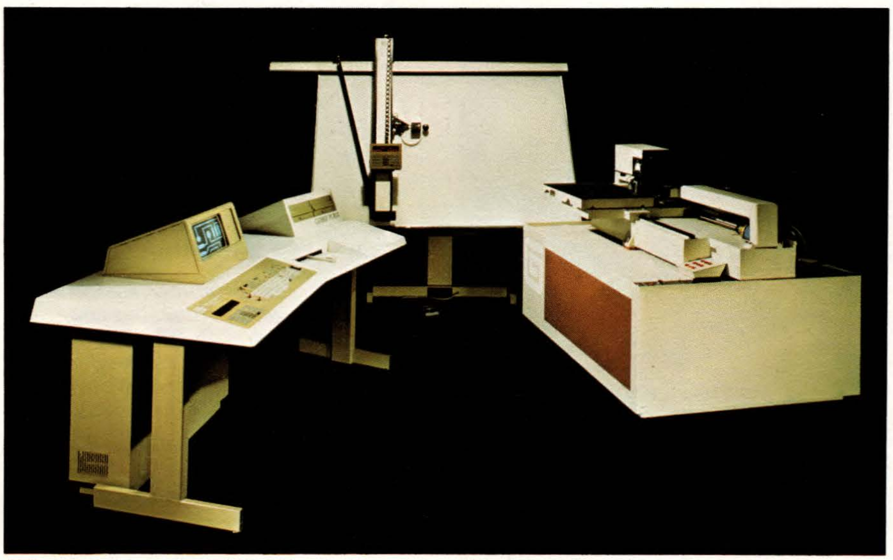
Used for pc-board layout, the GDSII can access more than 4000



Compatible with all major computer-graphics and analysis systems, *the stand-alone IC Designer from Avera Corp permits customized, in-house IC mask design and schematic entry. The basic system costs $39,250; options include an 11×11-in. tablet input device, a magnetic-tape drive, a hard-copy unit and a 10M-byte Winchester-type disk drive.*



Automated preparation of data *for wire-wrapping or wire-termination equipment is the hallmark of the Pen-Entry family of low-cost CAD systems from Wire Graphics Ltd. The family includes the 2000, 4000 and the newest 8000. A complete Pen-Entry 4000 consisting of an interactive graphics CRT, light pen, 64k-byte µC, keyboard, floppy-disk drive, paper-tape punch and printer costs $25,990.*



Priced at less than $95,000, *Gerber Scientific's PC-800 is designed exclusively for the production of pc artwork. It includes a console unit with keyboard, raster display, floppy-disk drives, a precision digitizer and a high-resolution artwork photoplotter.*

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CIRCLE NO 32

colors and features 512×640-pixel resolution, a 300M-byte disk drive, multiple library support, an alphanumeric display for monitoring inputs and system responses, and a command-menu facility that allows you to custom-tailor commands. The system's application program incorporates automatic circuit-function and parts-placement software and an automatic router.

Calma's most unusual enhancement, though, involves the addition of a voice-control unit to the GDSII. With this feature, operators can vocally initiate all system commands without the use of keyboard, pen or menu.

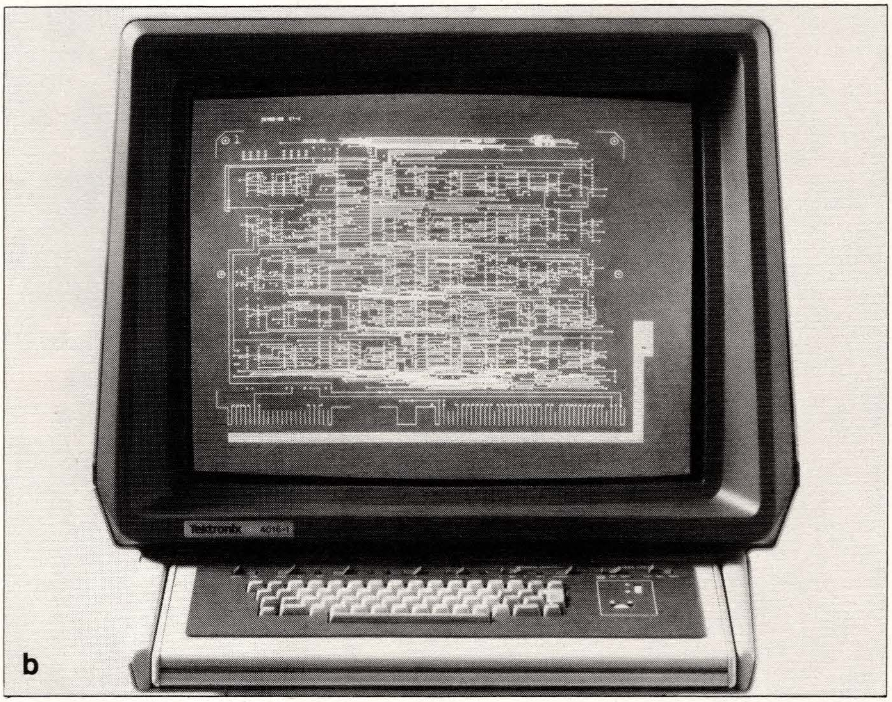
System use expands

Enhancements such as voice control, improved user/system interfaces, the addition of color to graphics terminals and faster response times are only some of the CAD/CAM trends evident today. Less obvious but no less important are moves by some turnkey-system suppliers to expand their products into large, multifunction engineering-design facilities, capable of concurrently attacking a wide variety of technical assignments.

This concept is exemplified by some of the new CAD/CAM capabilitites offered by Auto-trol Technology Corp, which has incorporated an optional 32-bit VAX-11/780 into its system. The power of this high-end minicomputer makes it practical to support a large number of users performing complex design tasks on one system.

Auto-trol also tackles the problem of geographic dispersion of engineering functions within a company with a telecommunications capability for remote operation of graphics terminals. Its CC-80 workstations can communicate with a remote central host processor at data rates to 32k bps, using commercial communications facilities.

Another trend gathering momentum is the emergence of small, special-purpose turnkey CAD/CAM systems, as typified by Gerber Scientific's PC-800. Designed exclusively for the production of printed-circuit artwork, it consists of a large-area digitizer, an interactive edit/verification station with raster display and keyboard, floppy-disk drives and a high-resolution photoplotter for 1:1 artwork generation.



Configure your own CAD/CAM system *with components such as Hewlett-Packard's HP7580A pen plotter* ***(a)*** *and a storage CRT from Tektronix* ***(b).***

Gould doubles design output with PC-800.

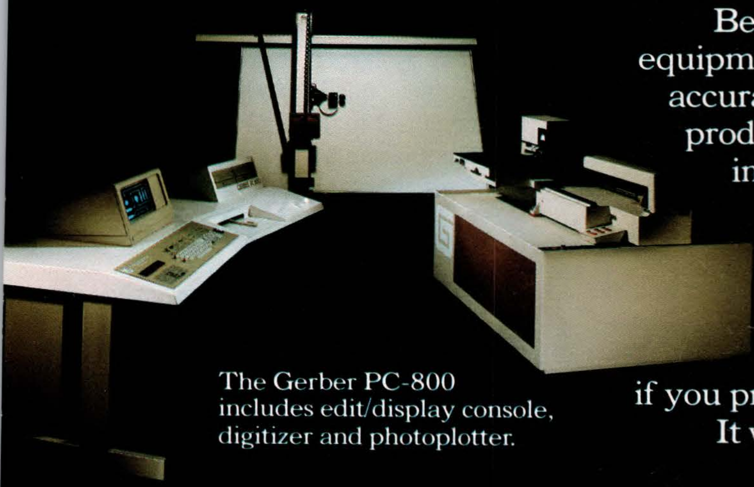
The Gerber PC-800 CAD system is helping the Modicon Division of Gould Inc. stay ahead of the competition in the rapidly evolving field of programmable controllers.

How? By cutting PCB artwork production time in half. And by freeing designers from laborious hand taping. The result: Gould is able to generate twice as many designs in the same amount of time.

Because Gould uses automatic insertion equipment to meet its high volume demands, accuracy is critical. With PC-800, Gould produces 1:1 master artwork with accuracy impossible to achieve by hand taping. And with perfect registration.

PC-800. It's the proven CAD system that cuts turnaround, boosts productivity and improves board manufacturability. And you can justify it even if you produce as few as 10 PC designs a year.

It works for Gould. And it can work for you.



The Gerber PC-800 includes edit/display console, digitizer and photoplotter.

Gerber PC-800
The CAD success story of the year.

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CIRCLE NO 33

Technology

Priced at less than \$95,000, PC-800 suits installation in small electronics companies and pc service bureaus. Gerber estimates that 90% of the thousands of companies designing pc boards are still hand-taping artwork, and low-cost CAD systems will fill an obvious need to automate those operations.

A similar system is available from Nicolet CAD. It offers four equipment configurations, ranging from an 11-in. black-and-white storage-tube graphics terminal and a pen plotter driven by an 8-bit μP to the System 81, which uses a 19-in. high-resolution color graphics terminal with 1000×1000 addressable pixels.

The system incorporates an LSI-11/23 μC, 1½M bytes of memory, a 36×48-in. tablet, a built-in modem for remote diagnostics and the firm's top-of-the-line Zeta high-speed drum plotter. All versions contain floppy-disk drives for data storage; the System 81 accepts a 30M-byte hard disk.

The System 81 also accepts some novel options, such as a video-camera tracing attachment that can display rough layout sketches on the CRT screen, allowing an operator to directly capture a design at the graphics terminal. Nicolet claims that with this feature, a designer no longer need prepare a precise layout. Furthermore, thanks to the elimination of the normally tedious digitizing operation, data-capture errors are reduced, increasing productivity.

Nicolet also offers a variety of application and post-processing software packages, including pc layout, schematic drafting, hybrid-circuit layout, mechanical design and drafting, and photoplotter and N/C-drill outputs.

The System 81 costs \$98,200; look for Nicolet to introduce a black-and-white version this summer.

Extensive menus

Another entry in the pc-design field, the AutoMate 80, is produced by AutoMate (formerly Markrevel

Price breakthrough: $499.

For a CMOS microprocessor development system.

Our new CDP18S693 costs less than any other 1802 microprocessor development system on the market. And the development system can even become your final target system.

The incredibly low $499* price includes:

- CDP18S601 computer Microboard.
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Develop software for any 1802-based component design, or for any Microboard system in BASIC or assembly language.

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Or contact RCA Solid State headquarters in Somerville, N.J. Brussels, Belgium. Sao Paulo, Brazil. Hong Kong.

Or call Microsystems Marketing toll-free (800) 526-3862.

* U.S. optional distributor resale, single unit price.

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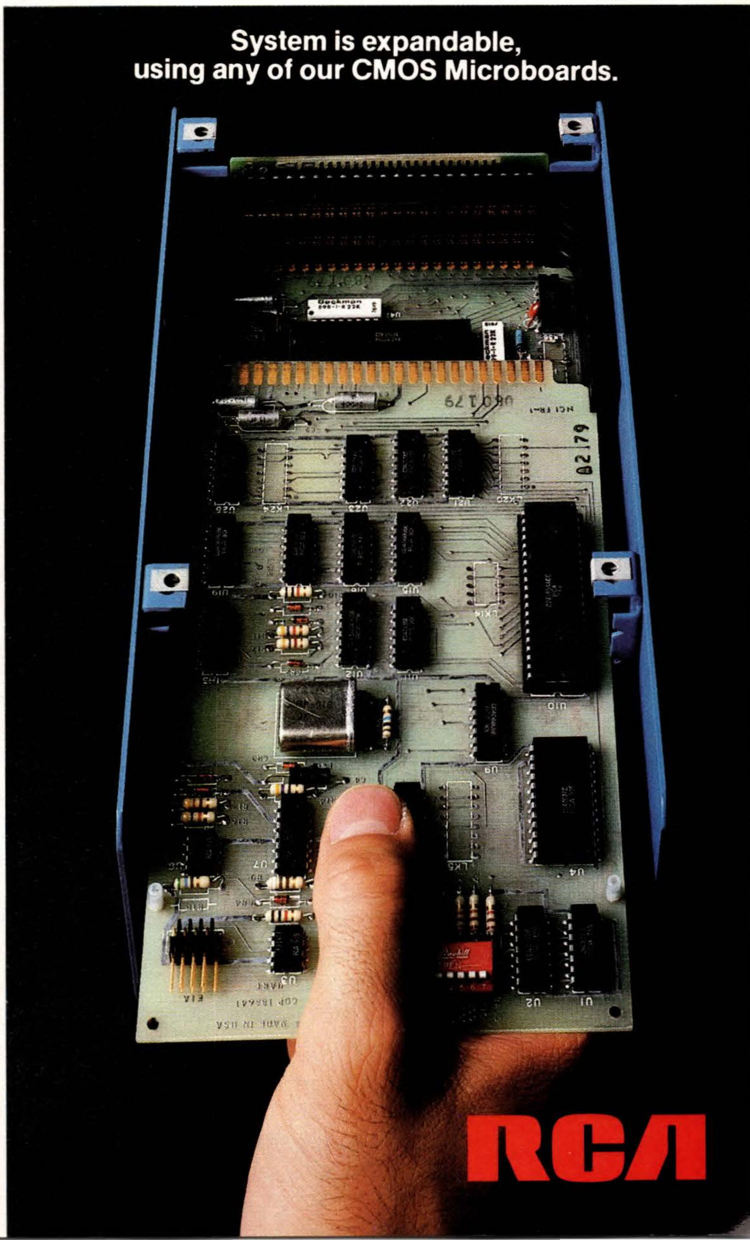
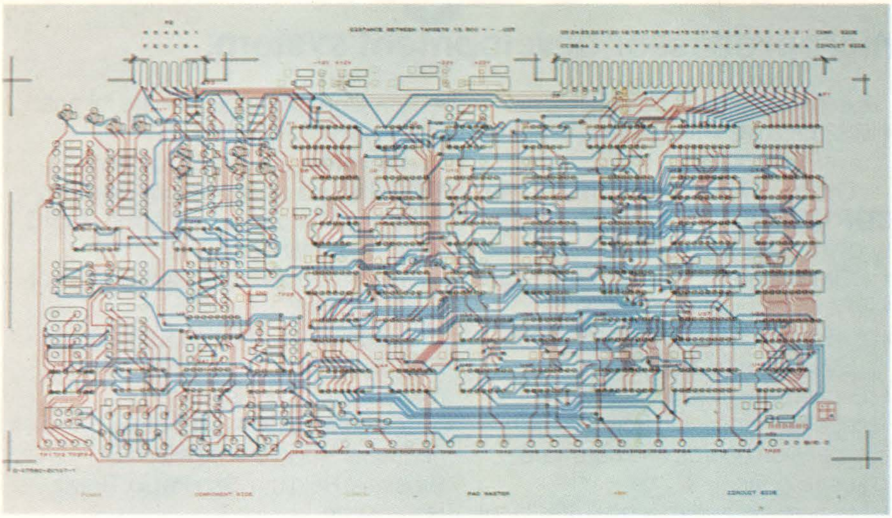


Another reason to switch to CMOS.

RCA



Through software control, *HP's HP7580A pen plotter produces multicolored plots of pc layouts. It can display various circuit features on a single sheet.*

Systems Group) and features a Data General 16-bit minicomputer that supports two color graphics terminals, a digitizer, a multicolor pen plotter and an array of applications software. This software includes a schematic-capture program, logic-circuit diagnostics and automatic-placement and routing routines with on-line design-rule checking.

An extensive menu-command set permits selective graphics editing of all design data. The schematic-capture software can serve in digitizing ungridded, freehand-sketch schematics to provide a net-list and parts-list data file to the layout software, as well as producing a final plotted and back-annotated schematic drawing. The firm claims to have also used AutoMate 80 for layout of thick-film hybrids and gate-array ICs.

Another pc-design system is Redac's Cadet. Priced at slightly less than $50,000, this desktop system features a μP-based raster-type CRT terminal and a keyboard and tablet for command entry and graphics-data manipulation. Using a comprehensive menu of commands, you can enter design data, place components and route interconnections interactively at the CRT, and perform layout-rule checks.

A completed design gets stored in a built-in magnetic-tape cartridge recorder. You then send the cartridge to a Redac design service center, which provides 24-hr turnaround on 1:1 master artwork, silkscreen and solder-resist artwork, assembly drawings, N/C-drill tapes and component-insertion tapes.

In the area of large, special-purpose CAD/CAM facilities is McDonnell Douglas's (McAuto) Unigraphics System. This multiterminal system serves primarily for mechanical design, drafting and creation of N/C machining data. Software capabilities include graphical generation of 2- and 3-dimensional data, mechanical analysis, generation and display of multiaxis cutter-tool paths and sophisticated data-file-management routines.

Application programs

If you want to develop your own CAD/CAM system by integrating available equipment and applications programs, you now have access to a variety of special-purpose software. Examples include SCI-CARDS, a pc-layout system licensed by Scientific Calculations Inc; AD-2000, a program for mechanical design and drafting marketed by Manufacturing & Consulting Services Inc (MCS); and GAELIC, an IC-layout system licensed by Compeda Inc. Each package can perform a total design

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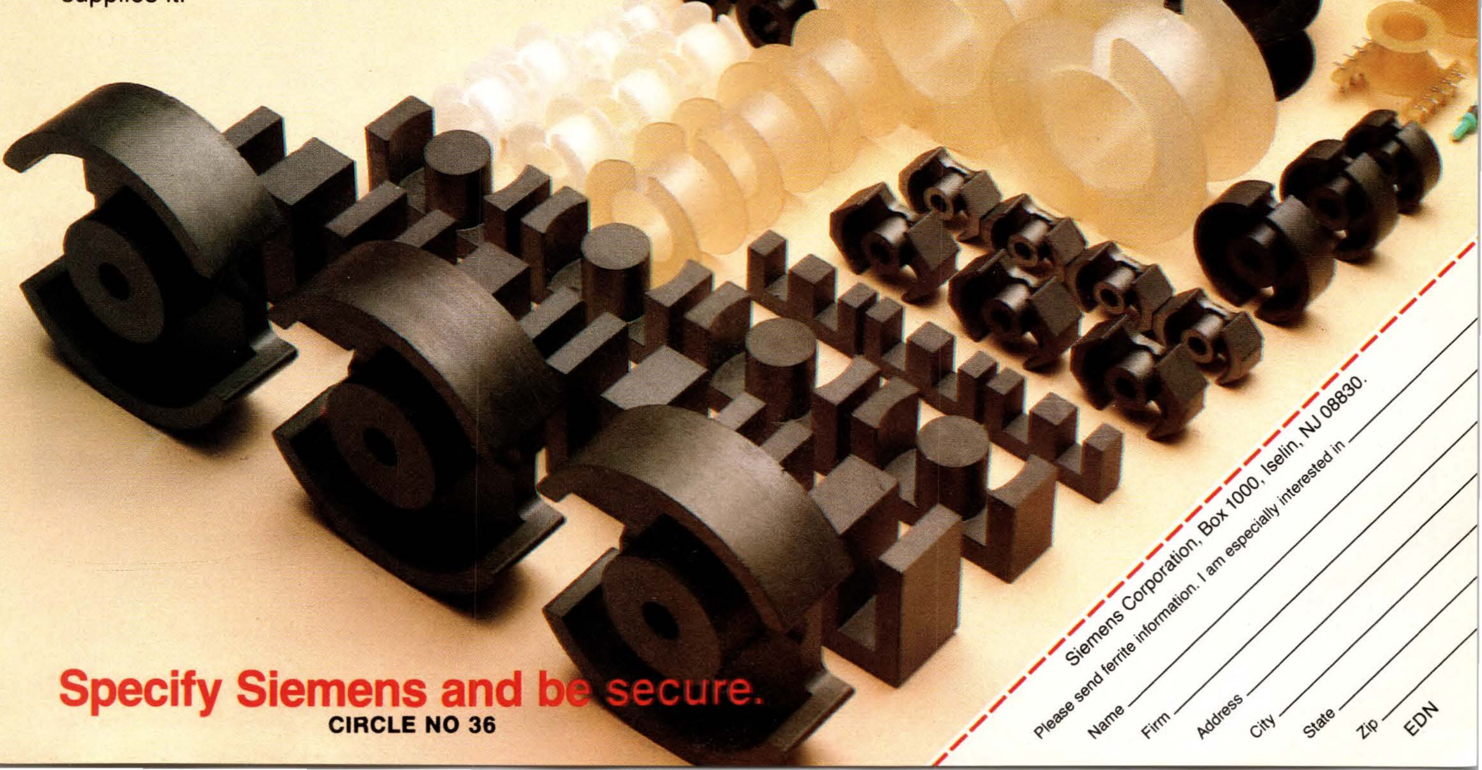

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and documentation job within its individual area of technology.

Licensees of these programs get ongoing software support, and all vendors are dedicating significant amounts of internal resources to system enhancement and the addition of new capabilities.

For instance, Scientific Calculations has introduced new software for automated generation of schematic drawings conforming to ANSI, MIL-STD-806B or a user's own design standards. This feature interfaces directly with the SCI-CARDS interactive graphics-based pc autoplace and routing software, providing interconnection and parts data to that program. SCI-CARDS runs on DEC's VAX-11/780 or Prime Computer's P650 or P750, with either machine supporting as many as four refresh-type graphics terminals.

AD-2000, a mechanical-analysis, design and drafting program, supports interactive graphics operations on both refresh- and storage-tube displays. Written in ANSI FORTRAN, it installs in virtually any computer of the proper size, including CDC, DEC, Honeywell, IBM, Modcomp, Prime and Xerox machines. It includes a broad range of capabilities relating to geometric-construction manipulation, plus generation of data for a variety of N/C machine tools and plotters. MCS will market a turnkey system containing the AD-2000 software in addition to leasing the program.

For on-line design of VLSI circuits, Compeda's GAELIC program allows multiterminal operation on mainframes or 32-bit minicomputers. GAELIC consists of several modules operating on a common database, including an interactive graphics editor, logic simulator and automatic layout and design-rule checker, as well as interfaces to plotters, pattern generators, digitizers and turnkey graphics systems such as Applicon's or Calma's.

Compeda also offers a menu-driven, tablet-controlled editor in-

terfaced to both a color-graphics terminal and a command monitor, featuring extensive self-help software for easy operator training and use. And the firm's drafting program, DRAGON, runs on the same equipment as GAELIC and can produce a wide range of 2-dimensional engineering drawings in any size or format.

Future looks bright

Extensive developments in the CAD/CAM industry have produced only optimistic forecasts from market researchers (EDN, June 5, 1980, pg 272). Even so, manufacturers and users of CAD/CAM systems believe that many new capabilities must appear before users can realize the technology's full potential. These features should include:

- Further reduction of equipment costs and improvements in performance
- Faster, more powerful CPUs containing more memory
- Improved communication facilities, allowing greater use of networking and remote distributed-processing techniques
- Greater emphasis on database-management systems
- More sophisticated application software with increased analysis and simulation capabilities
- Simpler, more flexible command languages
- Better man/machine interfaces and increased "user-friendliness"
- Greater terminal - resident intelligence
- A uniform graphics language facilitating data interchange among systems
- Improved handshaking with automated manufacturing and test systems
- Broader use of color raster-type graphics terminals having larger screens and greater resolution
- More extensive use of voice recognition for command-data input
- Utilization of pattern-recognition techniques to automate data capture. **EDN**

For more information...

For more information on the CAD/CAM systems and software described in this article, contact the following manufacturers directly.

Applicon Inc
32 Second Ave
Burlington, MA 01803
(617) 272-7070

AutoMate
(Formerly Markrevel Systems Group)
285 Hamilton Ave
Suite 420
Palo Alto, CA 94301
(415) 321-7970

Auto-trol Technology Corp
12500 N Washington
Denver, CO 80233
(303) 452-4919

Avera Corp
340 El Pueblo Dr
Scotts Valley, CA 95066
(408) 438-1401

Calma
527 Lakeside Dr
Sunnyvale, CA 94086
(408) 245-7522

Compeda Inc
2180 Sand Hill Rd
Suite 260
Menlo Park, CA 94025
(415) 854-2370

Computervision Corp
201 Burlington Rd
Bedford, MA 01730
(617) 275-1800

Gerber Scientific Instrument Co
83 Gerber Rd
South Windsor, CT 06074
(203) 644-1551

Hewlett-Packard Co
1507 Page Mill Rd
Palo Alto, CA 94304
Phone local office

Lexidata Corp
37 North Ave
Burlington, MA 01803
(617) 273-2700

Manufacturing and Consulting Services Inc
2960 South Daimler Ave
Santa Ana, CA 92705
(714) 540-3921

McDonnell Douglas (McAuto)
Box 516
St Louis, MO 63166
(314) 232-0232

Nicolet CAD Div
2450 Whitman Rd
Concord, CA 94518
(415) 827-1020

Redac
1 Redac Way
Littleton, MA 01460
(617) 486-3529

Scientific Calculations Inc
7635 Main St
Fishers, NY 14453
(716) 924-9303

Tektronix
Box 500
Beaverton, OR 97077
(503) 644-0161

Wire Graphics Ltd
215 B Central Ave
Farmingdale, NY 11735
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The Future Is Here And Now

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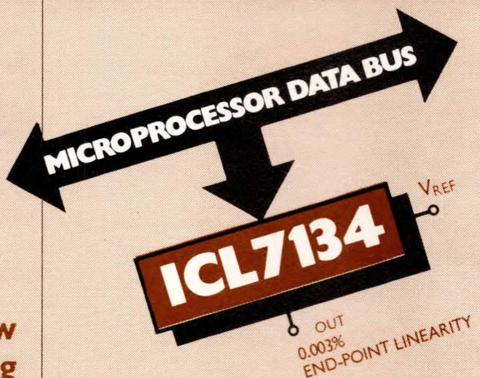
In this issue #7 of *Intersil Insight*, you'll read about a 14-bit D/A converter with ½ LSB linearity, the ICL7134. A single chip device that drives 8 alphanumeric LEDs, the ICM7243. And many others, designed for the future, in low-power CMOS.

Equally important is the fast-growing field of Power MOS devices—for instance, our 800V IVN6200.

Also in this issue are some down-to-earth application ideas, new ways to solve common problems, with lower component count.

For previous issues of *Intersil Insight*, check the You Got Me Coupon. Check #7-A for issue 6, or #7-B for issue 5.



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Intersil announces another brand new family of Power MOS—our IVN6200 series. These devices are available in either TO-3 (IVN6200KN series) or TO-220 (IVN6200CN series). And in four voltage/current versions:

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IVN6200KNP/CNP 250V, 9A, .5Ω
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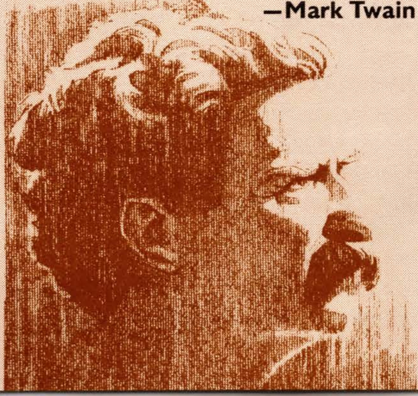
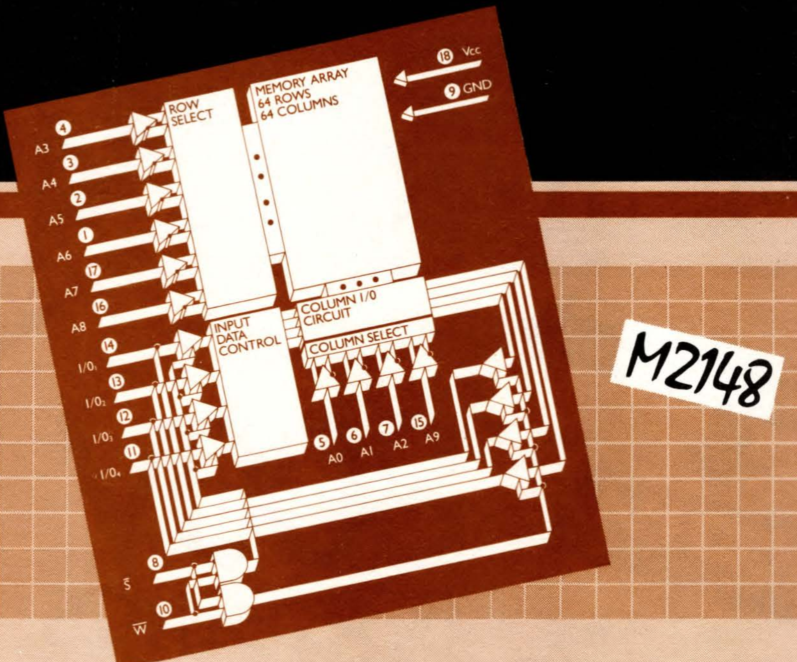
—Mark Twain





Military 2148 with 70ns Access

Now, the industry standard, high-speed 2148 static RAM is available for military—the M2148 from Intersil. Access times to 70ns guaranteed over the entire temperature operating range, −55°C to +125°C. Hi-rel processing to 883B Class B or your custom hi-rel requirements. Cerdip or flatpack. Our M2148 is pin-compatible with the 2114 and the commercial 2148 and has the same high speed, but meets the tolerances of extreme environments.

			Price each/100-up
M2148	**1K x 4**	**85ns**	**$26.09**
M2148-3	**4K x 1**	**70ns**	**32.25**

For the data sheet, check #7-E. And check Intersil for their complete Mil RAM family.

STD BUS CPU CARDS

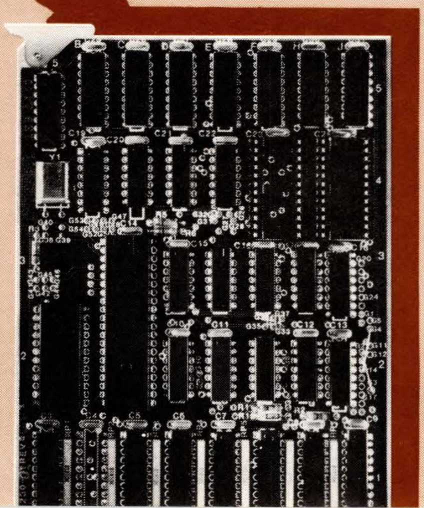
Intersil now offers new flexibility to Z80 and 8085 card users with its ISB-3100 and ISB-3110 cards—**fully STD BUS compatible**. Each has static RAM memory in 1K byte increments up to 4K and two 24-pin sockets for EPROM memory. Jumper selectable memory mapping for on-board RAMs and EPROMs. Can be mapped in 4K blocks anywhere in the 64K address field in 4K increments. Full memory decoding capability.

ISB-3100 (Z80 based) Central Processing card: either 4MHz or 2.5MHz clock frequencies. 4 interval timer/counter channels.

ISB-3110 (8085 based) CPU card: either 4MHz or 3MHz. 3 interval timer/counter channels.

Both are backed up by a full family of STD BUS compatible products from Intersil: from memory to I/O cards to peripheral controllers. Plus general-purpose operating systems for software development, on-line binary debugging monitor, and more. All available off the shelf with very competitive pricing.

Check #7-F for details on our ISB-3100 (Z80) or ISB-3110 (8085) cards.



SINGLE-CHIP 8 CHARACTER DRIVER

Another first! With a single chip, you can get direct interface between a μP and a 14/16 segment alphanumeric LED display. It's Intersil's new ICM7243. This unique device directly drives 8 characters (cascadable to 16, 24 or more)—without additional hardware.

Furthermore, external PROMs and ROMs are eliminated because the character generator is on board. The ICM7243 accepts and decodes the popular ASCII code. So you get a full range of 64 characters (.15" tall) for easy, direct communication between microprocessors and people, in words and number—and with only a single device.

For 16-segment characters, the ICM7243A; for 14 segments: the ICM7243B. Both are only $8.25 in 100-up. Check #7-G for the data sheet.

MICROPOWER VOLTAGE DETECTOR

Overvoltages/undervoltages—both can be detected, monitored and corrected by a single device, the ICL7665. Yet the part requires only micro-supply current—3.5μA (typical).

The undervoltage and overvoltage parts of the detector can be used alone, or together, though both use the same accurate internal bandgap reference (1.3V). Upper and lower trip levels are individually programmable, as well as programmable hysteresis levels.

The ICL7665 operates from a wide supply voltage (1.6 to 16V) and can sink a high output current—up to 20mA.

Indispensable for portable instruments, systems requiring low-current battery back-up, or instruments that require both HIGH and LOW voltage warning: ICL7665. Check #7-H.

OW-COST REMOTE DATA ACQUI-SITION SYSTEM

Move analog and digital data at mini-num cost with Intersil's new REMDACS II amily of remote data acquisition and ontrol system cards. Unique serial data protocol allows as many as 256 remote 16-analog channel cards to provide ready-o-use digitized data to your computer—all on a single low-cost twisted pair. With on-board signal conditioning and true 12-bit A/D conversion, superior data integrity is assured. Wide choice of analog input boards accept 16 4 to 20mA signals, 16 solid-state temperature sensors or 16 10mV full-scale voltages. And your choice of solid-state or mechanical relay cards for control applications. No special software is required. The on-board microprocessor supervises all data transfers, making the system transparent to your computer. You can add or relocate remote cards at any time. Just clip them onto the serial data bus.

The REMDACS II family includes over 20 analog, digital I/O and computer interface cards, which are easily configured using our "motherboard" concept.

REMDACS II brings you higher quality data at the lowest cost possible—pays for itself in reduced installation cost alone! For complete details, circle #7-I.

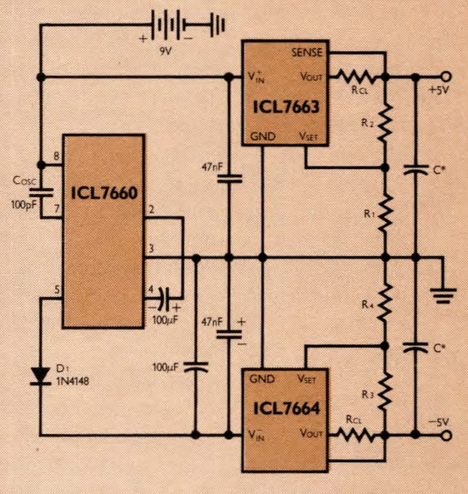
T E C H - T I P S

Our application engineers kick off this new INSIGHT feature by digging into their library of design hints and tips, accumulated as they field questions about the best way to use Intersil products. Some hints are simple. Some are subtle. But we hope they'll help our readers in their circuit design efforts.

GENERATING REGULATED SPLIT SUPPLIES FROM A SINGLE SUPPLY.

Both in battery-powered and line-powered equipment, a single basic source of power is generally the lowest cost and most efficient solution. However, many systems require several different supply voltages for optimum operation. In many cases the current required is small, and the extra cost of more batteries or additional power supply outputs is disproportionate. Although in many systems the raw power available from batteries, or from converters such as the ICL7660, will be adequate, there are other cases where better regulation is required. Ideally, two requirements should be met by a series-pass regulator for highest efficiency. The minimum input-output voltage differential should be as low as possible, allowing the raw power to be delivered at the lowest possible input value (also maximizing battery life), and the quiescent supply current to the regulator should be a minimum.

The high efficiency ICL7660 Voltage Converter and the ICL7663/4 Voltage Regulators can be combined as shown to generate regulated positive and negative supplies from a single input. The clock frequency of the ICL7660 voltage converter is reduced to enhance the efficiency of its operation at low power levels even more. The circuit will squeeze the maximum possible life out of the battery. For more details, check # 7-J.



Lowest Error MUX's

New Intersil IH6116/IH6108 multiplexers are pin-for-pin replacements for the industry standard 16 and 8 channel MUX's you're probably using now. But, they offer the low power, low error performance of Intersil's latch-up proof CMOS process. They draw a maximum supply current of 0.2mA. And they consume only about 1/10 the power of their nearest competitor: 4.5mW Max., at ±15V. This means virtually no self-heating... leakage current of 0.2nA @ 25° doesn't change as the device "warms up." You get the lowest power consumption and lowest leakage in the business. Just check #7-K.

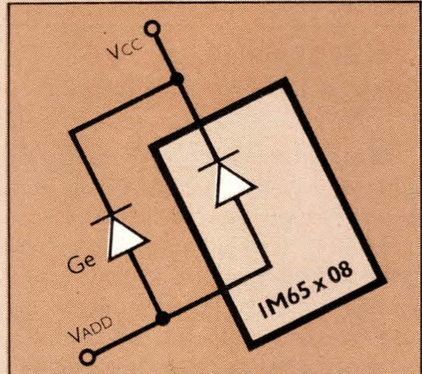
DESIGNER'S CORNER:

A Unique Answer to a Common Problem

In CMOS memories, SCR latchup is a common problem. It can cause system error from damage to the memory, excessive heat, a blown fuse or drained batteries. Here's a solution we found for one customer's problem.

We eliminated an overvoltage at input (due to a transient effect) by adding a germanium diode. This diode has a lower forward bias voltage than the internal protection diode. When turned on, it acts as a shunt for possible latchup triggering current. A typical bias value for the germanium diode is .2V.

This is just one solution. Our new app note #MO11, "Avoiding Problems in CMOS Memory Operation," has some other good ideas. More than that, it gives a detailed analysis of the problem so that



1K x 1 CMOS RAM

system engineers can formulate their own solutions. Individual constraints should make this necessary. Check #7-L for app note MO11. It's free.

INTERSIL

YOU GOT ME!

VOL. 7

For more information, just check the appropriate box, then clip and mail!

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Hot New Lit

Power MOS Application and Design Handbook

The latest information on Power MOS, the wave of the future. Includes newest app notes "Power MOS: Linear Applications" (A038), "Off-Line Switchmode Power Supply" (A037), and others. Plus data sheets, cross reference list, dice information, hi-rel process flow, technology description and selector guide. Check #7-M.

COMPLETE 1981 INTERSIL CATALOG

Usually $5., but with a "You Got Me" coupon from this *Insight* #7—only $3. Over 1200 pages of data sheets on all Intersil products: discretes, linear, digital; vertical power MOSFETS; analog switches and multiplexers; data acquisition; timers, counters, display drivers; consumer circuits. Also includes information on hi-rel processing, application note summary, and more. Check #7-N on the "You Got Me" coupon and send with your check for $3.

SUCCESSIVE APPROXIMATION REGISTERS

Use A-to-D or D-to-A converters? We now have the AM2502/3/4 registers which contain all the storage and digit control for successive approximation A to D converters. A low-power version, the AM25L02/3/4, is also available now from Intersil.

These 8- and 12-bit TTL successive approximation registers are pin-for-pin compatible with the industry standard AMD device. They have a provision for register extension or truncation, can be operated in START-STOP or continuous conversion mode, or can be used as serial-to-parallel counters. For full details, check #7-O. Competitive pricing.

Testing. One. Two. Three. Four.

Thanks to the wider selection of low frequency Philips oscilloscopes, you can buy all the performance you need—and not a penny's worth more.

Need a 25MHz single time base scope? Choose the PM3212.

A 25MHz with delayed time base? Choose the PM3214.

Need higher bandwidth and shorter rise time? Choose one of the new 35MHz scopes from Philips.

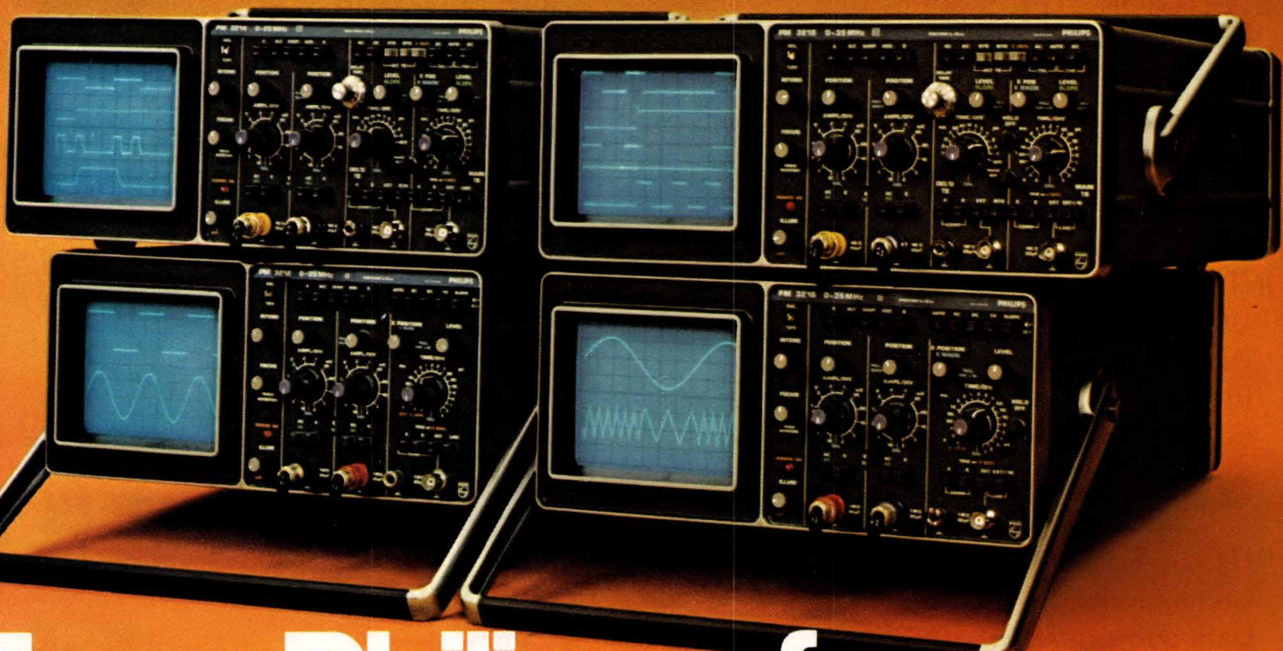
The PM3216 features single time base; the PM3218 has delayed time base. Both have a sweep speed of 10ns/div. and a variable hold-off facility to avoid double triggering on complex digital signals, making it unnecessary to use the time base in the uncalibrated mode.

All four oscilloscopes feature trigger selection from either channel, line, external source or composite triggering for asynchronous signals. The alternate time base displays of the PM3214 & 18 allow them to do the work of much more expensive instruments. Just press delayed time base and main time base simultaneously and both time base sweeps are displayed for one or both channels.

All four feature wide trigger bandwidth plus 10kV CRT for high light output and excellent resolution. Of course, they are strong, rugged and lightweight.

Now, more than ever, Philips wants to make *your* next scope. Philips plans to double sales by 1981. Much of this growth will come from our new U.S. manufacturing facilities. We have to offer you a better low frequency choice so you'll buy from us.

For more information call (514) 342-9180 in Montreal; (416) 789-7188 in Toronto; (613) 224-8374 in Ottawa; (604) 872-8106 in the West, or contact Philips Test & Measuring Instruments, Inc., 6 Leswyn Road, Toronto, Ontario, Canada M6A 1K2.



From Philips, of course.

PHILIPS **Test & Measuring Instruments**

PHILIPS

CIRCLE NO 43

Leadtime Index

ACTIVE COMPONENTS

PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
DISCRETE SEMICONDUCTORS			
Diode, switching	1	4	=
Diode, zener	2	8	=
Rectifier, low-power	1	4	=
Rectifier, power	1	4	=
Thyristor, low-power	1	4	=
Thyristor, power	4	8	=
Transistor, bipolar power	6	12	up
Transistor, bipolar signal	8	20	up
FET, power	4	11	=
FET, signal	4	12	=
Transistor, RF power	4	10	=
DISPLAYS			
Fluorescent	4	12	=
Gas-discharge	4	8	=
Incandescent	2	11	=
LED	2	8	=
Liquid crystal	2	10	=
Plasma panel	4	8	=
ELECTRON TUBES			
CRT, black and white TV	5	10	=
CRT, color TV	7	11	=
CRT, industrial	6	10	=
Industrial power	6	12	=
Light and image sensing	5	12	=
Microwave power	9	14	=
INTEGRATED CIRCUITS, DIGITAL			
CMOS	4	12	=
Diode transistor logic (DTL)	6	12	=
Emitter-coupled logic (ECL)	4	14	=
Low power Schottky TTL	4	14	=
Standard Schottky TTL	5	12	=
Standard TTL	4	12	=
INTEGRATED CIRCUITS, LINEAR			
Communications circuit	5	12	=
Data converter	8	12	=
Interface circuit	7	12	=
Operational amplifier	2	4	↓
Voltage regulator	2	4	↓

PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
MEMORY CIRCUITS			
EPROM	4	6	=
PROM, bipolar	4	6	=
RAM, bipolar	4	10	=
RAM, CMOS	4	12	=
RAM, 4k MOS dynamic	6	16	=
RAM, 16k MOS dynamic	6	16	=
RAM, 1k MOS static	6	16	=
RAM, 4k MOS static		6	=
ROM, masked MOS	6	8	up
MICROCOMPUTER/MEMORY SYSTEMS			
Core memory board	8	12	↓
IC memory board	4	8	=
Interface board	8	10	↓
Microcomputer board	4	8	=
MICROPROCESSOR IC'S			
CPU, bipolar bit slice	4	13	=
CPU, 4-bit MOS	4	10	=
CPU, 8-bit MOS	4	12	=
CPU, 16-bit MOS	4	12	=
Peripheral chip	4	10	=
OPTOELECTRONIC DEVICES			
Coupler and isolator	4	12	up
Discrete light-emitting diode	8	16	up
PACKAGED FUNCTIONS			
Amplifier, instrumentation	4	12	=
Amplifier, operational	4	10	=
Amplifier, sample/hold	5	12	=
Converter, analog/digital	4	8	=
Converter, digital/analog	4	8	=
PANEL METERS			
Analog	10	16	=
Digital	4	12	=
POWER SUPPLIES			
Custom	10	18	=
Enclosed modular	4	8	=
Open-frame module	11	13	=
Printed circuit	4	12	=

Leadtimes are based on recent figures supplied to *Electronic Business* magazine by a composite group of major manufacturers and OEMs. They represent the typical times necessary to allocate manufacturing capacity to build and ship a medium-sized order for a moderately popular item. Trends represent changes expected for next month.

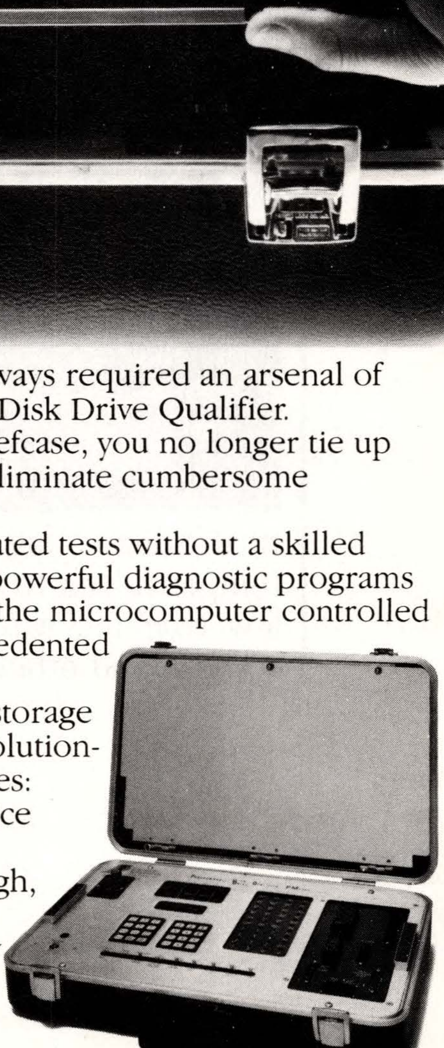
Thorough testing of disk drives and packs has always required an arsenal of expensive equipment. Now, all you need is the PM 4000 Disk Drive Qualifier.

With this programmable microcomputer in a briefcase, you no longer tie up mainframes and controllers. You run tests in real time. Eliminate cumbersome exercisers and null meters.

The Qualifier performs any number of sophisticated tests without a skilled operator. It's as simple as a calculator to use. Call up its powerful diagnostic programs at the touch of a key. Or, easily program your own. With the microcomputer controlled Qualifier, you format packs and align heads with unprecedented speed and accuracy.

It's compatible with any rigid disk moving head storage module drive and many others. The Qualifier offers revolutionary benefits to anyone involved with rotating media drives: original equipment manufacturer, system marketer, service company, user or media manufacturer.

For a brochure on this technological breakthrough, write or call Pioneer Research, 1745 Berkeley Street, Santa Monica, CA 90404 (213) 829-6751. Manufactured by Pioneer Magnetics.



THE DISK DRIVE QUALIFIER

By Pioneer Research

CIRCLE NO 44

Do standard, low cost power supplies have to be tweaked and modified to work? Not with Sierracin power systems.

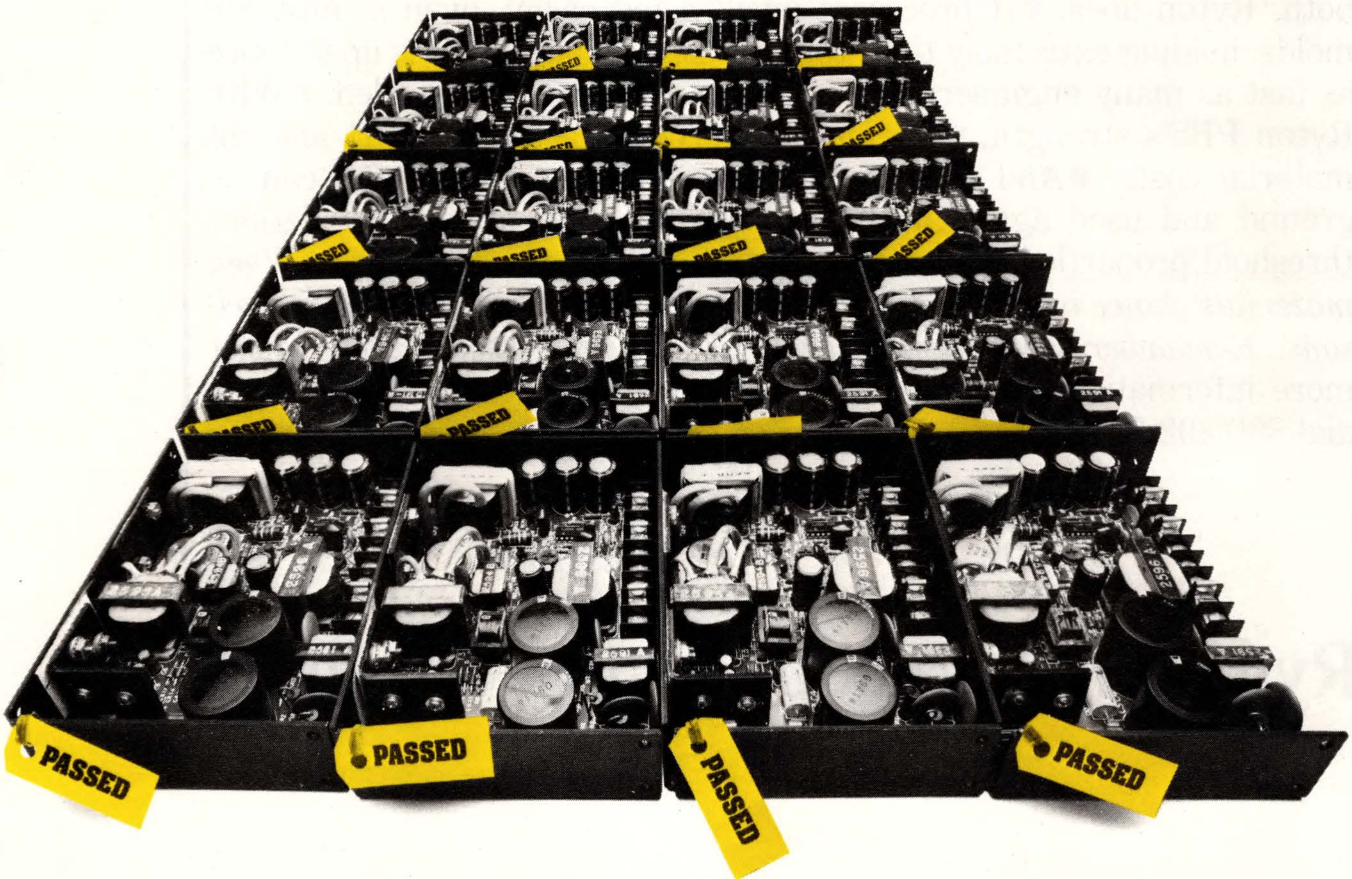
The power supplies we design are made to deliver a cost-performance ratio second to none. Our multi-output switchers are prime examples. Auxiliary outputs are pre-regulated by the switching section, then post-regulated with linear regulators. As a result, *each* output remains tightly regulated regardless of individual load changes. This means excellent dynamic response characteristics. No cross regulation. And "goodbye" to unexplained system crashes.

What about line transients? Our switchers have a wide ac input range of 90-132/180-264 volts which offers greater immunity to line noise and brownouts.

And those tight, little spaces? Our compact, low-profile line of 40 to 500 watt, open-frame dc switching power supplies will fit just about anywhere. Prices start at a low \$45—with OVP on every product including linears at no extra cost.

In short, we build affordable power supplies which keep on working—the first time, every time—you put them in your system. It's what you can expect from Sierracin/Power Systems. A young, dynamic 6-year-old company that's already a recognized industry leader.

See for yourself. Write for our new 1981 Power Supply Catalog. Or dial our toll free number.



For technical information or application assistance, call:

800-423-5569

In California, call (213) 998-6811 collect.

Sierracin/Power Systems

20500 Plummer Street, Chatsworth, California 91311
Telephone (213) 998-9873

CIRCLE NO 45

Editor's Choice: New Products

Computer's Multibus card slots tailor it to engineering design

A high-performance minicomputer based on a 16-bit 8086-type μP, the Monitor Workstation features five Multibus (IEEE-796) card slots that you can employ to extend its usefulness or to design your own Multibus-compatible cards.

The computer system incorporates a high-resolution 15-in. video display, a keyboard and up to 1M bytes of RAM. Mass-storage options include floppy and Winchester disk drives.

In the Monitor Workstation configuration, the CRT display and detachable keyboard sit on a desk; the processor and mass-storage units reside in vertical cabinets that, while designed to sit on the floor, are also small enough to fit on a benchtop. An older version of the system, the Integrated Workstation, houses the CPU and two Multibus card slots on the desktop, along with the CRT display.

Five Multibus card slots *complement the Monitor Workstation's own computer bus and tailor the system to custom hardware-design tasks.*

Multifunction keyboard

Each workstation has a 98-key keyboard with typewriter-style sculptured keycaps. The keyboard includes a 14-key numeric pad, an 8-key status/control-function pad, a 6-key cursor-control pad, a 4-key page-control pad and 10 user-definable function keys. LED indicators on eight keys are software controllable.

Mass-storage units are available in a variety of configurations, ranging from dual 500k-byte floppy-disk drives to dual 40M-byte Winchester units. Four versions of basic mass-storage units provide a disk controller and two disk drives: 500k-byte floppies or 10M-, 20M- or 40M-byte Winchester disks.

Mass-storage expansion units consist of one or two 20M- or 40M-byte Winchester disks. Because a base-unit disk controller can handle as many as three Winchester drives, you can connect as much as 120M bytes of Winchester storage to one workstation.

High-speed bus

The computer's processor, memory-I/O, video-display control and optional memory-expansion boards link up through a proprietary high-speed bus. The Multibus card cage, separate from this main bus, allows you to add more processors or additional masters or slaves to the system for custom-device I/O. The dual-bus architecture accommodates user hardware extensions in the Multibus slots without affecting the speed of the main bus.

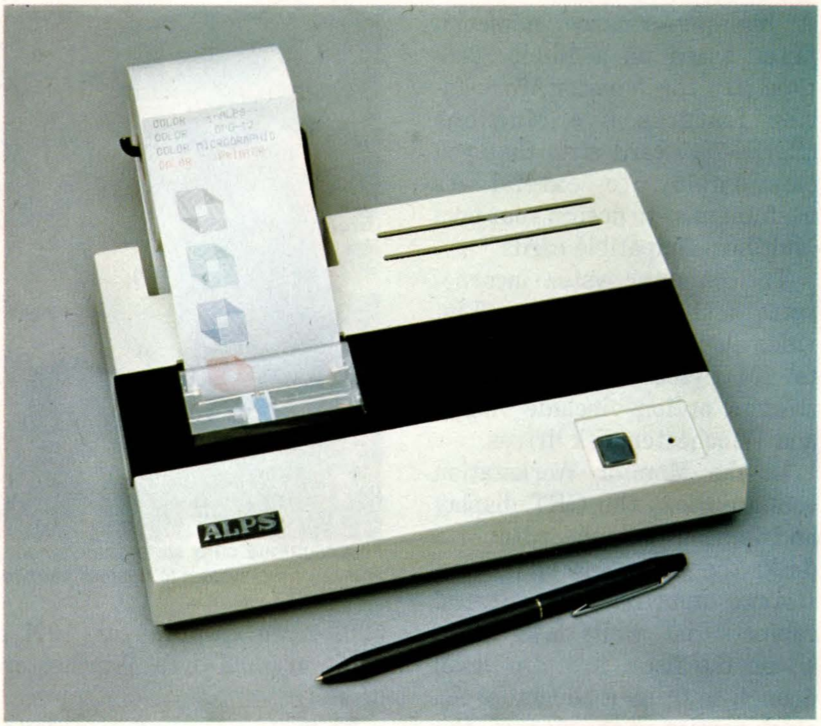
With a 10M-byte disk drive, 500k-byte floppy-disk drive, 128k bytes of RAM, two serial ports and a parallel printer port, the Monitor Workstation costs $22,500. With 256k bytes of RAM, it runs $24,000. A workstation without disk drives, which you can tie as a slave to one equipped with mass storage, costs $10,500 with 128k bytes of RAM and $11,990 with 256k bytes. The Integrated Workstation is about $4000 less expensive.

Prices include the CTOS operating system, with executive, editor, debugger, 8086 assembly language, diagnostics and asynchronous-terminal emulator. Available programming languages include COBOL, FORTRAN, BASIC and PASCAL.

Convergent Technologies, 2500 Augustine Dr, Santa Clara, CA 95051. Phone (408) 727-8830. **Circle No 464**

Editor's Choice: New Products

Miniature graphics printers make 4-color drawings



Smaller than textbooks *and weighing slightly more than 1 lb, Models 1100 and 1200 printers provide 1- or 4-color alphanumerics and graphics, several ASCII-character sizes, 6- to 12-cps print rates and a choice of 10 to 40 columns, all user programmable.*

Barely larger than textbooks, Models 1100 and 1200 printers use tiny ballpoint pens to transfer as many as four colors onto 2.28-in. roll paper. They can enscribe alphanumerics, graphics and special symbols (such as Chinese ideograms), as well as images, drawings and graphs.

The printers both come in 1.26×8.46×5.91-in. packages and weigh only 1.12 lbs. Offering true portability, they operate from four NiCd batteries (6V total). In fixed installations, you can power them with an ac-to-dc line converter.

Select 4- or 1-pen printing

Model 1200 employs black, blue, green and red pens, arranged Gatling-gun fashion within the printhead. It prints a 64 ASCII character set across 15, 18, 24 or 36 columns, which are user programmable.

Miniaturization does exact its toll on print rate: Model 1200 writes 36-column formats at 6 cps for a 0.059×0.038-in. character size. (Optional user-programmable character sizes range to 0.236×0.157 in. max.)

Utilizing one pen, Model 1100 prints alphanumerics over 10 to 40 columns in the same character sizes specified for Model 1200. With just one pen, though, it runs twice as fast as the 1200—12 cps across 40 columns.

Easy pen replacement

The pens are lifetime rated at 150,000 characters. To replace one, you merely pull it out and snap in the new one.

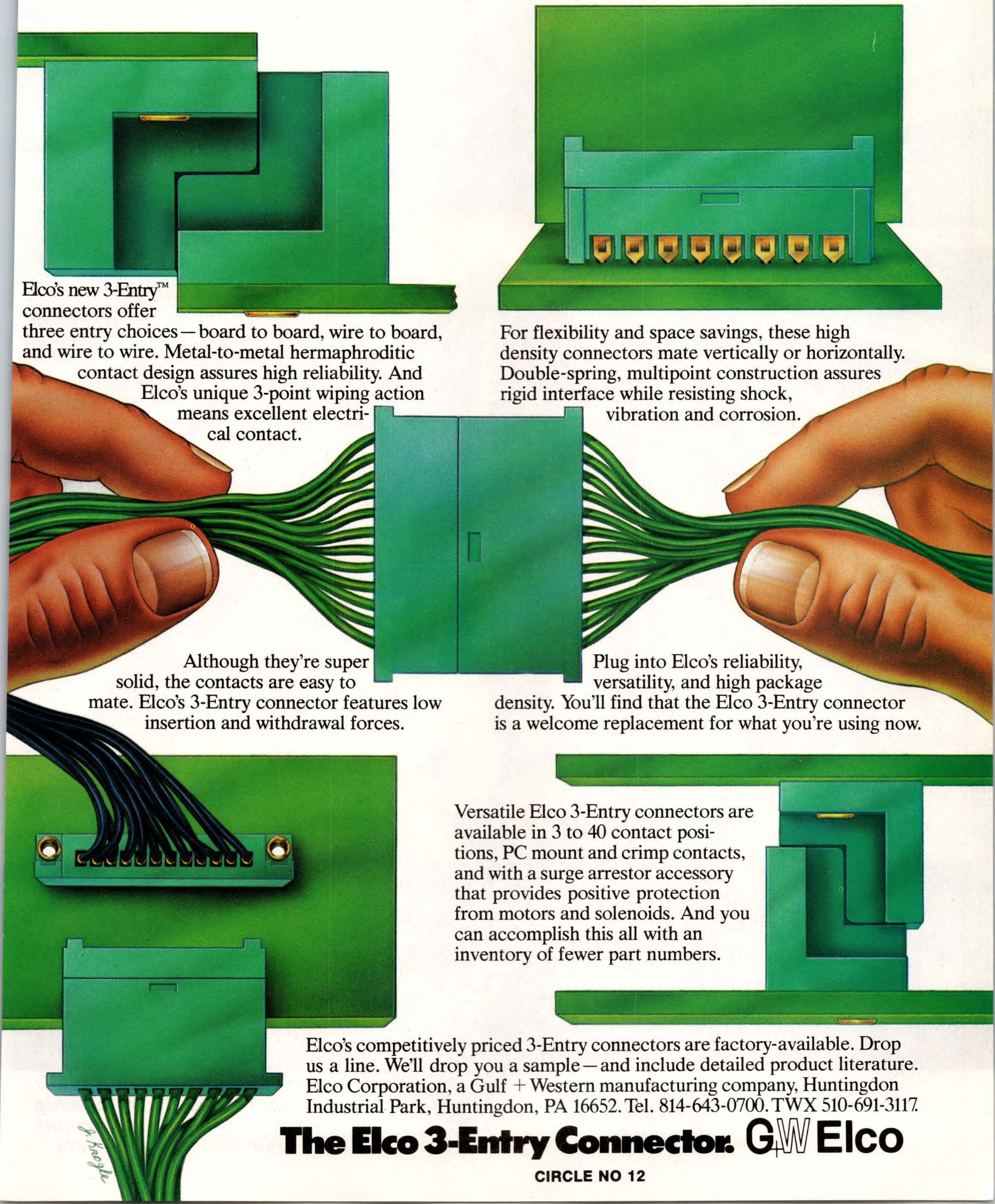
Each model incorporates two stepping motors. One drives the pens along the X axis; the other advances the paper along the Y axis. Model 1200's motor moves in 0.1-mm increments; Model 1100's, in 0.2-mm steps.

Handshaking with a host μP occurs via a Centronics-type parallel interface; an RS-232C serial interface will be available soon.

Aimed primarily at the personal-computer market, the printers function as stand-alone units. They each cost $300. You can buy the printing mechanisms — the 4 - color DPG-12 and the 1-color DPG-11 —as separate OEM units for $75 (100). Available in August.

Alps Electric (USA) Inc, 100 N Centre Ave, Rockville Centre, NY 11570. Phone (516) 766-3636. **Circle No 465**

You've never seen a connector do all of this before.



Elco's new 3-Entry™ connectors offer three entry choices—board to board, wire to board, and wire to wire. Metal-to-metal hermaphroditic contact design assures high reliability. And Elco's unique 3-point wiping action means excellent electrical contact.

For flexibility and space savings, these high density connectors mate vertically or horizontally. Double-spring, multipoint construction assures rigid interface while resisting shock, vibration and corrosion.

Although they're super solid, the contacts are easy to mate. Elco's 3-Entry connector features low insertion and withdrawal forces.

Plug into Elco's reliability, versatility, and high package density. You'll find that the Elco 3-Entry connector is a welcome replacement for what you're using now.

Versatile Elco 3-Entry connectors are available in 3 to 40 contact positions, PC mount and crimp contacts, and with a surge arrestor accessory that provides positive protection from motors and solenoids. And you can accomplish this all with an inventory of fewer part numbers.

Elco's competitively priced 3-Entry connectors are factory-available. Drop us a line. We'll drop you a sample—and include detailed product literature. Elco Corporation, a Gulf + Western manufacturing company, Huntingdon Industrial Park, Huntingdon, PA 16652. Tel. 814-643-0700. TWX 510-691-3117.

The Elco 3-Entry Connector. G+W Elco

CIRCLE NO 12


8/16
TMS9995
TMS9995
new, high-performance processor with exclusive on-chip features to reduce chip count . . . from Texas Instruments.

TMS9995

The fastest 8/16-bit processor available anywhere. From anyone. 16x16-bit multiply in 7.67 µs.

All you have to do is compare and you'll see that the biggest choice in 16-bits just got bigger. Faster. More powerful.

TMS9995 joins the industry's most complete 16-bit family of microprocessors, microcomputers, microcomputer modules, peripherals, software, and software and hardware development systems.

Now you have an easy upgrade to 16 bits, while retaining the economy of 8 bits. And, you'll get all the benefits of TI's all-pervasive family compatibility that lets you move from one product level to another — from single-chips to multi-chips to modules to systems — *protecting your software investment and development systems* as you go — no translators, no code converters, no extras.

And now there's TMS9995 — with all the inherent advantages of memory-to-memory architecture, plus 256 bytes of on-chip RAM.

And now there's TMS9995 — for all those tough tasks that demand 16-bit speed and processing power.

And now there's TMS9995 — with on-chip clock, 16-bit timer/event counter and 8-bit data bus for interfacing to everything from a minimum 3-chip system to a 16-megabyte memory system (just add the 99610 memory mapper).

TMS9995. Shrinking chip count and program size. Ready for VLSI.

Logical link

TI's TMS9940 was the first single-chip 16-bit microcomputer — and the first to transcend the limitations of high-speed and high-resolution. TMS9995 adds the ability to address off-chip memory to the TMS9940 — up to 64K bytes. Together they fill the requirements from small microcomputer-based systems to medium-sized systems, using on-board RAM and off-board ROM, to larger systems needing off-board RAM and ROM.

TMS9995 — Key features

- 16-bit CPU
- 12 MHz clock with on-chip clock generator
- 256-byte on-chip RAM
- 16-bit on-chip interval timer/event counter
- 7 levels of vectored interrupts
- instruction prefetch
- automatic first wait-state generation
- MID — macro-instruction detect interrupt
- single 5-V power supply
- 40-pin dual-in-line-package.

Performance plus

Three times faster than the TMS9900, TMS9995 executes a 16x16-bit multiply in just 7.67 µs. A 32-bit number divided by a 16-bit number in just 9.33 µs. TMS9995 can run with currently available fast memories of 120-ns access times, or by using automatically generated wait states, 450-ns access time memories.

256-bytes of fast on-chip RAM is organized as 128 x 16-bit words, allowing a full 16-bit word access in one clock cycle.

And, TMS9995 uses an intelligent pipelined architecture where the op code of the next instruction to be performed is prefetched. For example, the microcode for Branch and Jump instructions direct TMS9995 processors to prefetch the true next instruction instead of blindly prefetching from the next sequential memory location.

And now, a word about memory-to-memory architecture

The innovative architecture at the very heart of the 9900 Family reaches it's performance peak in the TMS9995 thanks to on-chip RAM. Comparison of execution speed benchmarks clearly show the advantages.

Support, support, support.

Necessary for any microcomputer family. TI's 9900 Family is supported by Pascal, Basic and Fortran software and software and hardware development systems, including a low-cost Evaluation Module, TMAM6095, for $800.* TI also offers training, documentation and expert field assistance. Training, service and design assistance are available at Distributor System Centers, and TI's Regional Technology Centers.

Commitment to 16-bit leadership

The continuing introduction of new, advanced, high-performance 9900 Family CPUs, with TI's state-of-the-art technology and production-proven resources, clearly demonstrates a commitment to leadership. A commitment to choice. A commitment to the future.

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9995 (12 MHz) w/120ns PROM	0.666	0.863	1.240	1.767	10.00	8.0
9995 (12 MHz) w/450ns EPROM	0.950	1.081	1.956	2.696	12.67	10.67
8088 (5 MHz) w/450ns EPROM	1.596	2.402	2.254	1.522	40.8	77.6
6809 (2 MHz) w/450ns EPROM	9.67	57.1	2.376	3.01	91.9	27.6

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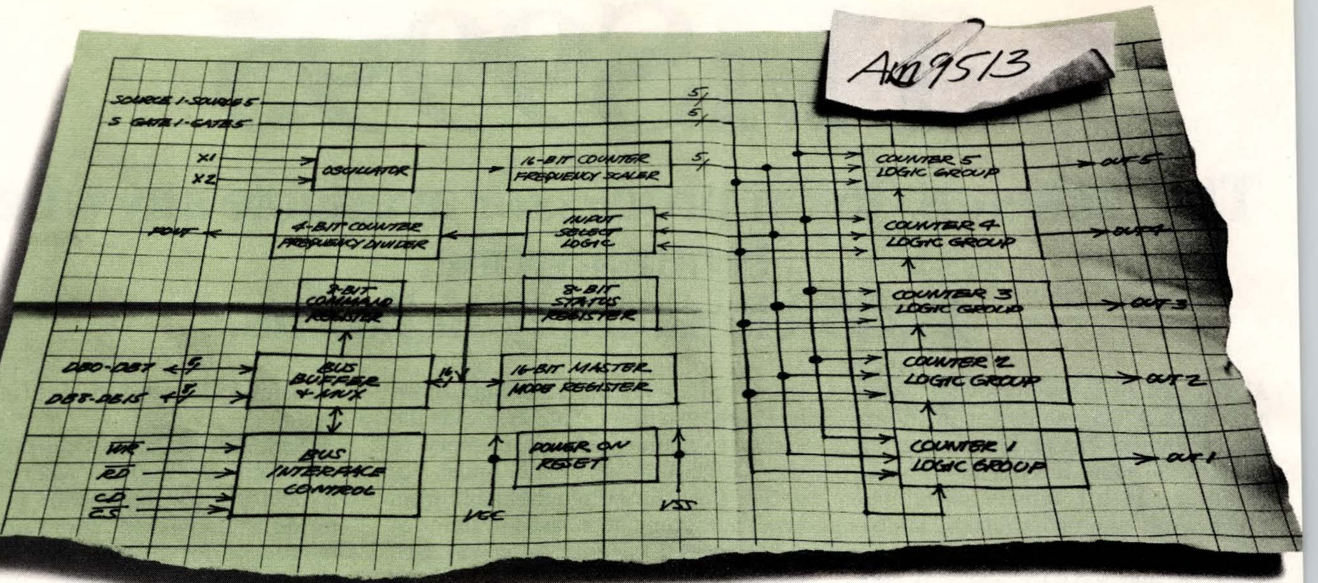

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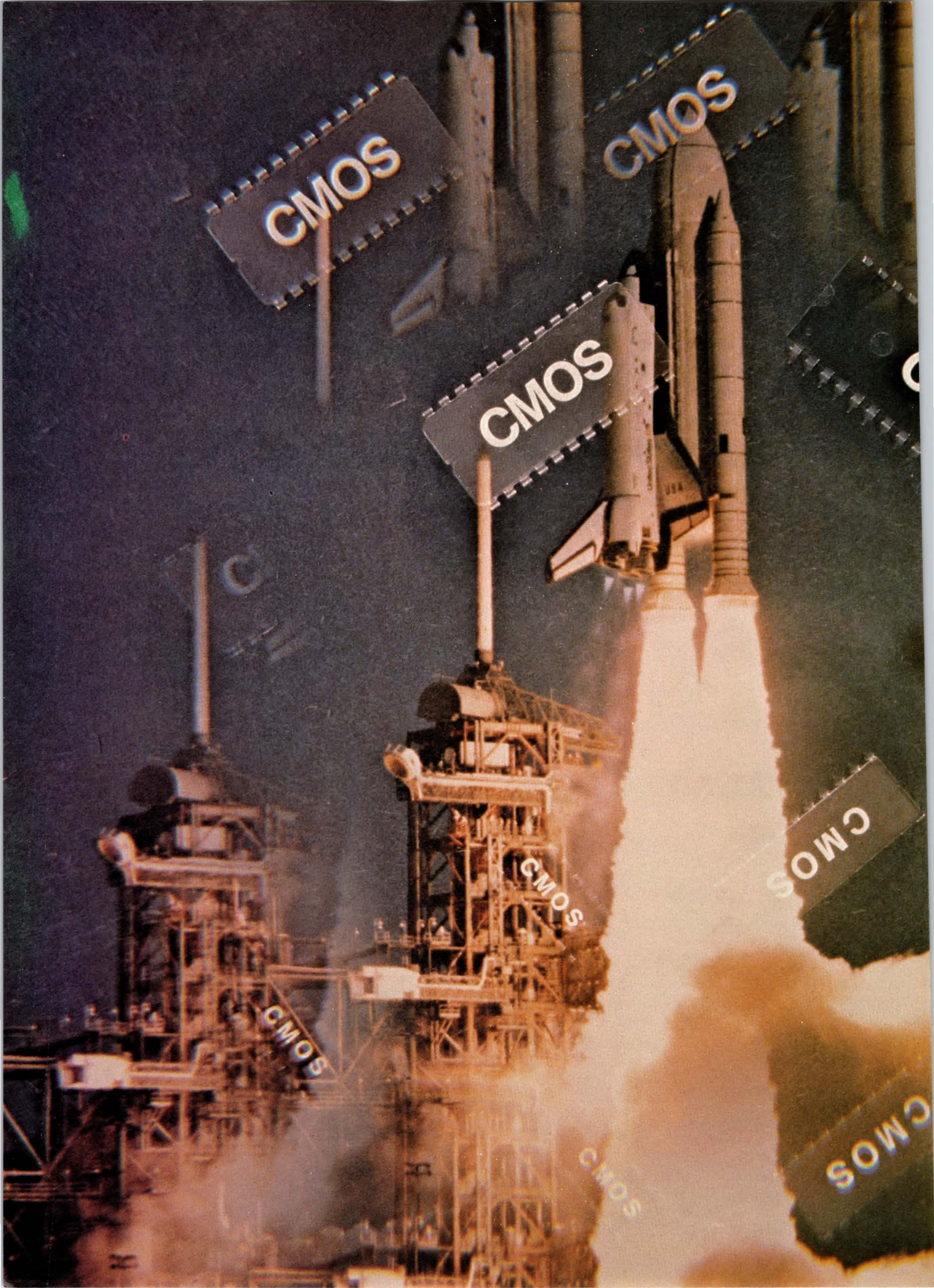
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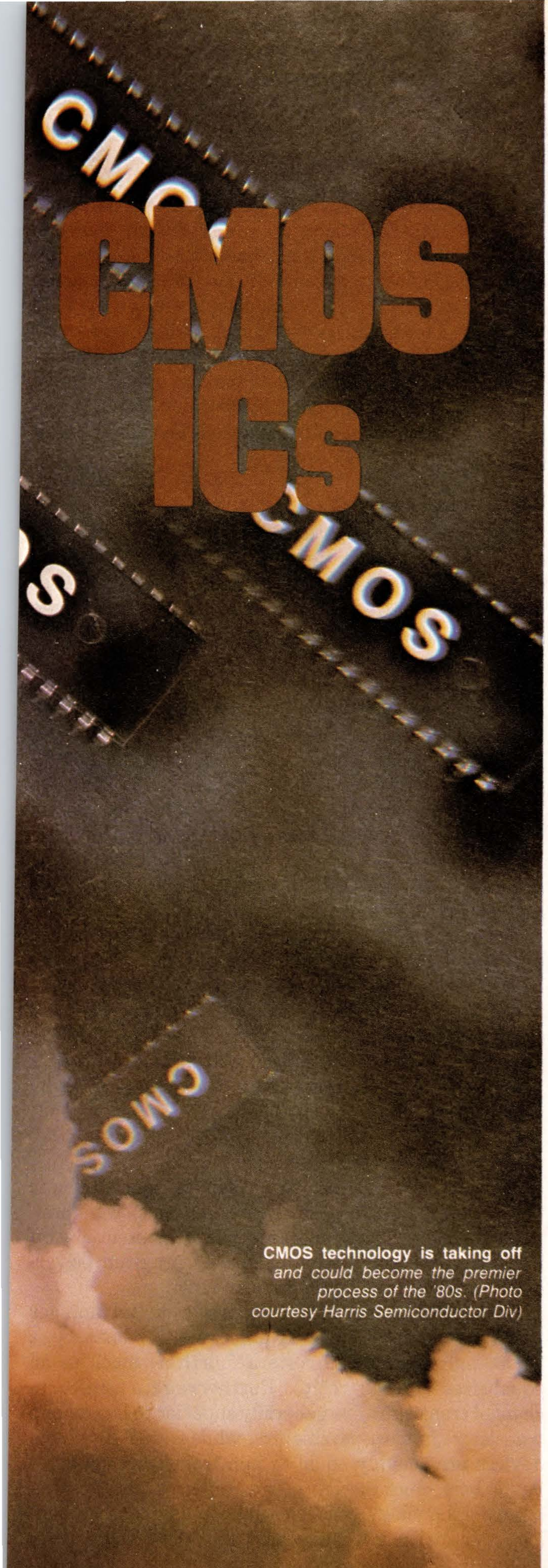


CMOS technology is taking off *and could become the premier process of the '80s. (Photo courtesy Harris Semiconductor Div)*

Riding on a wave of recent product introductions, CMOS is making its bid as the technology of the '80s. Technical and economic factors are combining to give this once-specialized process a shot at the top for use in LSI and VLSI products.

William Twaddell, Western Editor

The '80s belong to CMOS, or so many experts say. As a result, the prediction has become axiomatic—or possibly just a self-fulfilling prophecy. But what's behind all the acclaim? And can CMOS live up to its billing? (After all, I^2L was supposed to reign supreme but has yet to.)

In truth, although CMOS seems particularly suited to LSI and VLSI design by virtue of its performance features and its versatility in linear, digital and mixed-circuitry chip design, it's unlikely to take over the world. At the same time, because the '80s will see volume production of VLSI parts, CMOS's time as a major IC process might indeed have come.

No thermal barrier

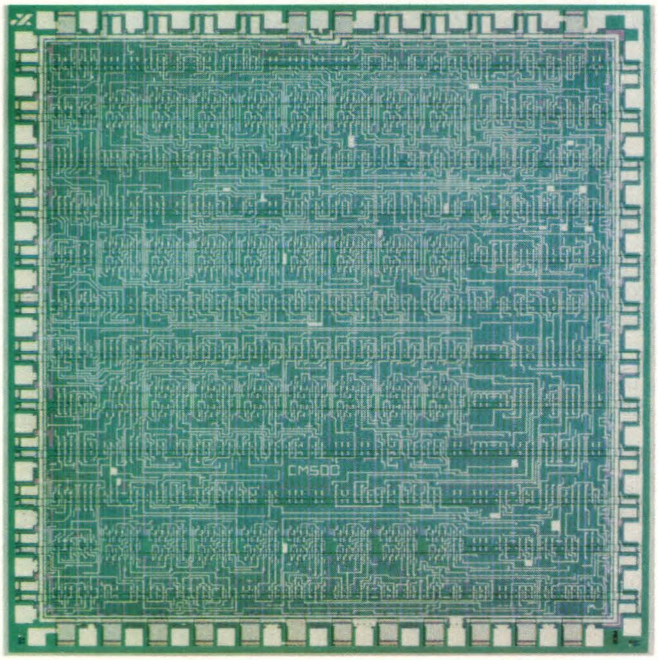
Chief among the many reasons for CMOS's impending ascendance is its low power dissipation. As circuit dimensions shrink and more functions get packed onto a chip, what American Microsystems CMOS R&D manager Don Wollesen terms the "thermal barrier" rises up to block the use of processing technologies that dissipate too much power per unit function. Bipolar technology hit this barrier long ago but survived because its switching time is little affected by junction temperature over its operating range. Additionally, manufacturers have developed special heat-sinked packages to deal with the thermal barrier; they handle as much as 4W dissipation. Such packages might prove essential for technologies such as NMOS to achieve VLSI densities.

The alternative, of course, is a technology that isn't up against the thermal barrier. And that's CMOS. With this technology, the only appreciable power consumed gets used during the brief switching period when a gate changes state; in the static state, the only currents drawn are junction and subthreshold leakage currents—usually orders of magnitude less than the standby currents of even powered-down NMOS logic.

CMOS has many advantages besides low power dissipation

As a result, with CMOS, system designers can save money on power-supply, power-distribution-bus, regulator and cooling-fan costs. And VLSI-chip designers could find that CMOS is the only viable technology for high-performance, highly integrated products.

Actually, CMOS also has several other advantages, which are only now being exploited, thanks to the industry's historical concentration of effort in high-performance NMOS. It features high noise immunity (typically 45% of V_{CC}), wide power-supply range, wide operating-temperature range, high-speed capability and the ability to combine high-quality linear and digital functions on one chip—all attributes that tend to make it a natural choice for LSI and VLSI designs.



CMOS metal-gate semicustom gate arrays *are available from Exar Integrated Systems in 200- to 400-gate complexities. Exar can fabricate prototypes in several weeks, and full production can start 2 to 3 months after prototype acceptance. The firm will have a silicon-gate process ready soon.*

The increased complexity of VLSI chips also requires a technology versatile enough to handle almost any circuit function, and that's where CMOS really shines. The number of functions available in it is staggering: In addition to general-purpose logic such as gates, buffers and flip flops, CMOS finds use in analog switches, multiplexers, A/D and D/A converters, μPs, RAMs, ROMs, PROMs, EPROMs, EEPROMs, op amps, timers, counters, oscillators, pulse generators, display and interface drivers, phase-locked loops, comparators and complex combinations of linear and digital circuits such as watch/clock chips, audio filters, codecs, speech synthesizers, smoke detectors and digital-voltmeter ICs.

The key factor illustrated by this diversity is that CMOS can implement complex linear and digital functions, combine them on the same chip and *still* dissipate little heat. And the key to this flexibility is in turn the number of basic circuit devices that CMOS can form. Among active devices, you can find symmetrical p- and n-channel MOSFETs and (in p-well designs) an npn common-collector transistor. And passive devices include MOS, bipolar and zener diodes; MOS and junction capacitors; p^+ (50 to 200Ω/square) and p^- (1 to 5 kΩ/square) resistors; and p^- pinch resistors (3 to 20 kΩ/square). These building blocks permit production of linear functions such as band-gap or zener voltage references, and the npn emitter follower allows incorporation of high-current source and sink drivers in circuit designs.

Competition heats up

The primary competition for CMOS is and will continue to be high-performance NMOS (HMOS). And although CMOS has a theoretical 2:1 speed edge over NMOS, in practice NMOS's smaller line widths have kept it ahead in the speed department.

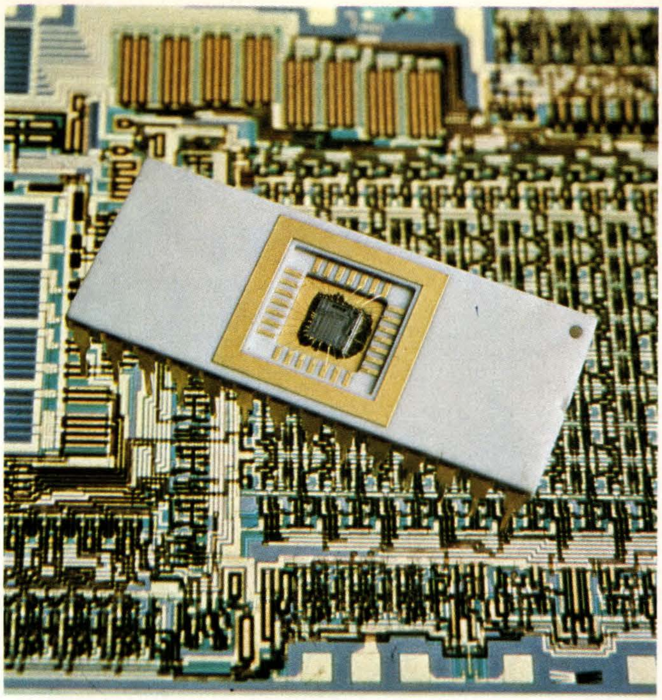
CMOS's speed advantage derives from its use of both active pull-up and pull-down in its gates, providing a symmetric waveform and good source and sink drive for capacitive loads. (Because of its passive pull-up, NMOS makes less source drive available and consequently has a slower average switching time.) The price paid for this speed, though, comes in higher dissipation: as much as four times that of NMOS at high toggle rates. However, all devices in a circuit rarely toggle simultaneously, so CMOS's low static dissipation offsets its high active power draw.

Other factors also affect the CMOS-vs-NMOS speed question. CMOS has a high noise margin because its logic states are very close to the supply-voltage rails. NMOS, on the other hand, has a poor V_{OL} margin and might also have a poor V_{OH} margin if the depletion-load process isn't closely controlled. And thanks to NMOS's poor rise time, if you push circuit speed, V_{OH} can really degrade.

Power-down is automatic

Another key CMOS advantage is its automatic power-down: As you decrease frequency, power dissipation declines correspondingly; power is essentially off in a static state. You can also easily program power-down capability into CMOS linear functions.

Linear CMOS circuitry even has some advantages that surpass those of bipolar processes. For instance, a 30,000-mil² CMOS chip costs a fourth as much as an equal-sized bipolar chip. Furthermore, CMOS p-channel transistors are generally superior to lateral pnp transistors in most parameters, while CMOS n-channel devices are roughly equal to npn transistors. CMOS's input bias characteristics are superior to those of bipolar technology, and although it has poorer open-loop gain, drift, matching characteristics and 1/f noise,



µP-connection problems are virtually eliminated *with Analog Devices' AD7581 8-channel, 8-bit ADC. Incorporating an on-chip 8×8-bit dual-port RAM, it can perform a channel conversion in 66 µsec and store the result in the RAM, ready to be read by the µP. The device connects directly to most 8-bit µPs and removes a great deal of software overhead from a µP system.*

switched-capacitor autozero techniques (such as those used in Intersil's ICL 7600 family of commutating autozero op amps or its new 7650 chopper-stabilized amp) can produce a precision op amp comparable to a bipolar unit. And compared with NMOS in complex analog/digital applications such as codecs, CMOS consumes less area because it makes more circuit elements available and uses fewer devices to accomplish a given function, even though NMOS device sizes might be smaller.

CMOS can also perform many functions that NMOS can't or finds very difficult. For instance, the complex ac waveforms needed to drive multiplexed LCDs can't experience a net dc bias of more than 50 mV without producing permanent damage. CMOS, with its symmetrical voltage swing, easily satisfies this waveform requirement—and at an unmatched low power level. The process's complementary transistor pair provides a current mirror, referred to the positive supply, that's missing in n-channel technology. Additionally, high-temperature operation (greater than 150°C) is possible with CMOS for short times, and the fact that CMOS junctions run about 20°C cooler than their NMOS counterparts gives CMOS a 10- to 100-times reliability edge with respect to failure rates.

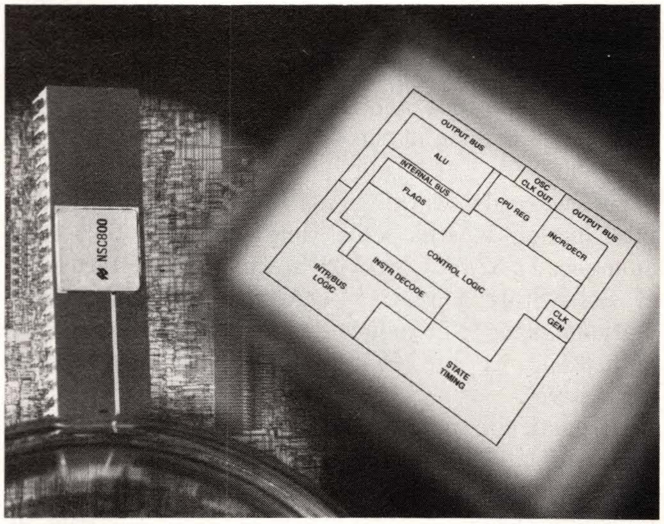
But what about n-channel technology's density edge over CMOS? According to CMOS industry sources such as AMI's Wollesen and Intersil R&D vice president Dave Fullagar, this edge comes mostly from using smaller line widths and, of course, from the passive poly load in an NMOS RAM cell. CMOS is closing the line-width gap: The parameter is now only 20 to 30% larger than its NMOS counterpart in complex logic circuits. And as for the NMOS poly load cell, the high-gigohm values achieved in the latest generation of loads are consistent with CMOS design. Thus, large-RAM designs employ CMOS in their peripheries and NMOS in the memory cores. As a bonus, the n-channel core is built into the diffused p wells necessary for CMOS—a feature found to lend the cell transistors more immunity to alpha-particle strikes than standard NMOS affords.

Products abound

All these factors are no doubt impressive, but what about product availability? Can you get what you want?

The answer is yes. As noted, a very wide range of CMOS products is available, covering both linear and digital devices. And new manufacturers are continually appearing as everyone jumps on the CMOS bandwagon.

A rough count of manufacturers providing CMOS gate arrays, for example, reveals 13, including such old timers as California Devices, Exar, International Microcircuits, Interdesign, Master Logic, Microcircuit



The basis of a new family *of high-performance 8-bit µPs, National Semiconductor's NSC800 employs the company's oxide-isolated double-poly CMOS process and combines the Z80's architecture and instruction set with the 8085's multiplexed I/O structure. The firm is also offering a RAM/I-O/timer chip and a ROM/I-O chip, as well as several peripheral "glue" circuits, all in P²CMOS, for design of high-performance systems at 1/20th the power dissipation of conventional TTL.*

Technology and Holt. These firms have been joined by more recent arrivals such as American Micro Circuits Corp, Semi Processes Inc, AMI, Fujitsu and Mitel, and Precision Monolithics will soon add to the ranks.

Another bellwether product area encompasses µPs and µCs. Here CMOS is or will shortly be represented in the products of 15 companies. For example, AMI now makes the 4-bit S2000 µC in CMOS and will soon offer a CMOS version of the 6809 that will actually be smaller than the µP's original NMOS version. Mitel Semiconductor fabricates a CMOS version of the 6802, and

NMOS's density edge is now less pronounced

Motorola has manufactured its own 6805 in CMOS. Hitachi is also working on a 6805 CMOS version, as well as a 6801 and a 4-bit controller μC. Furthermore, CMOS versions of the 8048 are promised from Hughes, National Semiconductor, NEC and Oki, and Toshiba expects to start sampling its TCP8049 next month.

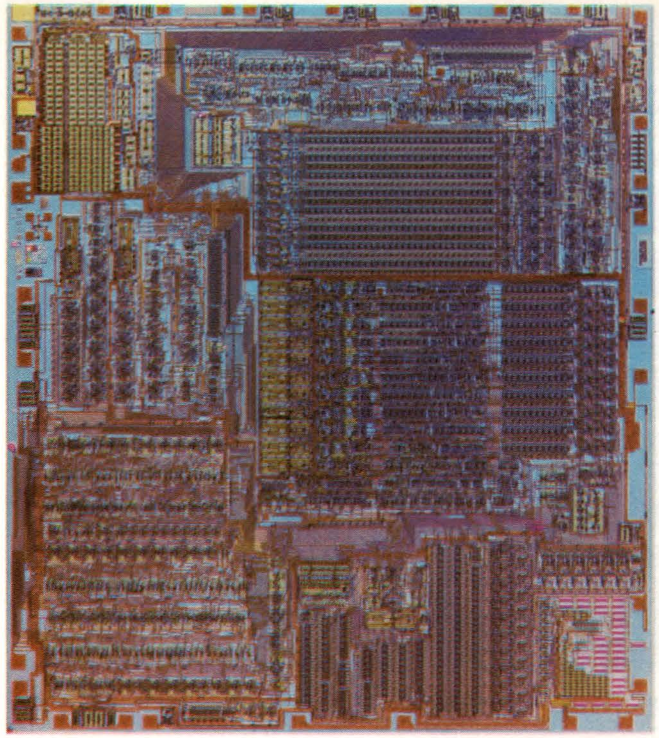
Toshiba has also demonstrated a 16-bit CMOS-NMOS/SOS μP which will probably be used in the firm's own minicomputer. Also aiming at in-house use, Rockwell produces a totally CMOS/SOS 16-bit μC for its airborne computer systems. Other μP/μC families now or soon to be in CMOS include Texas Instruments' 4-bit TMS 1000, General Instrument's 8-bit PIC16C55, National Semiconductor's NSC800 (combining the best features of the Z80 and the 8085), Oki's 4-bit offering (MSM5840), a processor from Commodore (probably the 6502) and the 6100 family from Intersil and Harris.

Indeed, along with the 6100, one of the earliest CMOS-μP families is still going strong: RCA's 1802 is second-sourced by Hughes and Solid State Scientific, and new versions are appearing: RCA has announced the single-chip 1804, and Hughes is expected to produce a superset version of the 1802, tentatively designated the 1806.

Hughes is also working on a 16-bit CMOS μP, but its introduction is still some time off. And Bell Labs announced a 32-bit CMOS μP at this year's International Solid-State Circuits Conference (ISSCC), while National plans to introduce a commercial CMOS version of a 32-bit μP by 1985 (perhaps it will be a 16000 derivative).

Of particular note among these offerings, the Bell CPU uses latchup-free Twin-Tub CMOS technology and implements its ALU with a glitch-free dynamic circuit technique termed domino CMOS. In this technique, all circuits get activated simultaneously by a single clock. Bell reports a 2-times speed increase compared with conventional CMOS, along with the density boost associated with dynamic techniques.

The two SOS/CMOS 16-bit μPs now available are architecturally quite different, reflecting their differing intended applications. Rockwell's AAMP (advanced-architecture microprocessor), for example, features 2-μm channel lengths with molybdenum-silicide gates, a 200-nsec microcycle, more than 48k of on-board ROM, power dissipation of only 400 mW and a stack-oriented architecture that supports high-level languages. The Toshiba T88000, on the other hand, uses a mix of NMOS and CMOS to achieve high density, high speed and low power. In this device, channel lengths are 3.5 μm with poly gates, power dissipation equals 600 mW and the architecture is register oriented. Although the Rockwell device is microprogrammed, its application is essentially fixed; the Toshiba part uses external ROM microcoding that allows it to be targeted at different applications—for example, personal computers, minicomputers and word processors.



Fabricated with moly-gate CMOS and thin-film processes, *this custom chip from Micro Power Systems is a high-clock-rate speech synthesizer that can create any voice, male or female, as required. Micro Power Systems specializes in very-low-voltage and very-high-frequency CMOS processes.*

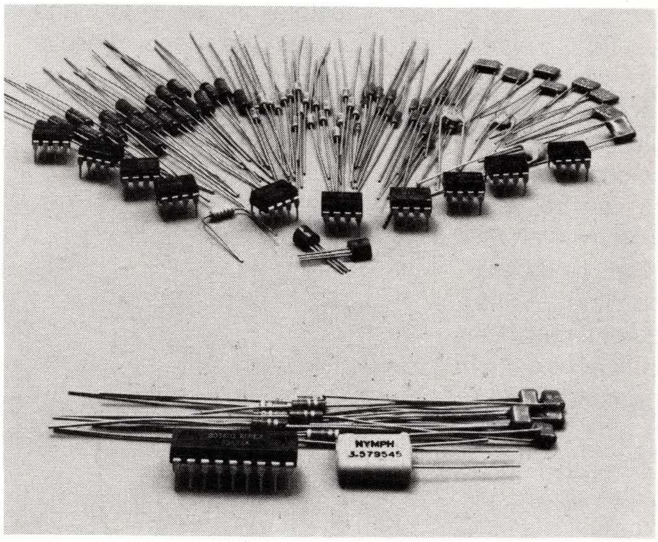
RAMs lead the field

As key products in the move to LSI and VLSI techniques, of course, μPs are important in their own right. But without memory, they're nothing. And so, manufacturers of CMOS products haven't neglected RAM, either—the count includes at least 15 suppliers. Represented are such pioneers in the field as Harris Semiconductor, which produced the first 4k CMOS RAM, the first CMOS PROM and the first 64k CMOS RAM module. Harris is also manufacturing CMOS EPROMs and EEPROMs and is committing heavily to CMOS in the telecommunications area, a prime CMOS application.

Other pioneers in CMOS RAMs include AMI, RCA, Intersil and Intel. The latter, for example, has recently re-entered the field with an updated process compatible with its HMOS n-channel efforts. Termed CHMOS, its first products are the 100-nsec 4k×1 5104 and 1k×4 5114, which use full 6-transistor static cells but sport lower power consumption than the older 6514 design.

AMI, Intersil and RCA are broad-line suppliers of all types of CMOS parts, including RAMs. Especially noteworthy is RCA, which pioneered the first line of CMOS logic (CD4000 family) and has been the only commercial supplier of SOS/CMOS parts. The firm produces RAM, ROM, EPROM, peripherals and watch/clock chips in addition to the upgraded 4000B logic family, and its most recent introduction is the CA3300, a 6-bit, 15-MHz flash A/D converter that sells for only $38 (1000). Consuming only 200 mW, this part is fabricated in SOS/CMOS—proof that RCA has not abandoned the technology but is merely being more selective in its use (EDN, September 20, 1980, pg 55).

AMI's broad line of CMOS parts is particularly strong in the telecomm area, and the company has recently introduced the LPC-10 CMOS speech synthesizer with 20k of on-chip ROM. And although Intersil sells CMOS RAMs, ROMs, EPROMs and μPs, its forte is in linear CMOS devices, including analog switches,



A DTMF bandsplit filter, *the S3525 includes a dial-tone filter, high-group and low-group separation filters and limiters for squaring off the filtered signals. The $14.50 (100) CMOS device from American Microsystems, available now, replaces a large number of active and passive devices and achieves improved reliability.*

multiplexers, A/D converters, counters, display drivers, op amps and timers. Indeed, the company's work with autozero techniques has advanced the CMOS cause in linear design more than virtually any other development. The best product example is the ICL 7650 chopper-stabilized op amp, which features a gain-bandwidth product of 2 MHz, 5-μV offset voltage and long-term drift of less than 100 nV/month.

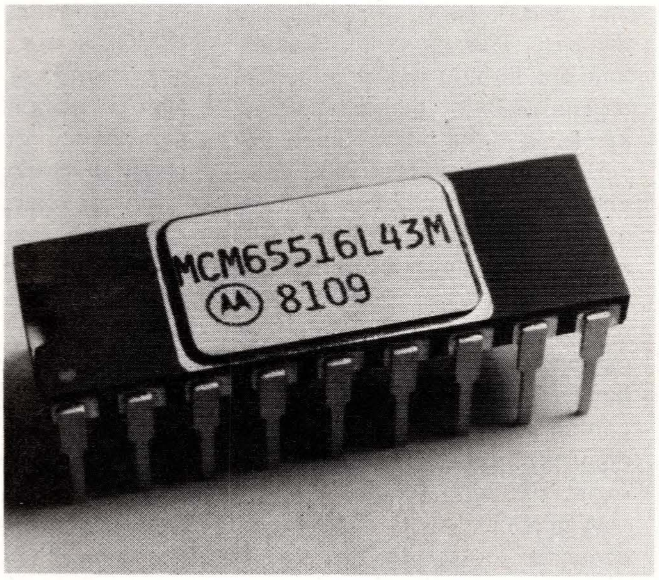
The rest of the list of CMOS-RAM suppliers includes such newcomers as Hitachi, Matshushita, Micro Power Systems, Mitsubishi, National, NEC, Oki, Solid State Scientific, Synertek and Toshiba. Hitachi, indeed, has lit a fire under the stodgy CMOS-RAM market by introducing very dense RAMs with speeds rivaling those of the fastest NMOS parts. And the company shows no signs of slowing its progress in that area. Meanwhile, Matsushita is one of the two companies that have developed a 64k CMOS RAM; its device was discussed at the 1980 ISSCC and could be ready next year. Toshiba also foresees an early '82 introduction for its 64k CMOS RAM; it's now selling the 2k×8 5516—a 250-nsec, 200-mW device for which it claims a standby power three orders of magnitude less than that of previous chips—for $22.95 (100). Maximum standby current for the device is just 0.2 μA.

Strong competition from Japan

As you can see from the lists of CMOS-device manufacturers, Japanese semiconductor firms are strongly represented in the CMOS field. They gained their expertise years ago in the manufacture of watch and clock circuits and could have a technology edge as a result of this early work.

One expert who foresees such an edge is John Hall, president of Micro Power Systems, a custom house turning commercial manufacturer. Hall has been predicting for years that the Japanese will take a large part of the CMOS market, and he hasn't changed his opinion. And although MPS is now sticking its toe into the commercial volume market, Hall's experience in custom circuitry is leading him to search for niche markets that won't experience the brunt of the Japanese competition.

Hall's firm has several advanced CMOS processes to



Organized as 2k×8 bits *of silicon-gate CMOS ROM, the MCM65516 from Motorola has a 430-nsec access time and works with multiplexed-bus μPs. It operates in three different modes: active HIGH, active LOW and MOTEL (MOTorola/intEL), the latter directly compatible with the 6800 and 8085. The device complements the firm's CMOS MC146805 μP and costs $20.50 (100) in plastic.*

its credit, including a 1V process, a high-density, 2-layer metal (moly and Al) technique and a high-frequency process that permits fabrication of 50-MHz dividers. The company's latest thrust combines CMOS, bipolar and thin-film processes on one chip; first commercial use of this technique will be in a high-performance A/D converter.

One Japanese company that Hall's strategy is aimed at is Oki Semiconductor. In addition to complex watch/clock chips, it manufactures RAMs, ROMs, display drivers, μCs, μPs and some peripheral circuits. And its products compete directly with those of two US suppliers: Motorola and National Semiconductor.

Motorola's product lineup includes remote-control encoder/decoders, MUXed LCD drivers, PLLs, codecs

Continued on pg 96

What is CMOS?

Complementary metal - oxide semiconductor (CMOS) technology involves nothing more than the fabrication of n- and p-channel MOS devices on the same substrate and is analogous to using both npn and pnp transistors in a bipolar circuit. The process has been around since the late '60s but has not enjoyed the popularity of bipolar or NMOS for various historical reasons, despite its many excellent features.

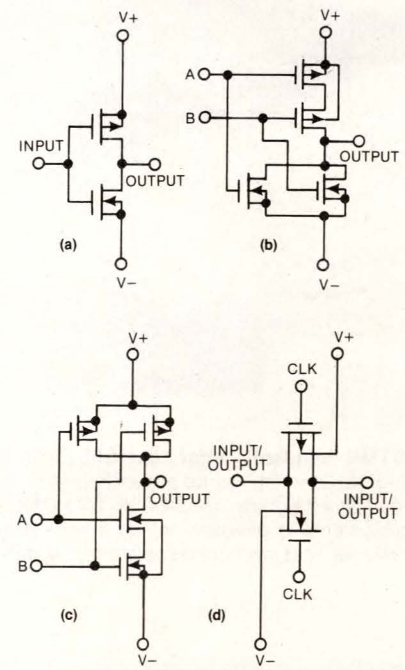
The basic junction-isolated CMOS structure is built on a lightly doped n^- silicon substrate into which deep p^- wells are diffused. The p-channel transistors are formed in the substrate region, while the n-channel devices reside in the p-type tubes. For wider supply-voltage operation and to stop parasitic surface-current leakages between elements of different transistors, guard rings (also termed guard bands or channel stoppers) are diffused between n- and p-type devices. Gate-electrode material can vary widely, from the original aluminum gates to the newest exotic silicide materials.

Whatever flavor CMOS you consider, you can be sure it uses only enhancement-mode transistors, in contrast to high-performance NMOS, which employs enhancement, depletion and zero-threshold devices. This use of enhancement-only device types gives CMOS its automatic power-down capability and permits easier matching of gate thresholds. Furthermore, use of both n- and p-channel MOSFETs in the basic inverter gate means one of the transistors is always OFF, so there's no current path from power supply to power supply, and both active pull-up and pull-down paths exist for the load. The first feature gives CMOS its extremely low power dissipation in the static state (only leakage currents flow), and the second means tha CMOS devices can be very fast—even faster than NMOS. (CMOS's rise and fall times are short and symmetrical, while NMOS has a short fall time but a significantly longer rise time because of its high-resistance load.)

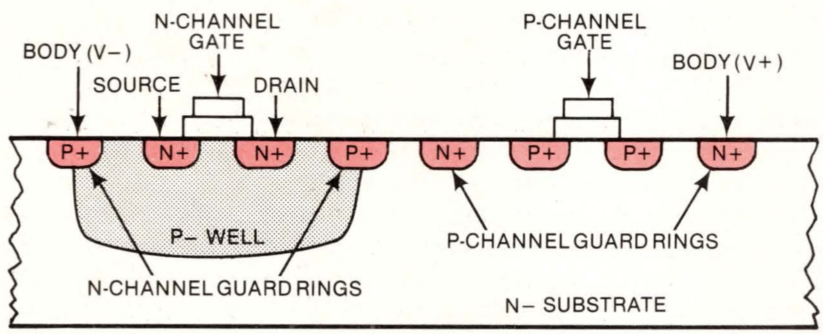
On the negative side, at very high toggle rates, CMOS can draw two to four times the power of NMOS because as a device changes state, both transistors are ON for a short time, creating a power - supply - to - power - supply path. And the faster a CMOS device toggles, the longer this path exists, producing a straight VI-type power draw. Additionally, in charging the capacitive load of the next gate and its own internal capacitances, a CMOS element also incurs a CV^2f power factor, which is directly related to frequency of operation. Fortunately, in practice, all circuit elements rarely toggle at once, so most of the devices remain in a quiescent state.

The simplicity of the inverter configuration and the guard-ringed transistors give CMOS a wide supply range, typically 1 to 15V. (The lower figure results from controlling thresholds with ion implantation to 0.4V and below, while the upper one is more dependent on device-to-device isolation and the gate oxide's punch-through voltage.) An advantage of this increased power-supply range is CMOS's greatly increased drain-source current (I_{DS} increases as the square of V_{GS}), but the penalty is greatly increased power dissipation as well from CV^2f dissipation, plus larger VI dissipation from the increased logic swing.

CMOS logic swing ranges virtually from supply to supply, giving the technology an excellent noise immunity—typically 45% of V_{CC},

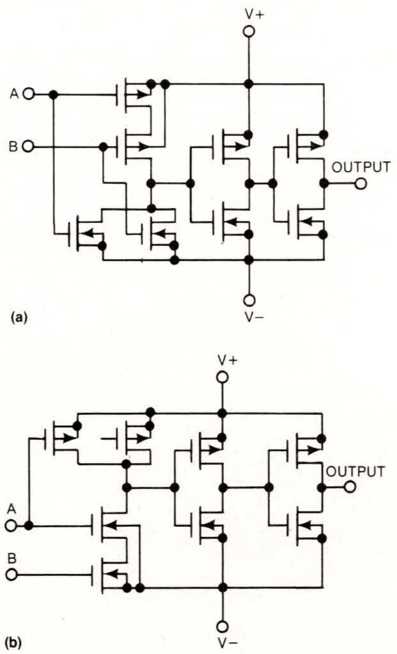


All CMOS digital circuitry *is implemented using four basic circuits: inverters* ***(a)****, NOR gates* ***(b)****, NAND gates* ***(c)*** *and bidirectional switches* ***(d)****. Complex gates combine two or more of these basic circuits to achieve any logic function.*



The basic junction-isolated CMOS structure *exhibits many space-wasting features that are eliminated in the newer selectively oxidized, silicon-gate field-doped processes.*

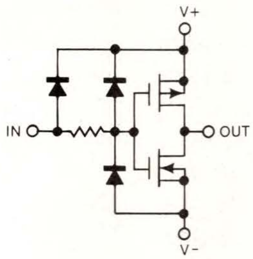
which is better than that of either TTL or NMOS. This feature, combined with CMOS's noncritical power requirements and wide operating - temperature range, spawned RCA's original CD4000 logic family, which quickly established itself with industrial, automotive and aerospace customers.



B Series 4000 CMOS circuits *contain buffered gates that provide increased drive output and reduced pattern sensitivity. Buffering allows the use of smaller geometry transistors because the buffer stages offer a low-impedance load.*

However, the original family (now designated 4000A), while exhibiting all of CMOS's advantages, wasn't terribly stable and was terribly expensive. It was also easily destroyed by input overvoltages and exhibited a pattern sensitivity at the output. In the early '70s, with the perfection of the ion implanter and the double-buffered B Series parts, these problems were solved.

The B Series has JEDEC standard specifications superior in input, output and internal transfer characteristics when compared with those of the old unbuffered logic. This series is the logic

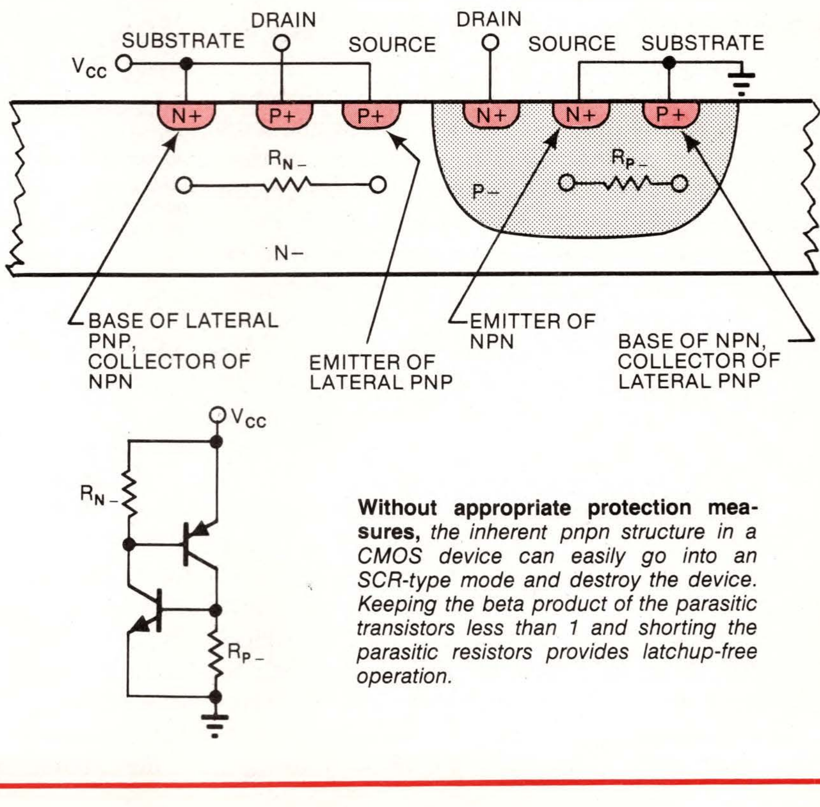


A 2- or 3-diode input-protection scheme *allows operation over wider input levels and costs very little in additional space. This type of circuit is standard on almost all CMOS devices.*

currently sold and widely second sourced. Another logic family, National Semiconductor's 54C/74C, has the same characteristics as 4000B units but is pin and function compatible with 54/74 TTL.

The newer logic families have also alleviated the problem of static-charge breakdown, thanks to a dual-diode input-protection scheme. This protection method is the most widely used, but it's not a cure-all (for fast-rise transients, the internal diodes can't turn on rapidly enough). The best means of protection limits all input voltages to a level between the supply voltages.

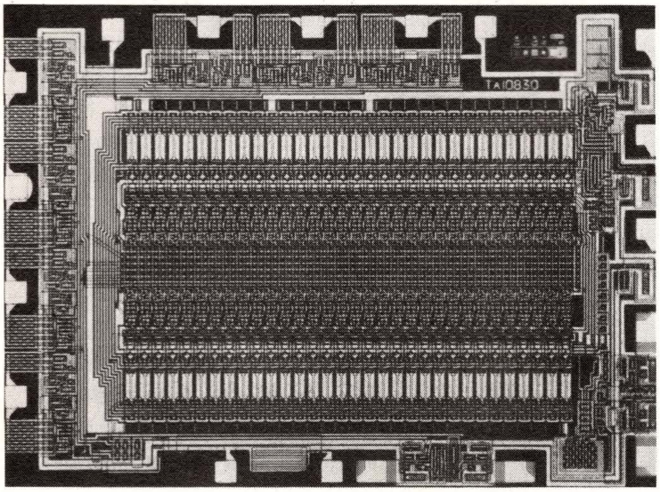
Another serious problem inherent in the CMOS structure comes from the SCR action of pnpn elements formed when n- and p-channel devices are fabricated on the same substrate and in close proximity. Once again, holding the inputs and outputs between V_{CC} and ground prevents latchup of this structure and subsequent device destruction. Manufacturers, however, usually employ design/process techniques to solve the problem. These fixes include wide geometric spacing, buried layers, guard rings, gold doping and bipolar-transistor shunts. In various combinations, these measures serve to reduce the product of the npn and pnp transistors' betas by reducing carrier lifetime, thereby preventing sufficient trigger current from reaching the SCR. The buried layer (possibly using an n epi on an n^+ substrate) reduces parasitic resistances to levels below those necessary to sustain SCR action.



Without appropriate protection measures, *the inherent pnpn structure in a CMOS device can easily go into an SCR-type mode and destroy the device. Keeping the beta product of the parasitic transistors less than 1 and shorting the parasitic resistors provides latchup-free operation.*

CMOS finds use in a staggering product array

and filters, modems, crosspoint switches and other telecomm devices, plus general-purpose logic. National also produces general-purpose logic, and most of its newer CMOS parts use the company's P²CMOS, a high-performance silicon-gate, selectively oxidized double-poly process typical of the type of processing that future generations of CMOS parts will employ. National uses it for the NSC800 μP family, some RAMs,



Heralding a move into telecommunications, *RCA Solid State's CA3300 6-bit latched flash A/D converter is produced with the company's SOS/CMOS process. It achieves sampling rates of 15 MHz with power consumption less than 200 mW from a 3 to 12V supply. Accuracy is within ±0.5 LSB, and pricing stands at $38 (1000) in ceramic.*

EPROMs (27C16) and a few logic functions that are upgrades of the old 74C family.

That family differed from RCA's 4000 logic components in that it was pin and function compatible with 74LS logic. Such compatibility is getting another go-around from several companies in addition to National, notably Mitel Semiconductor and Semi Processes Inc. Mitel introduced its oxide-isolated ISO-CMOS process about 3 yrs ago and has since added a second layer of poly to produce the ISO² CMOS process. It now produces gate arrays and other parts with 5-μm geometries but has presented papers recently on the performance of 2-μm scaled CMOS. And it's also using ISO² CMOS to produce 74LS-compatible logic functions, a few of which have begun to appear.

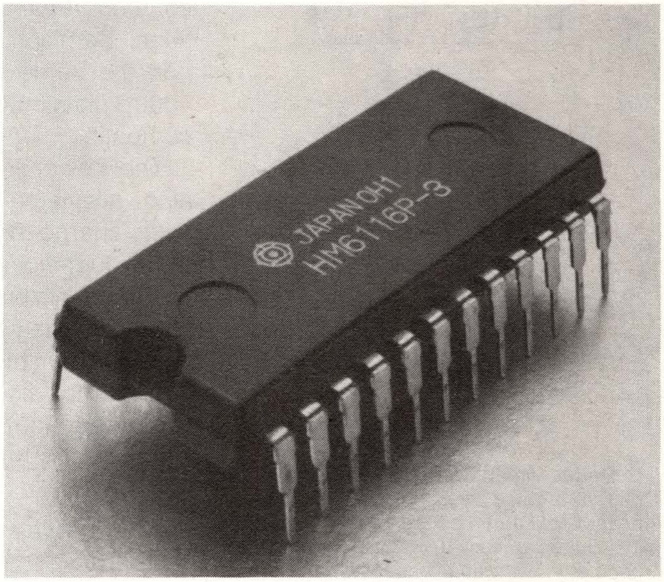
Meanwhile, Semi Processes announced the first 20 parts in its SP74SC product line, which employs a comparable silicon-gate process. Initial offerings include decoders, multiplexers, octal drivers, transceivers, flip flops and latches. Combined with its CMOS gate arrays, Semi Processes intends these parts to offer full systems breadboard capability with performance equaling or surpassing that of TTL.

Other companies you might expect to produce logic parts of this type are GTE Microcircuits and Plessey Semiconductor, both licensed second sources for the Mitel ISO-CMOS process.

Focusing on linear devices

Two of the smaller companies in CMOS, Holt and Nitron, have fine-tuned their metal-gate processes to produce a sophisticated real-time clock chip developed by Holt. A μP-bus-oriented interface on the HI8000 can handle multiplexed bus processors in the Intel and Motorola lines and can count up to 128 yrs with 15.3-μsec resolution. The device has three programmable prescalers, four buffered clock outputs and an alarm output. Leap-year compensation is automatic, and the part can operate in 12- or 24-hr modes.

Another smaller firm, Analog Systems also produces only a few CMOS devices, one of which is quite interesting from a linear standpoint. The MA-113 op-amp chip incorporates six independent high-performance op amps with 1-pA bias current, 25-MHz



A state-of-the-art 16k CMOS RAM, *Hitachi's 6116 utilizes 3-μm rules and a single-poly process that lets it achieve a 120- to 200-nsec access time. Its periphery is CMOS/bipolar with a core of NMOS cells; power to the poly loads goes through a buried-JFET structure in each cell. Active power dissipation is 200 mW, while full power-down drops that figure to 500 μW.*

gain-bandwidth product, 25V/μsec slew rate and 45-nsec settling time. It's very useful for breadboarding and is another example of the expansion of CMOS into the linear field.

Further proof of the inroads CMOS has made into linear circuitry is the announcement by Precision Monolithics, a staunch bipolar house, that it is developing an oxide-isolated silicon-gate CMOS process along with a dual-layer metal-gate process that it will use to combine linear and digital functions on gate arrays. One of the company's first products in CMOS will be an 8-bit successive-approximation register used in ADCs and DACs for shared-codec systems.

For Analog Devices, meanwhile, linear CMOS applications have been around a long time, and the company's experience allows it to produce some of the most advanced linear CMOS devices on the market. For example, one of its latest products is the AD7581, an 8-channel, 8-bit ADC with on-chip dual-port RAM that takes the software overhead out of μP data acquisition. Other complex chips available are the AD7555 4½- or 5½-bit BCD ADC, plus the 7525 monolithic pot.

Look for Analog Devices to introduce a 16-bit monolithic CMOS DAC with guaranteed monotonicity over temperature and the Stackdac, a 12-bit DAC incorporating a 6×12-bit FIFO register. Both devices will combine analog and digital functions on the same chip.

Rounding out the list of CMOS-device manufacturers is Hughes Aircraft's Solid State Products Div, which uses technology developed for military applications to produce a variety of μPs, including RCA's 1800 family and the only CMOS EEPROM on the market, the HNVM 3008. The latter device recently saw a price cut from $300 to $115 (100) on its way to a predicted price of $50 by year's end (EDN, January 21, pg 37). In line with Hughes's nonvolatile-device effort, a CMOS version of Xicor's (Sunnyvale, CA) shadow RAM is also in

Varieties of CMOS

Three main categories of CMOS are in production today: junction isolated, oxide isolated and silicon on sapphire. Within these categories, there are many variations in manufacturing details, such as gate-material type, method of achieving isolation and substrate-material type.

The earlier forms of CMOS used n^+ and p^+ diffusions between the n- and p-type devices to achieve isolation and increase usable supply voltage. This method still serves in SSI, MSI and some LSI circuitry, but the spacings required between guard rings and from guard rings to transistors preclude high-density designs. If a design uses metal gates, these, too, must be isolated and must also overlap the source/drain regions, giving rise to capacitances that slow device operation. Thus, to improve the performance of their processes, manufacturers have devised a variety of solutions now in common use, and more techniques appear every year.

One of the first steps taken involved the use of polysilicon for the gate material. This procedure produced smaller and faster self-aligned structures and a second level of interconnect to boot. Another density improver, used notably in RCA's LOVAG (low-voltage aluminum-gate) process, eliminates the spacing between guard rings and the source/drain diffusions. This provision forms an n^+ p^+ zener diode with a breakdown of approximately 6 to 8V, so the process is only good for products operating at or below 5V. It also sacrifices speed.

The density-improvement technique now receiving the most attention is oxide isolation in any of its various forms. The original idea was to create a thick field oxide over the regions between switching devices, forming an FET with a threshold voltage much higher than that of those switching devices: The FET is effectively OFF at operating-signal levels. The problem with this approach is that large oxide steps cause coverage problems. The solution is a process termed selective oxidation, in which nitride masking selectively oxidizes the field oxide below the silicon surface, producing physical separation as well as a thick-oxide guard FET. Additionally, a field implant under the field oxide can adjust surface concentrations. The basic process has various names, including Fairchild's Isoplanar C, Mitel's ISO² CMOS, Intersil's Selox-C and National's P²CMOS, but the folks at Integrated Circuit Engineering (Scottsdale, AZ) prefer the term SOCMOS (selectively oxidized CMOS), which gets away from company designations.

Another variable in CMOS production involves the choice of starting-substrate material. Classic CMOS uses an n^- substrate into which p^- wells or tubs are implanted; this is the technique used by the old-line CMOS manufacturers. However, several other approaches are under development, notably an n^--well process that Intel terms CHMOS and is touting as the best way for NMOS manufacturers to get into CMOS production. As the name implies, the process is compatible with HMOS processing, and Intel claims it provides an edge in building CMOS EPROMs. Other manufacturers obviously agree: Matsushita has built a 64k static RAM with n-well (*ISSCC Digest,* 1980, pg 236), Honeywell says it has built submicron CMOS in the lab using an n-well process, and other companies, such as Mitel, are known to be investigating n-well applications. P-well advocates, however, contend that the n-well process exhibits some basic disadvantages that will force these companies to develop p-well devices except for certain special applications.

Meanwhile, research into new CMOS approaches continues. Researchers at Bell Laboratories (Murray Hill, NJ) noticed that scaling of p-well CMOS caused degraded n-channel-transistor performance due to increased well doping, which adds source/drain-to-p-tub capacitance. Their solution is an 8-mask process, Twin-Tub, in which separate n and p tubs optimize the performance of both device types. The process is latchup proof, uses 2-μm channels and no guard rings, operates down to 2V and can be easily shrunk.

Japanese firms compete strongly in CMOS designs

development and should be ready for sampling in the second half of this year.

The verdict isn't in yet

The reasons for using CMOS in LSI and denser device designs during the '80s all seem compelling, and the list of parts available from CMOS manufacturers is impressive. But some questions remain. CMOS has always been a more expensive process, thanks to the large number of masks it requires compared with NMOS. However, note that NMOS has steadily been adding mask levels to achieve its high performance without burning up. Thus, CMOS manufacturers are now claiming parity with regard to mask levels, and that means costs are converging.

With respect to die area, process complexity and yield, CMOS has also been an expensive technology, but it's getting cheaper; conversely, NMOS was a cheap process and is getting more costly. In fact, many observers feel that NMOS has run out of gas while CMOS is just starting with a full tank, but of course that's not really the case: Manufacturers are constantly inventing new forms of each technology, and which process will eventually dominate is anyone's guess. Thus, despite CMOS's many advantages, you can't rule out *any* process because researchers keep producing improvements that eliminate old problems.

Indeed, several promising methods for improving CMOS density are under investigation. Toshiba, for example, is evaluating a variable-resistance polysilicon load for a CMOS RAM cell that allows a 6-transistor static cell to occupy no more space than a poly-load cell. This polysilicon transistor load (PTL) is controlled by a buried n^+ gate and can be fabricated as either an n- or p-channel structure.

Two other approaches to CMOS improvement use 3-dimensional cell structures that stack MOS transis-

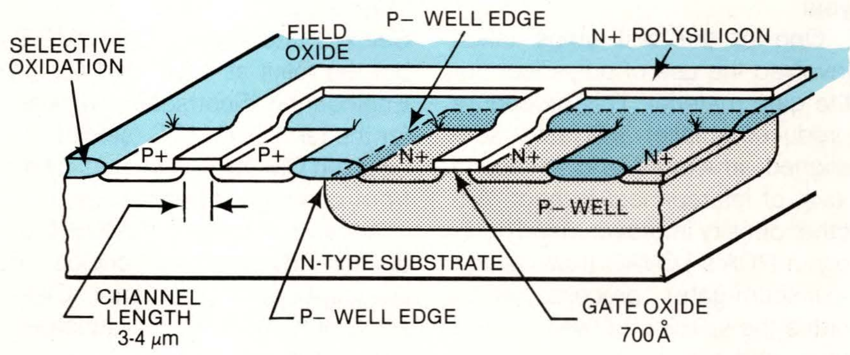
Is SOS/CMOS still viable?

Is it time to again sound the death knell of silicon-on-sapphire (SOS), or will the needs of VLSI keep this CMOS process alive and viable? The debate has long raged between bulk-silicon advocates and those in the SOS camp. In the long run, though, a new technology might displace both.

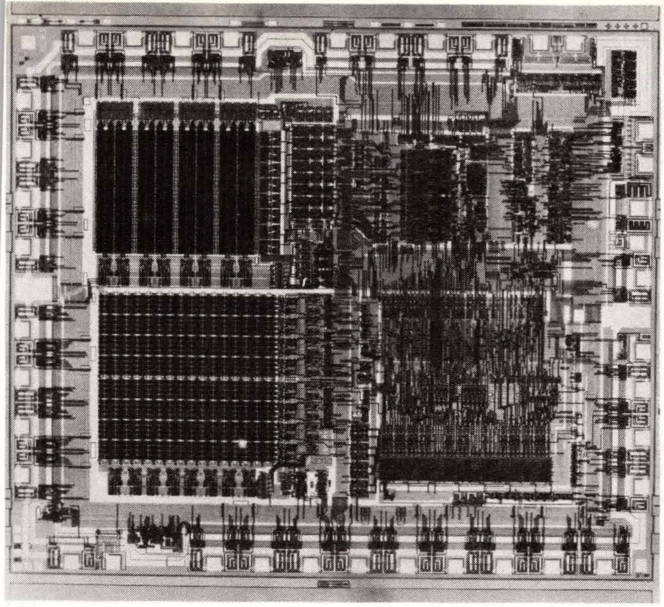
The nice thing about CMOS fabricated on an SOS substrate is the process's retention of all CMOS advantages—low power dissipation, high noise immunity, wide operating voltages and wide temperature range—with the addition of a few more. Claimed additional advantages include higher density, faster speeds, lower power, higher yields, freedom from latchup, easier design, three available levels of interconnect and better radiation hardness. Bulk-silicon backers take issue with many of these claims and assert that bulk-processing techniques now under development achieve the same advantages.

For instance, with regard to density, SOS's processing eliminates the guard rings separating different devices, thereby allowing much closer spacing. But bulk CMOS can achieve nearly the same density using selective-oxidation and field-doping techniques, while the Twin-Tub approach developed at Bell Labs eliminates channel stops and optimizes each transistor type in its own well. The SOS speed and power-dissipation claims hinge on the lower levels of internal capacitance gained by use of the sapphire substrate. In particular, wiring and drain/source-to-substrate capacitances are lower than in bulk devices. In reply, however, SOCMOS (selectively oxidized CMOS) boosters claim reduced substrate capacitance—mainly in the sidewall—and point out that in scaled devices with metal lines as narrow as 1 μm and close spacing, the sapphire substrate aids capacitive fringing-field interaction between metal bus lines. They also claim that in addition to a strain-induced reduction of carrier mobility in the epi layer, SOS suffers speed loss when used in VLSI circuits. As for higher yields, bulk-silicon advocates observe that although SOS's fewer processing steps and freedom from oxide-pinhole problems over the sapphire should theoretically increase yields, in practice that doesn't seem to be the case.

Freedom from latchup is also possible in bulk CMOS through



A selectively oxidized CMOS (SOCMOS) structure *reduces substrate capacitance and provides an alternative to SOS/CMOS designs.*



CMOS microprocessors, *such as this TCP8049C from Toshiba, are appearing in increasing numbers.*

tors atop one another. The single-device-well (SDW) approach developed at the University of Waterloo (Ontario, Canada) and Bell-Northern Research (Ottawa) merges a surface-enhancement-type device perpendicular to but in the same well with a buried depletion-mode device. This technique only works with technologies that permit lightly doped wells (usually CMOS) and offers extremely dense structures and improved alpha-particle resistance. The second approach comes from Dr J Gibbons and K Lee of Stanford's (Palo Alto, CA) Solid State Electronics Lab. Termed JMOS, the technique uses a single (joint) gate to control a bulk-silicon p channel and a laser-recrystallized polysilicon n channel in the form of a vertically integrated CMOS inverter. The techniques involved are similar to those used in fabricating silicon-on-insulator (SOI) devices, so progress in one field will apply to the other.

Of course, discoveries such as these can also occur in any other processing technology and thereby shift the balance of desirability to that technology and away

the use of n-epi-on-n^+ substrate material and careful layout of I/O circuits. Each side claims easier design through superior predictability in modeling, and experimentation at Sandia Labs (Albuquerque, NM) has shown that properly processed silicon-gate CMOS has radiation tolerance comparable to that of SOS with regard to total gamma dosages. (In fact, recent ads by National Semiconductor say its radiation-hard metal-gate CMOS can withstand as much as 10^6 rads—two orders of magnitude higher than traditional CMOS.)

Bulk-CMOS manufacturers go on to point out that VLSI, the very level of integration that's supposed to save SOS, could in fact be its downfall. Specifically, the lower surface-channel mobility resulting from the lattice and thermal-expansion mismatch between sapphire and its silicion epi layer becomes aggravated as the epi layer is scaled. Researchers have observed defects extending from the silicon/sapphire interface as much as 4 μm into the epi layer—a thickness below which the epi might have to be scaled for VLSI use. Defects at the interface also cause higher leakage when combined with the higher carrier lifetimes experienced in the epi layer.

But even putting these problems aside, the big killer for SOS always was and still remains high cost. Sapphire substrates cost four to seven times as much as comparably sized silicon substrates, and despite 15 yrs of effort by manufacturers such as RCA, the differential remains.

RCA, while not giving up on SOS technology, has stopped trying to use it for every product type. And Hewlett-Packard (Palo Alto, CA) has also scaled down its use of SOS. Furthermore, most of the other manufacturers (Rockwell International and Hughes Aircraft, for example) use SOS only for aerospace/military applications. However, at least two Japanese companies (NEC and Toshiba) are convinced of the viability of SOS/CMOS and are pursuing commercial development.

In the long run, both of these technologies might succumb to a newly developed process that combines the best features of both. This new process, termed silicon on insulator (SOI), utilizes a silicon-oxide insulator rather than a sapphire one. Primarily under development by Texas Instruments, the process employs a thin (1 μm) oxide insulating layer placed on a silicon substrate, with a layer of polycrystalline silicon deposited on top. The poly is then recrystallized with a laser to form a single crystal for fabrication.

The process has many advanges compared with SOS. It's silicon based and should be low in cost and high yielding. Additionally, it solves many of the problems of SOS. Surface mobility approaches that of bulk silicon while retaining the isolating-island approach of SOS. The silicon/oxide interface is stable and defect free and can easily serve for device fabrication (although mobility is lower). And because the interface is defect free, the poly layer can be scaled to VLSI dimensions without problems, and the thin oxide allows the substrate to act as a ground plane so that fringing effects from metal runs are strongly reduced.

Although more work remains—particularly in the area of grain orientation—SOI/CMOS could overtake not only SOS but bulk CMOS as well before the decade is over.

from CMOS. But regardless of such potential shifts, CMOS, thanks to its versatile combination of attributes, will be on stage for the '80s and possibly far beyond. EDN

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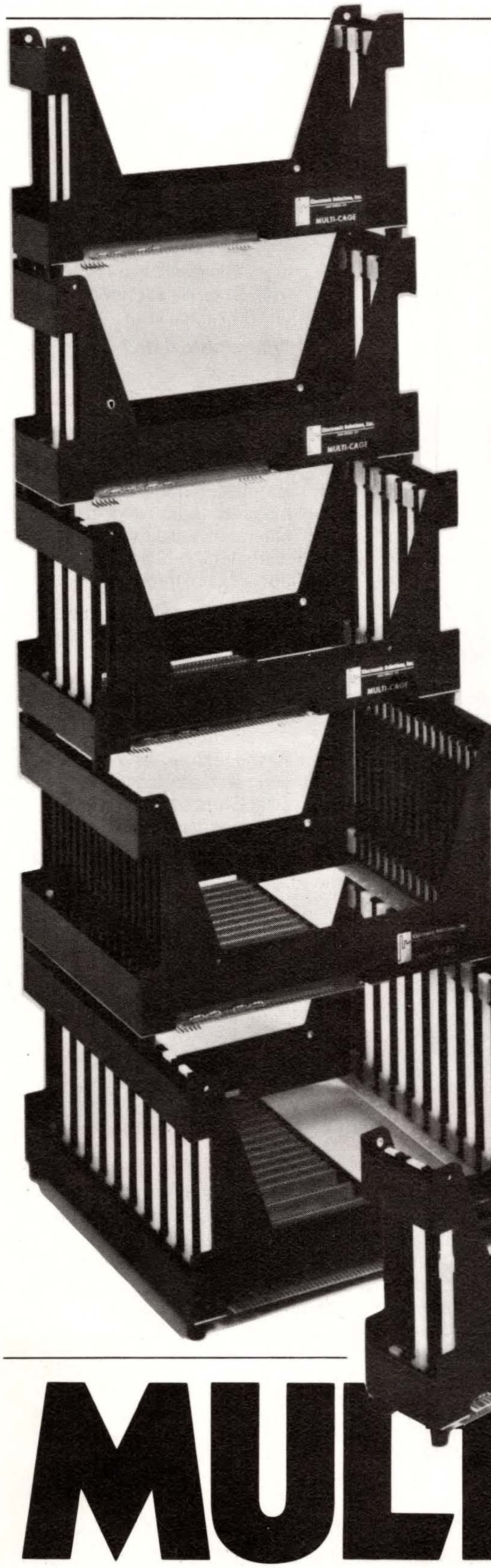

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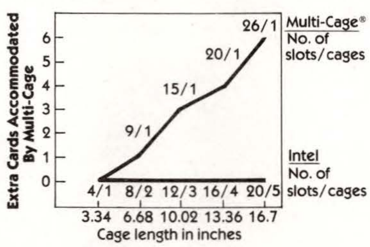

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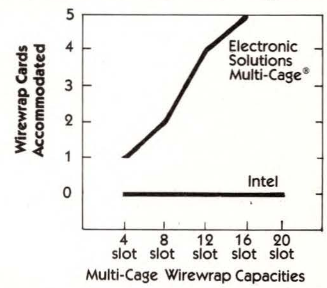

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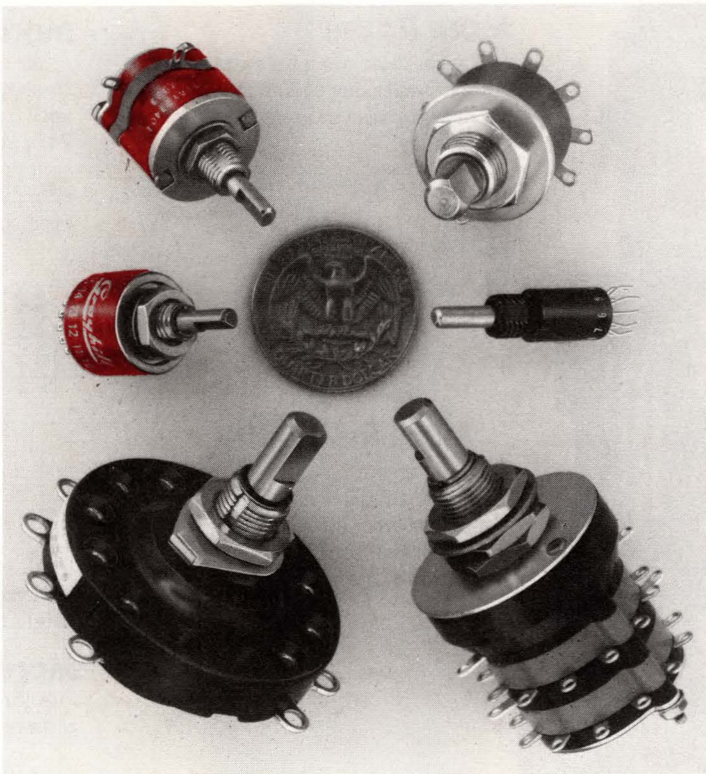

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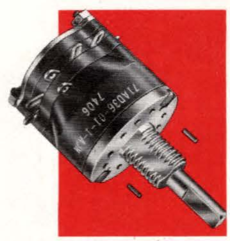

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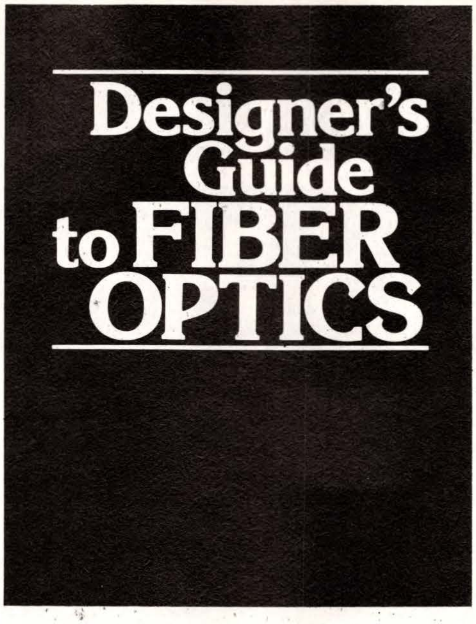

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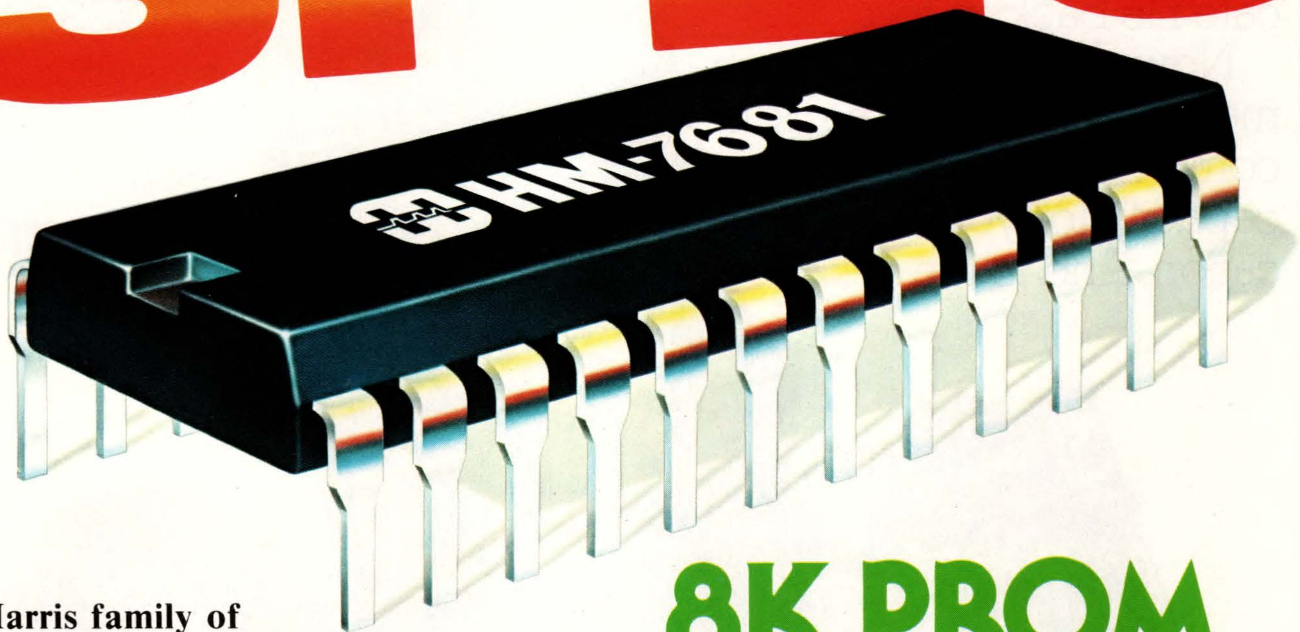

8K PROM

Harris family of bipolar 8K PROMs...

PART TYPE	PINS	FORMAT	SPEED	ICC	ICCPD (1)
			STANDARD		
HM-7681	24	1K x 8	70nsec	170mA	—
HM-7608	24	1K x 8	70nsec	170mA	—
HM-7685	18	2K x 4	70nsec	170mA	—
			HIGH SPEED		
HM-7681A (2)	24	1K x 8	50nsec	170mA	—
HM-7685A	18	2K x 4	55nsec	170mA	—
			POWER DOWN		
HM-7681P	24	1K x 8	70nsec	170mA	55mA
HM-7681RP	24	1K x 8	70nsec	170mA	60mA
HM-7685P	18	2K x 4	70nsec	170mA	40mA
			LATCHED OUTPUTS		
HM-7681R	24	1K x 8	70nsec	170mA	—
			REGISTERED		
HM-7681S (2)	24	1K x 8	70nsec	215mA	—

(1) ICC during the power down mode
(2) Available in .600" or .300" Cerdip

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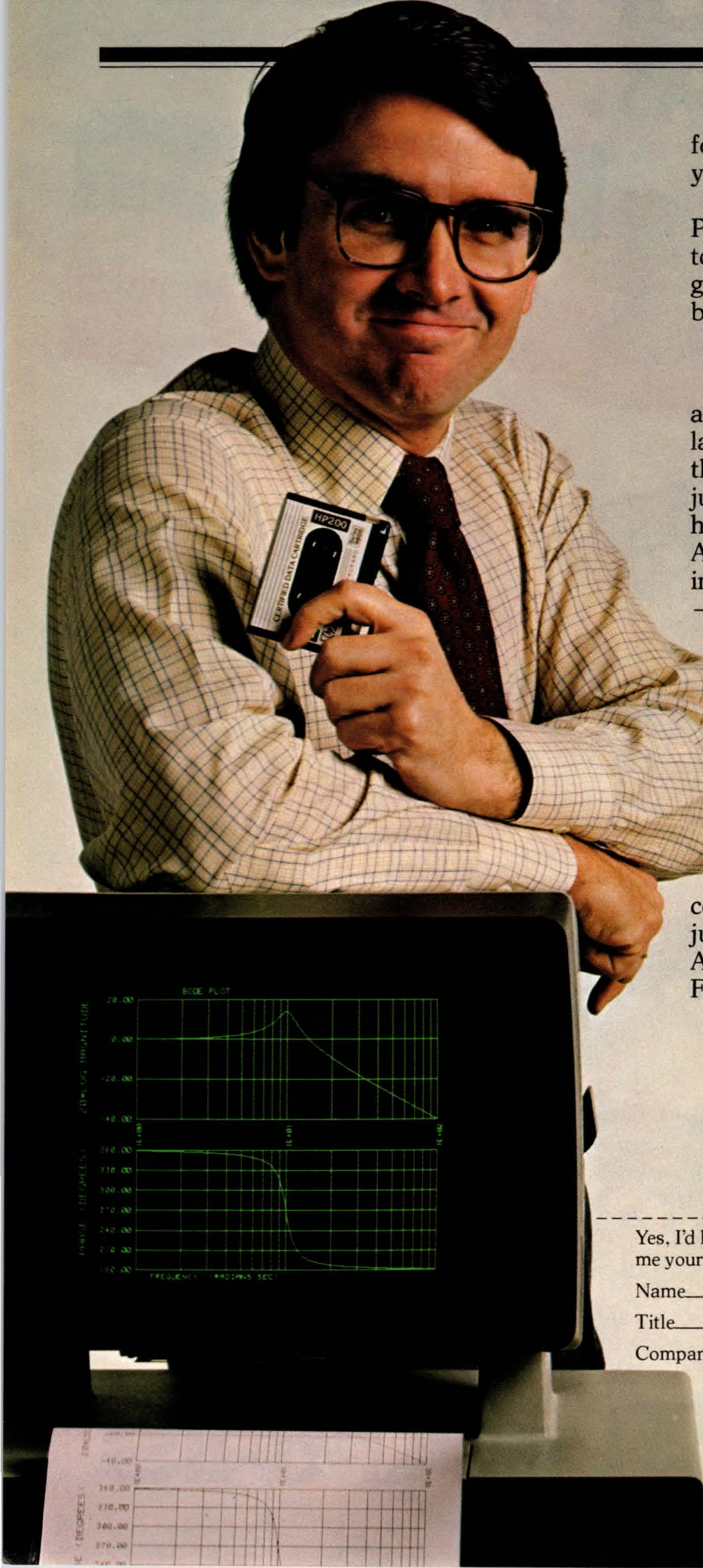

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Current-mirror ICs aid in current handling

A circuit's varying load currents won't affect its input-signal source if you use current mirrors to isolate the circuit's input from its output.

Dale Pippenger, Texas Instruments Inc

When your design's varying load current reflects back to the circuit's input and upsets the signal source, you can deal with the problem in two ways: insert an overly complex buffer-amplifier design into the middle of the troublesome circuit, or head off problems by employing current mirrors.

Current mirrors (see **box,** "Mirrors that don't reflect") are rather like 1-way streets: The output current follows the input current, but whatever happens to the output current doesn't reflect back to the input. Output-to-input isolation of 80 dB is typical.

These unusual devices lend themselves to solving unusual—as well as everyday—circuit-design challenges. Three application examples show how they can benefit your next design.

Locate a robot's hand

The first application involves motion and position sensing, commonly required functions in today's automated world. Whether your design must direct an industrial robot's "hand" or steer a radio telescope, you must solve the same problem: You have to find where an object is before you can control it.

The position sensor shown in **Fig 1** employs four types of current-mirror ICs to directly generate a 4-bit binary-weighted output current that's proportional to 16 different positions. (Note that although **Fig 1** depicts a linear motion-sensing plate, you can employ a suitably

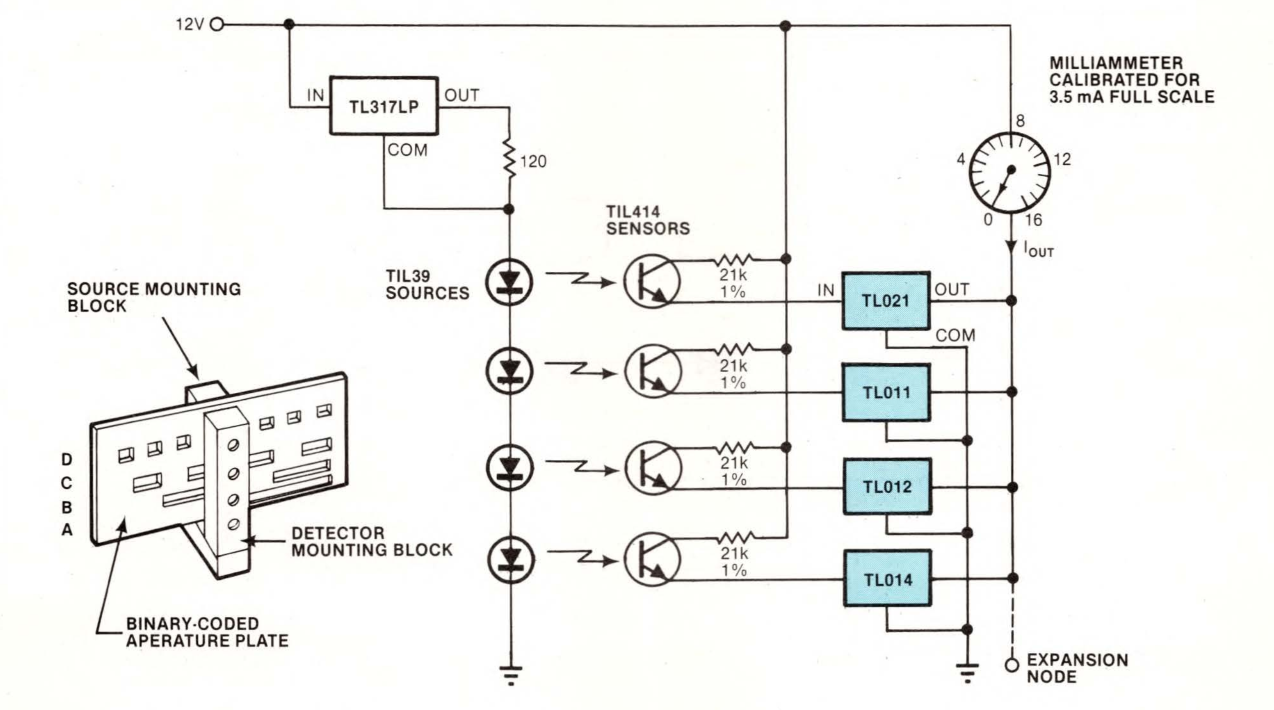


Fig 1—Digital-to-analog position data *becomes available when sensors are illuminated through an aperture plate's windows in this circuit. Binary scaling occurs due to the current mirrors' differing transform ratios. ORing the mirrors' outputs yields a 16-step analog output value equal to the 4-bit position data.*

Current mirrors' differing ratios help detect position

encoded rotating disk for angle measurements.) Current mirrors with four different input-to-output current-transform ratios furnish the key to this design's simplicity.

By using the TL317 as a constant-current source, you achieve a relatively uniform output from the sensor-source LEDs despite power-supply variations. Thus, the TIL414 photosensors always output the same ~0.5-mA current level when turned on via a window in the aperture plate. (But note that not only is careful source-to-sensor alignment necessary, you must also ensure that stray (ambient) light can't falsely trigger a sensor.)

The TL021 current mirror transforms the input current to output current according to a 2:1 ratio. Hence, the LSB output equals ~0.25 mA. Similarly, the MSB equals ~2.0 mA due to the TL014's 1:4 ratio. You sum all the stages' currents by wire-ORing the current mirrors' outputs and sinking the result through a suitably calibrated milliammeter.

Because the current mirrors achieve a 60-dB min dynamic range, you can easily increase the number of sensed positions. For example, if you want to resolve 256 positions, add one more of each device type, put the extra LEDs in series with the existing ones and wire-OR a similar sequence of current mirrors into the meter circuit. However, you must adjust the additional sensors—via their collector resistors—to operate at an output current of 31.25 μA to obtain the correct binary scaling.

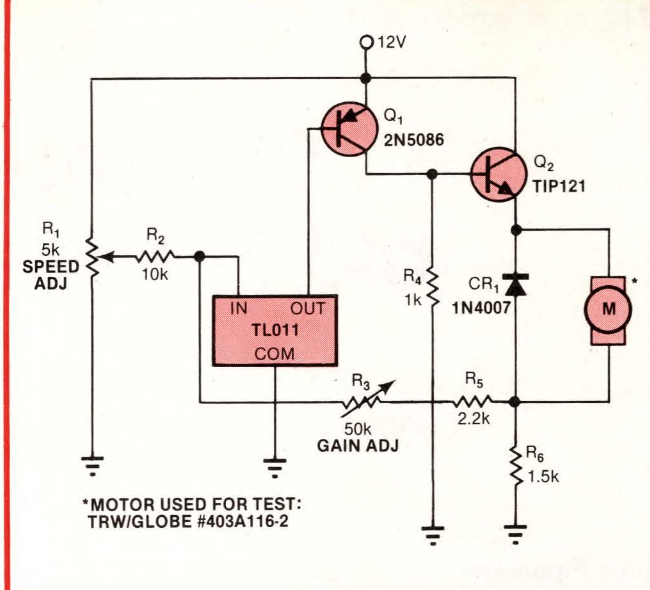


Fig 2—Constant motor speed *results when the current mirror sums current analogs of the motor's desired and actual speeds. This IC's output current in turn servos the transistors' operating levels until the motor's input power just balances its load requirement.*

Keep your motor on speed

Current mirrors can also help govern a motor's speed. Accurately maintaining a small dc motor's speed over widely varying shaft loads without current mirrors often results in an overly complex controller design. But not only does the technique presented in **Fig 2** solve a small motor's speed-control problem easily and simply, it also allows you to extend the concept to higher powered applications.

To maintain a motor's speed as its shaft loading increases, you must increase its deliverable torque by

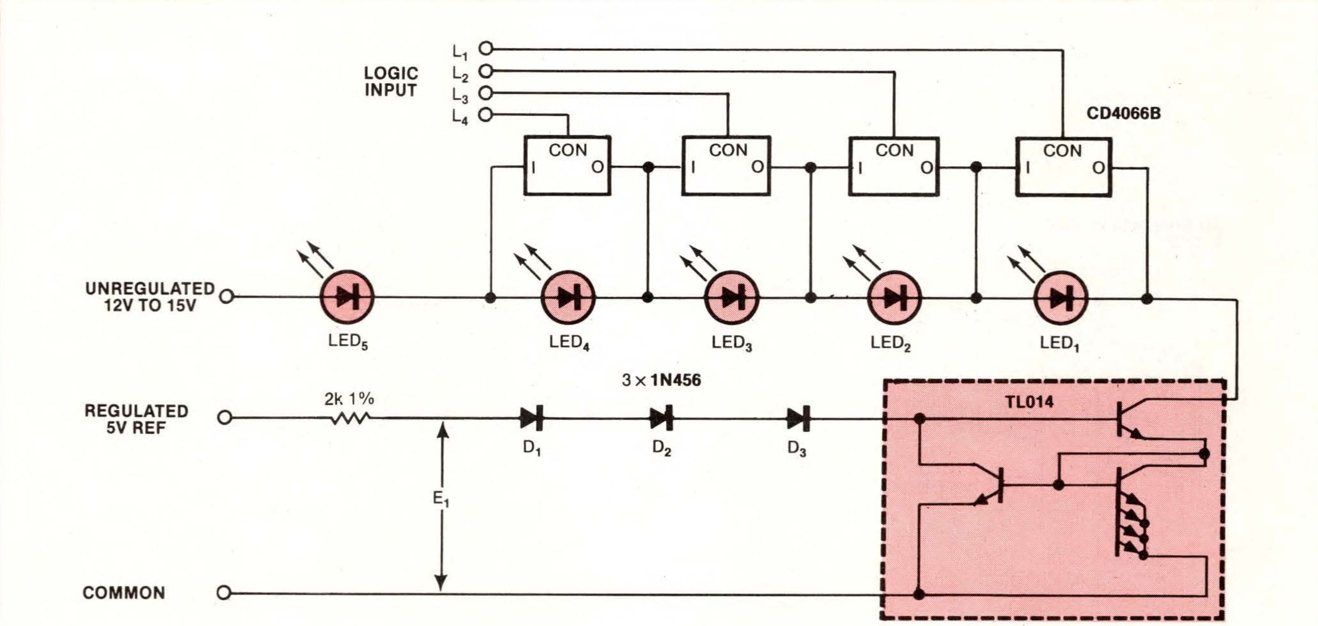


Fig 3—The LEDs' light output remains constant *whether only one of them (LED_5) is ON or any or all of the others are also ON. Constant LED brightness is assured over a wide temperature range due to the 3-diode/current-mirror network's tracking characteristics. You turn the LEDs on or off by logically driving the CD4066B lamp-shunting CMOS switches.*

raising the electrical power into the motor. This design accomplishes the task by sensing the motor's operating current and error-summing it with a set-voltage-derived current.

At start-up, R_2 converts the voltage determined by R_1's setting into the current mirror's input current. (Note that at this instant, no current yet flows through the motor and thus there's no feedback.) The current mirror's 1:1 transform ratio provides an equal current level that serves as Q_1's drive. Q_1's current gain (β) and inversion in turn serve to drive emitter follower Q_2 ON. This action starts current flowing into the motor and through R_6.

The resulting IR_6 voltage is converted to a current by the R_3/R_5 combination and summed with the speed-setting current at the mirror's input. The result? A closed-loop servo: When the motor's shaft load increases, for example, the circuit supplies the resulting higher motor-current demands until the servo balances. To achieve a stable loop gain, adjust R_3.

Light your LEDs equally

Another current-mirror application demonstrates the devices' talents for lighting LEDs. Normally, trying to maintain a constant and tracking output from randomly switched LEDs over a temperature range is tricky. Using a conventional one-driver-per-LED approach, you must first individually adjust each driver/LED stage to match output intensities. And then, because an LED's output decreases with increasing temperature, you have to temperature-compensate everything to maintain a constant intensity level.

Mirrors that don't reflect

Current mirrors provide an output current that's a true reflection of their input current. However, changes in the circuit's output load current don't reflect back to the input port. Devices with forward (input-to-output) current-transfer ratios of 1:1, 1:2, 1:4 and 2:1 are available from Texas Instruments; the reverse (output-to-input) isolation for all devices exceeds 80 dB.

Fig A shows how a basic 1:1 Wilson current mirror functions. The device consists of three transistors (npn types in this case) connected in a closed loop. The output current is thus clamped at a value exactly equal to the input current. Because the current mirror is monolithic, Q_2's V_{BE} exactly tracks Q_3's V_{BE}. Hence, they both operate at exactly the same current levels, ensuring that Q_1's base current (I_{BE}) is exactly compensated. Additionally, I_O equals I_{IN}.

To understand how this scheme provides other I_O/I_{IN} options, consider **Fig B**'s configuration. Here, the same current-distribution rules apply, except that now four devices are in the feedback loop and therefore the input-to-output current-transform ratio is 1:4.

In all these designs, the circuit's apparent output impedance varies inversely with the output current. For example, at $I_O=100$ μA, Z_O is greater than 10 MΩ, and at $I_O=10$ μA, Z_O is greater than 100 MΩ.

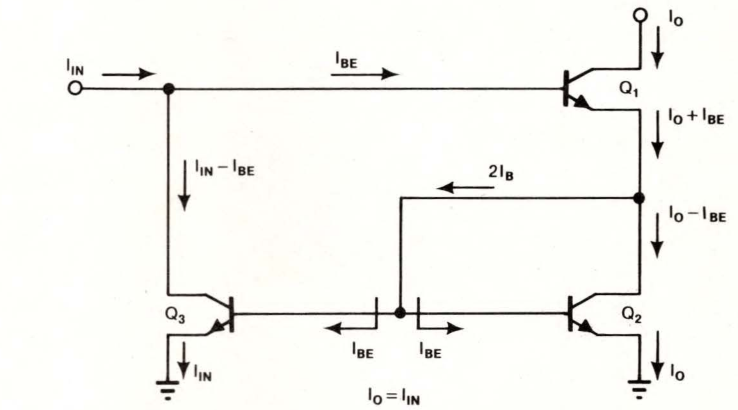


Fig A—A 1:1 forward current-transform ratio *occurs in the TL011 current mirror because Q_2 and Q_3 exactly split and control the device's input signal. And because the device's output derives from a transistor's collector, its reverse isolation exceeds 80 dB.*

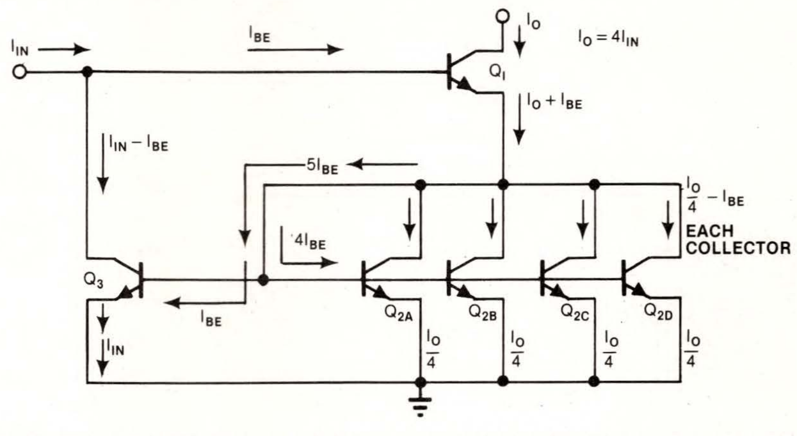


Fig B—Extending Fig A's concept by four steps *yields a TL014 current mirror, whose output is exactly four times its input. But even with an input-to-output ratio of 1:1 or 1:4 (or anything in between), Q_1's output impedance would still be inversely proportional to I_O. Note that by making Q_2 a single transistor and Q_3 a double one, you can achieve a 2:1 ratio.*

TL011, -12 and -14 current mirrors operate at input currents to 1 mA; the TL021, up to 2 mA. All types handle output voltages to 35V. Prices for all versions range from \$0.26 to \$0.37 (100) for units with -CLP specs.

For a data sheet on the TL current-mirror family, **Circle No 449.**

One temperature-compensated current mirror drives LEDs

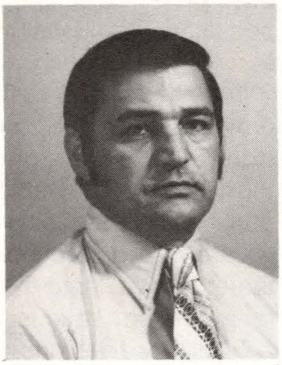
Fig 3's design circumvents these problems by driving several LEDs with a single temperature-compensated current source. Although this circuit leaves one LED (LED_5) ON continuously and allows the others to switch randomly, you can adapt the design to your needs.

Connecting the LEDs in series and employing the current mirror as a settable constant-current LED driver automatically ensures that each device sees the same ON current. You accomplish the selective turn-off function by shunting the chosen LED with a logically driven CMOS switch. Thus, so long as the LEDs' intensity tracks over a limited drive-current range, you can meet the matched-output requirement at a constant ambient temperature.

Note, however, that at a constant input current, an LED's light output decreases with increasing temperature. The circuit compensates for this temperature effect by combining characteristics inherent in both the current mirror and diodes D_1 through D_3.

To understand how this compensation works, first consider the current mirror's internal configuration. The current mirror's input appears as two diodes in series. Hence, the diodes have a forward voltage drop of 1.4V at 1 mA and 25°C; their temperature coefficient is -3.5 mV/°C. Adding the three series diodes (D_1 through D_3) brings the input's voltage drop to approximately 3.5V at 1 mA and 25°C and the temperature coefficient to -8.75 mV/°C. Working in conjunction with these parts, the 2-kΩ resistor converts the regulated 5V input to a temperature-controlled variable current into the current mirror. The result? At 25°C, the current mirror multiplies the ~750-μA input to a 3-mA output level; at 75°C, these values become 950 μA and 3.8 mA, respectively. And they're exactly what's required to maintain the LEDs' output at a constant intensity. Note, however, that all the devices must share the same thermal environment to guarantee accurate tracking. **EDN**

Author's biography



Dale Pippenger, section manager for Texas Instruments' (Dallas) Linear Applications Group, joined the firm in 1957. His design experience includes power-system controls and TV applications. Additionally, he has spent several years in consumer marketing and product applications. Dale received his BS (math) from Memphis State University and his MSEE from SMU, Dallas. A prolific writer, he has coauthored two books, many papers for leading electronics publications and a videotape series on op amps.

DP Dialogue

Notes and observations from the IBM Data Processing Division that may prove of interest to the engineering community

Demonstration of a Biomation logic analyzer. IBM's COPICS helps the Gould Inc. division assemble electronic instruments like this at much lower costs.

At Biomation, An Assembly Line With a Steady Pulse

Today, assembly lines at the Biomation Division of Gould Incorporated almost always flow smoothly, with never a threatened stop to production because of missing parts.

"We used to operate with 130 days of inventory on hand," says Robert Nazarenus, vice president, finance.

"We've cut that down to between 85 and 95 days. And on expensive parts, we time our orders so the items arrive just when we need them. We use less space for storage, and we don't buy and hold them before they are needed.

"At the same time, we've cut work-in-process time in half: from 24 weeks to 12 or 13."

Biomation's line of high-performance waveform recorders and logic analyzers is a materials-intensive business, Nazarenus continues. About 70 percent of the cost of a completed instrument is in the parts. To minimize the costs of lost production and out-of-balance inventory, the Santa Clara, California, division installed IBM's Communications Oriented Production Information and Control System (COPICS) in a 4331 Processor.

"Now that we can plan manufacturing," Nazarenus notes, "we can enter into long-term contracts with component manufacturers. Before we had COPICS, 50 percent of our purchase orders were for delivery in one or two days—which meant that we were buying from distributors, at 20 to 40 percent more than we would have paid the manufacturers."

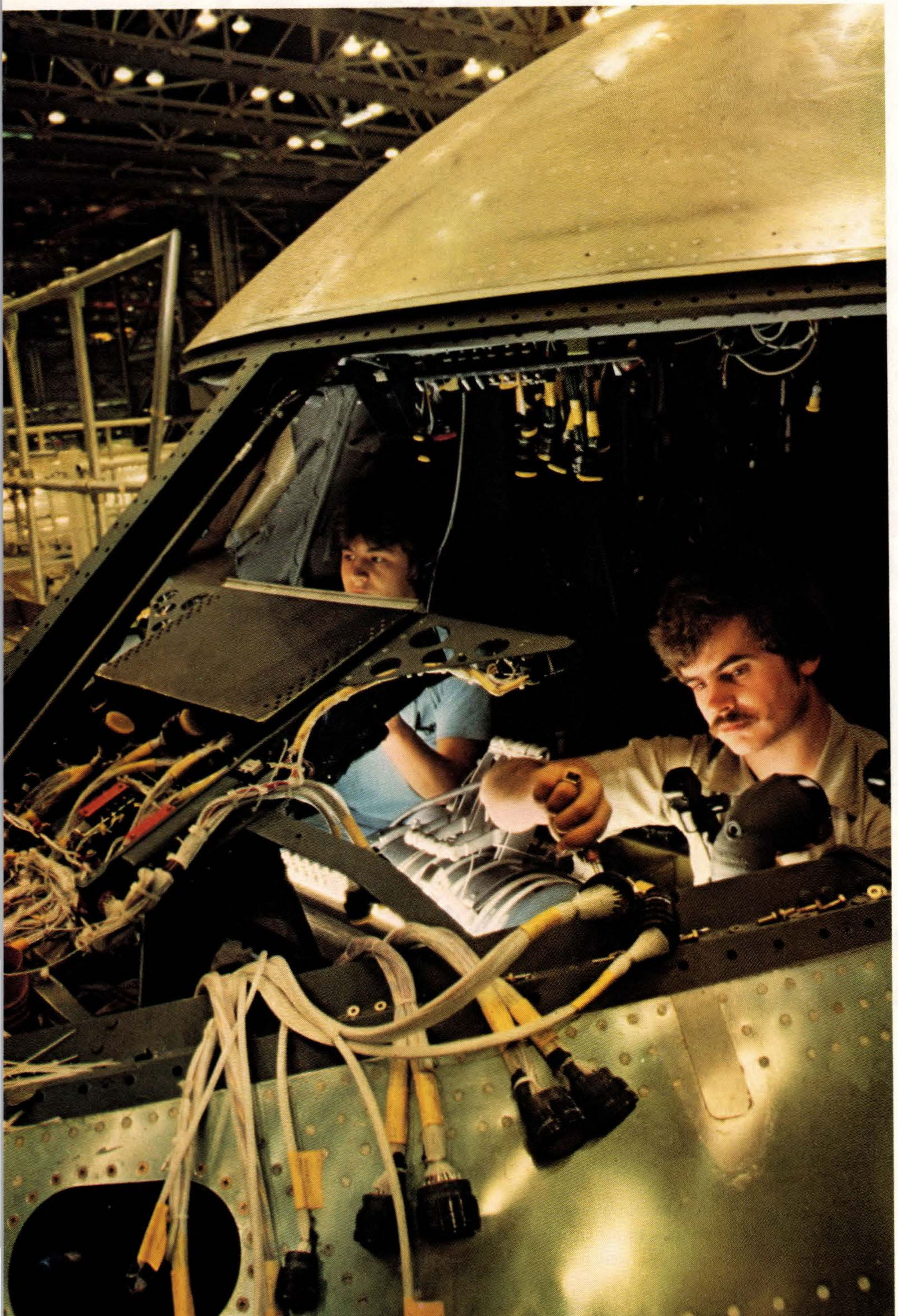
COPICS is a complete online system for control of manufacturing, with modules for material requirements planning, inventory accounting, shop floor routing control and other specific tasks. At Biomation, the first module to be installed was the bill of materials processor.

"There are 2,000 parts in a typical Biomation product, and frequent engineering changes to most models," Nazarenus explains. "So our bills of materials often contained errors. Since purchasing is done from the b/m's, this meant shortages of needed parts and purchases of unneeded ones. And expensive, high-level people spent a great deal of time running around looking for materials.

"With COPICS, we achieved a 100-percent-accurate manufacturing document, and then a time-phased bill of materials to take account of engineering changes. With that and a valid master schedule, we were able to begin material requirements planning (MRP) using COPICS, letting us schedule vendor shipments to coincide with need.

"This mode of operation is profitable," Nazarenus points out. "Putting out brush fires was not."

WIRS Wraps up 747 Wiring in a Neat Bundle



A Boeing 747 jumbo jet contains two tons of copper wire: 49,000 separate segments. Keeping track of the details of this massive electrical system requires the services of a large IBM computer.

As a jet airliner is designed and built the details of its electrical system undergo constant change. For the 747 jumbo jet Boeing Commercial Airplane Company uses a computer to keep track of each piece of wire.

Since there are extensive wiring differences for different customers, and even among individual planes, Boeing uses an interactive computer system, permitting changes and variations to be entered immediately, as they arise, and allowing engineering and manufacturing people to stay abreast of the configuration for each plane.

Running on an IBM 3033 Processor in Kent, Washington, the Wire Information and Release System (WIRS) stores the identity of each of 49,000 segments of wire in a 747, and its assignment to a bundle Robert M. Beers, functional manager, WIRS explains. Through the design, release, and fabrication of the bundle, WIRS identifies the device or connector at each end of the segment, the wire type and gauge, and the aircraft to which it applies. Data is added or changed by filling in blanks on the screen of a terminal in one of five Seattle-area plants or the plant in Wichita, Kansas.

During an average week, 500 engineering change notices are entered against the wiring of the 747, affecting one plane, all of them, or a limited number. For each entry WIRS performs 38 engineering edits which identify such errors as two wires using the same pin or the same wire number, release sequence errors, or connectors that don't match. Other automatic checks catch invalid wire codes, aircraft effectivity errors and the like. "By catching errors before they get into the system," Beers points out, "we cut the total number of basic changes to be processed by 25 percent. And we accomplish more of them in sequence, without reworking a completed bundle."

WIRS was built on the Information Management System/Virtual Storage (IMS/VS), an IBM data-base management program product. "IMS lets us access a wire or bundle in many ways," says Beers. "Engineers can look at a particular bundle or equipment item, or look for all wire of one type. They can go in by airplane number, change number, or by customer. Since a complete history is retained, they can look at past configurations, and see when a change was made.

"Today, we roll out seven 747's a month," Beers continues, "for any of 64 different customers. Since there is less lead time on wiring than on any other part of the design, we couldn't sustain that production rate without such a system."

Engine Development Revs up With Low-Cost Online Simulation

Online computer simulation at an af-
ɔrdable price has helped Mechanical Tech-
ology Incorporated reach its goal of becom-
ıg the U.S. leader in the technology of
tirling Cycle engines. Based in Latham,
lew York, near Albany, the company re-
ently installed an IBM 4341 Processor and
ngineers can now interact directly with a
etailed computer model of the engine,
ırough IBM visual display terminals.

"Compared to our previous use of out-
ide services for computing, we've lowered
ur costs while gaining important capabili-
ies," says Don Castor, manager of the data
rocessing center. "For example, if we want
ɔ modify the model, it's now very simple to
nter and test the change ourselves.

"The 4341 allows us to distribute termi-
als to all the people who need them. It has
laced interactive computing within
ur means for the first time."

The Stirling Cycle engine is a
60-year-old invention that Me-
hanical Technology is develop-
ng for practical modern use.
The kinematic engine has
exciting potential for auto-
notive power, and the
ree-piston Stirling
as a wide range of
pplications. The com-
any has already
ested baseline Stirl-
ng engines installed in
hree modified passenger
ars. A newly designed au-
omotive Stirling engine will be
vailable for testing shortly.

Development of the engine to
ts full potential is a formidable
challenge, explains Roy Krasse,
manager of administration, Stirl-
ing Engine Systems Division.
"With many variables to manipu-
late, we would like to build and
test 200 automotive engines; ac-
tually we'll test eleven. As an alternative, we use computer simulation."

Each user enters test variables through one of 23 IBM 3278 Visual Display Stations, and sees the results of the simulation on the screen in seconds. "An engineer can change a parameter and rerun the simulation immediately," Krasse says. "He has better control —he doesn't interrupt his train of thought. The model, or any other engineering program, is available online. An operator needn't load it from tape."

The model simulates the combined engine and vehicle—transmission, shift points, tire characteristics, and vehicle weight. The engineer manipulates such variables as mean pressure, temperature, bore and stroke, and cooling parameters. The output of a simulation run shows him the effect of the change on fuel mileage, emissions, and engine performance under standard operating regimes.

"Without the computer model," Krasse adds, "this simply couldn't be done within the available time and money."

Technicians tear down a prototype free-piston Stirling engine. With an IBM 4341, Mechanical Technology Inc. can present an online model of the engine to designers through 23 terminals.

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CIRCLE NO 56

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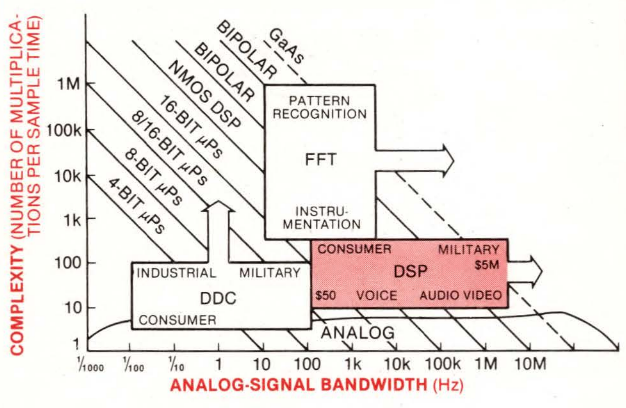
Data Processing Division

Signal-processing design awaits digital takeover

Just as digital processing techniques are poised to invade applications in dynamic control systems, so they're also ready for widespread application in signal processing.

Robert H Cushman, Special Features Editor

Are major portions of the analog-design world ripe for digitization? As the previous article in this series (**Ref 1**) pointed out, the answer is yes. That article enumerated the three major design areas—digital dynamic control (DDC), digital signal processing (DSP) and fast Fourier transformation (FFT)—in which VLSI progress will allow performance of analog functions more economically in the digitized-analog (sampled-data) mode than in the conventional manner. And it detailed how a standard μP can perform a typical DDC task: servo control. Here, we focus on the DSP area and its emerging specialized signal-processing hardware.



NOTES:
DDC = DIGITAL DYNAMIC CONTROL
DSP = DIGITAL SIGNAL PROCESSING
FFT = FAST FOURIER TRANSFORMATION

Fig 1—Here's how DSP (digital signal processing) *fits into the complexity-bandwidth picture. This figure is a repeat of an illustration used in the previous article in this series* ***(Ref 1),*** *but with the application region for DSP emphasized. We have also added some system-cost figures, ranging from $50 for the simplest low-performance systems to $5 million for the most complex high-performance configurations. These costs will drop by an order of magnitude as more VLSI devices for performing DSP functions reach the market.*

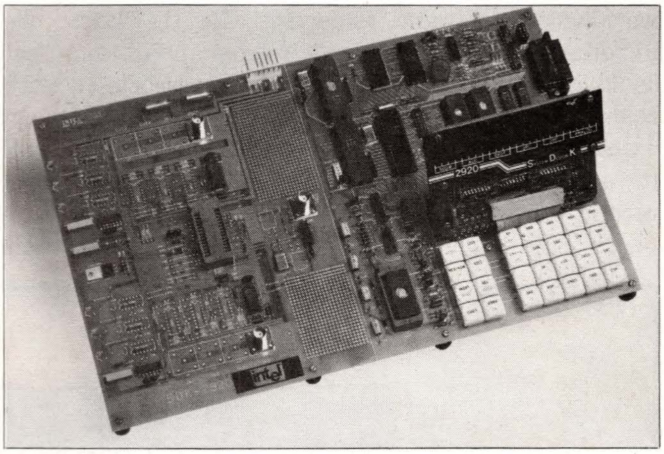


Fig 2—A single-board development tool *for the Intel 2920 DSP chip, the SDK 2920 comes in kit form and costs $950 ($665 to schools). It houses three μP devices: the 2920 and an 8085 and 8041A. The 8085 serves such functions as 2920 emulation, programming and system control; the 8041A is used for keyboard-display interfacing. With this board, a user can develop 2920 programs, burn them into the 2920's on-chip EPROM and then run the 2920 as a real-time signal processor handling voice-bandwidth analog signals.*

As a memory refresher, examine **Fig 1,** which repeats **Ref 1**'s first figure and exhibits where DSP applications fit in the computation-complexity/bandwidth plane. Note that from the standpoint of the equations processed, DSP resembles DDC, but with regard to applications served, the two areas differ in several respects. Specifically, DSP serves open-loop communications channels rather than closed-loop control systems; hence, DSP applications often crowd the available hardware's upper frequency limits. DDC applications, on the other hand, are typically more safely within the hardware's bandwidth limits.

As a result, DSP designers must invariably use special-purpose hardware for sum-of-products number crunching. The newest DSP chips make such hardware available economically, at least for voice-bandwidth

Japanese companies could be a force in DSP chips

applications. And hardware for faster audio and even video DSP is available if your application can afford the more costly bipolar LSI DSP building blocks.

Where to look for DSP advances

Table 1 lists some of the sources of DSP-component progress. It presents the semiconductor suppliers first because they will have the most immediate, practical interest to designers. However, it also lists other sources, including corporate research centers that are sources of captive DSP devices and universities that have been active in the theoretical investigations so vital to DSP. This list is by no means complete—its intent is to make you aware of the breadth of interest in DSP.

As you can see, the roster reads like a Who's Who of worldwide electronic expertise. In the past, the impetus for research came only from applications that could afford the expensive hardware associated with real-time digital processing of analog signals—an expense that effectively narrowed the interest in DSP to military uses (such as radar and sonar). More recently, however, the large telecommunications suppliers have joined the aerospace contractors in their interest in DSP. And now, thanks to LSI progress, even toy manufacturers, such as Mattel, can afford an interest in DSP (for speech synthesizers).

As in the μP Revolution, Intel again leads in the commercialization of the field at the OEM device level for the merchant market. It's again followed by American Microsystems Inc (AMI), which, in case you've forgotten, was one of the early birds in the μP Revolution. (Remember AMI's 7200 and 7300 μPs, announced from 1972 to 1974 but never produced in working silicon because they were too far ahead of their time?)

Many of the other semiconductor manufacturers are also doing their part to repeat μP history: They are again in the process of cautiously following Intel's lead. We feel the ones to watch are those that make μPs and also have been manufacturing LSI devices for telecommunications (such as codecs and switched-capacitor-type digital filters). Individuals responsible for product planning at Advanced Micro Devices (AMD), National Semiconductor and Mostek have told us they are monitoring the success of the first-generation DSP chips and are making their own plans to enter the market.

We also hasten to make special mention of TRW/LSI Products, one supplier that's not following Intel. TRW, with its fast bipolar LSI multiplier/accumulator, has been pioneering DSP applications all the way up to video bandwidths. Its experience in DSP goes back to

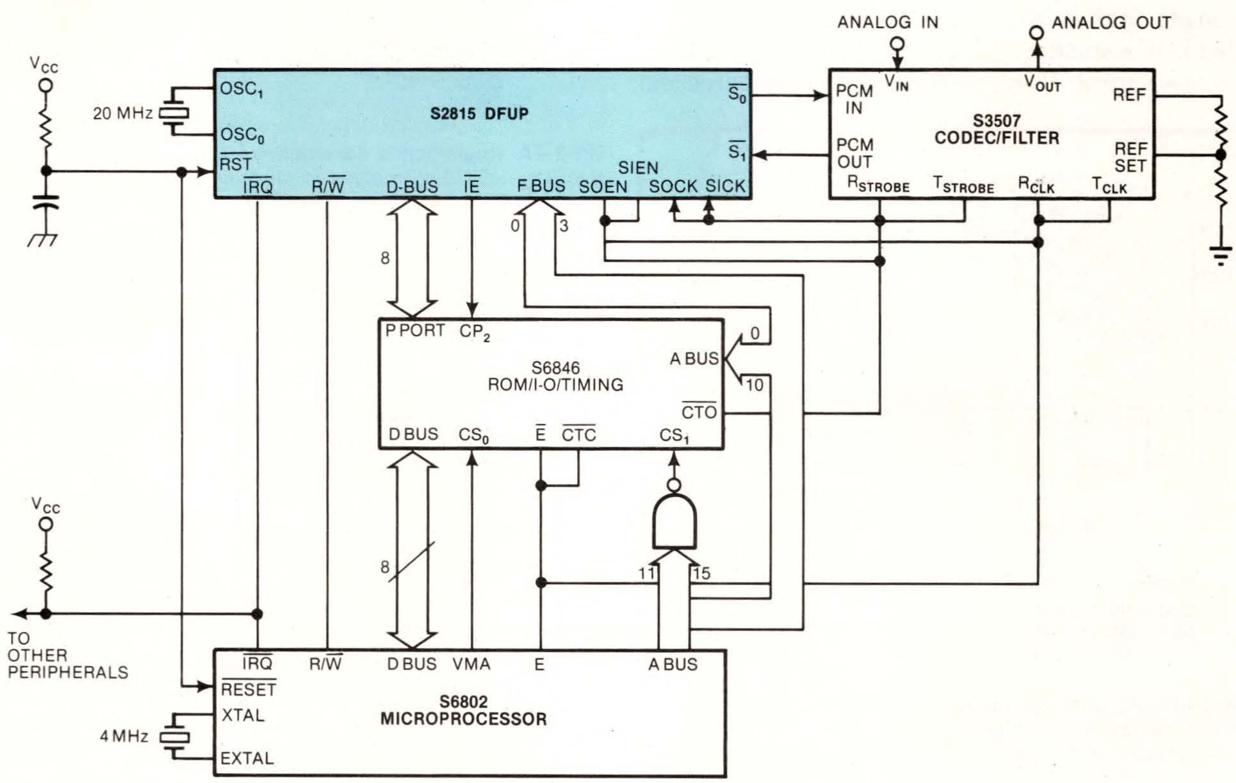
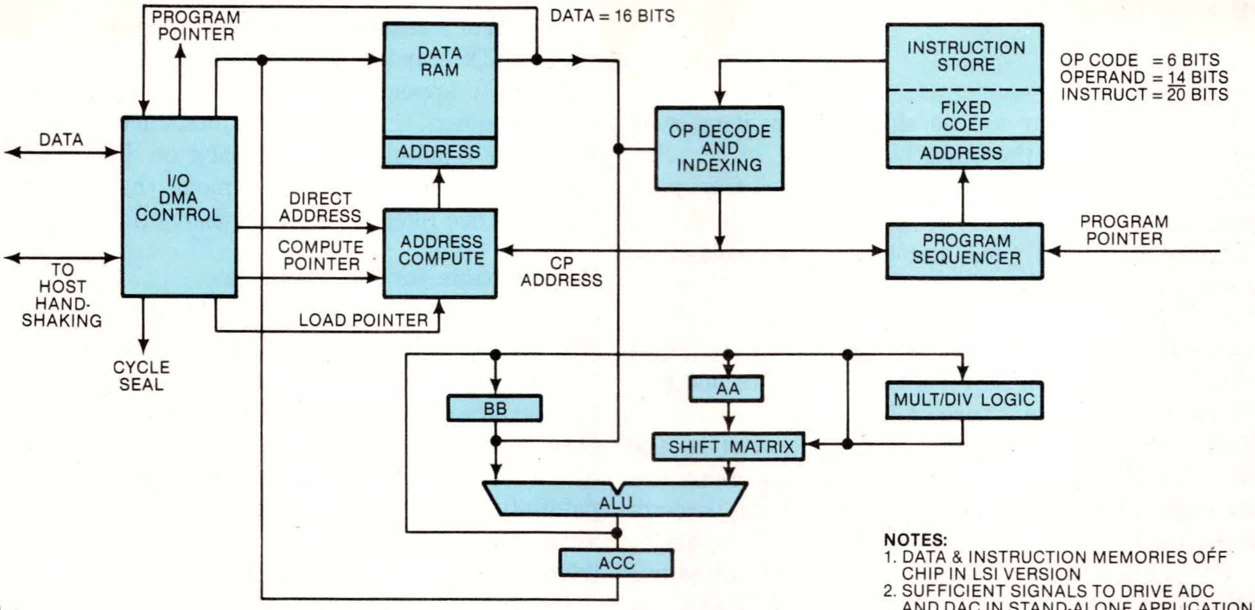


Fig 3—This simple system *provides experience to novices in DSP applications. It uses American Microsystems' preprogrammed 2815 chip as a peripheral to a 2-chip 6800-family μP system. An inexpensive codec provides the analog interface. The 6802 μP receives its instructions from the ROM in the 6846 combo chip and sets up a jump table in the 2815. This jump table selects the proper subroutines from the 2815's preprogrammed repertoire for use in the DSP iteration loop.*



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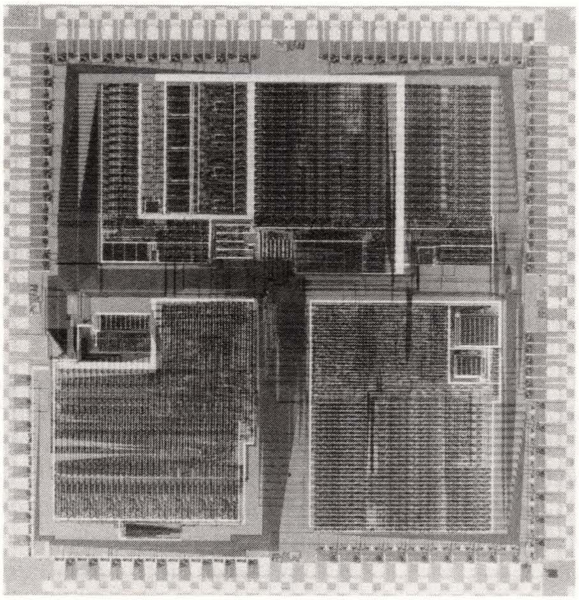

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Fig 4—A large (300×300-mil) NMOS device *with an extraordinary number (181) of off-chip connection pads, IBM's DSP chip* ***(a)*** *uses the connections to facilitate data movement, especially in multiple-chip configurations in large arrays. It employs the same shift-and-add approximation for multiplication as Intel's 2920, trading off some speed for architectural simplicity* ***(b).***

the 1950s—when it produced a process-control computer (the RW-300) that in all respects except speed could perform the scientific number-crunching-type computations needed in DSP. TRW's DSP application notes, and its recent Designer's Guide to digital signal processing, which appeared in this magazine (**Ref 2**), are examples of the quality of its commitment to DSP.

Observe that **Table 1** also includes some Japanese companies. The Japanese represent a new factor in the digitization race—a factor that wasn't present in the critical early phase of the μP Revolution. This time, the Japanese firms are neck and neck with the US leaders, and the fact that so many of them are not only technically able and aggressive but also large, well-financed industrial giants makes us expect them to be on equal footing with US firms in this race. Indeed, we keep hearing rumors of sophisticated new second-generation DSP chips due from NEC, Hitachi and other Japanese contenders.

How do the DSP chips stack up?

Table 2 presents some of the important parameters of the first-generation DSP chips. It comes from **Ref 3** and has stood the test of exposure to comment from industry DSP experts. Consultant Richard Blasco compiled it for an EDN session on DSP at last fall's NEC conference in Chicago.

Like the first-generation μPs (remember the 4004 and 8008?), these first-generation DSP chips exhibit some shortcomings. For example, an Intel source says that he thinks the 2920's designers might have paid too high a price in squeezing analog interfaces (ADC and DAC) on chip, and he predicts that some future Intel DSP devices will have off-chip analog interfaces. They'll probably also employ 10- to 12-bit analog conversions instead of the current nine bits. The source also predicts that the future Intel devices will have μP-bus interfaces like those of the AMI 2811 and NEC 7720; users have complained that it's too difficult to transfer variables into the 2920.

The 2811's most glaring shortcoming is its 12×12-bit multiplication, which most users feel is marginal. 16-bit-wide arithmetic will probably become standard in the next generation of DSP chips.

The 7720 has its faults, too. It doesn't provide automatic saturation arithmetic, so users expecting overflow must insert extra code to check and make corrections for it. (Otherwise, very erratic system

Architectural advances will be the key to DSP-chip success

operation could occur as the signal bangs hard over from one polarity to the other.)

Blasco's list of desirable features for the next generation of DSP chips (see **box,** "What will future DSP chips look like?") has also been well received by the industry experts to whom we've shown it. If you're not familiar with DSP technology, we urge you to study these 11 features carefully; they reveal the weaknesses of the first-generation DSP chips and point to features that will help you use future chips.

Such architectural features will be crucial to the success of NMOS DSP chips; performance gains are more likely to come through architecture than through raw increases in chip operating speeds. VLSI technology will help, because it will permit architectural sophistication. As some of Blasco's 11 points indicate, a good part of the next generation's design effort will go toward making the chips easier to use. Certainly, small-volume users would appreciate having chips with built-in self-emulation capability, for example.

A word of warning to designers who are already up to speed on DSP and itching to obtain the next-generation devices. It appears that the recession is temporarily slowing down the products' introduction schedules. Intel, for example, has cut back on DSP marketing budgets, and that move will mean that all the Intel followers are likely to slow up their efforts, too.

Helpful tools for the beginner

But the spotty availability of DSP hardware is not what will slow the inevitable digital takeover; rather, the forcing function will be most designers' lack of knowledge. Experts agree that capable, economical DSP devices will probably arrive before most designers have been educated to use them. Suppliers are painfully aware of this designer education barrier and are producing solutions. We'll briefly describe two: one from Intel and one from AMI.

Intel's SDK board for the 2920 **(Fig 2)** is a relatively low-cost ($950) kit that allows designers to ease themselves into familiarity with the 2920. It's a far less

What will future DSP chips look like?

If you read older research papers on DSP using MSI bipolar devices, then look at the features enumerated in **Table 2,** you'll discover certain trends that in turn will lead you to ask what future VLSI DSP devices will look like. In his paper **(Ref 3),** consultant Richard Blasco speculates on this subject and comes up with an 11-point list of desirable features for the next generation of DSP chips:

- **Writeable control stores.** For flexibility, users will want programs to be stored in on-chip RAM so different programs can be downloaded from the host μP. Blasco reasons that DSP programs tend to be short, and for multimode operation, it's desirable to change them during system operation.
- **Dynamic RAM.** Because of the repetitive nature of DSP algorithms, Blasco says it makes sense to use dynamic RAMs. (Coefficients would also be stored in RAM, of course.)
- **Floating-point arithmetic.** Most users tell us they would love the freedom from scaling worries provided by floating point. Blasco believes that although it will be impractical for future DSP devices to give users full floating-point capability (it requires too much chip real estate and execution speed), it will be possible to compromise and give them block floating point.
- **Nested subroutines.** Blasco believes that this feature will be desirable because it will significantly reduce overhead in matrix calculations (important if the chip is also to be used for FFT).
- **16-bit word length.** Blasco agrees with what we have found in our user surveys: A 16-bit word appears optimum for most users. And he reasons that the 16-bit width should be carried through to the I/O ports to provide compatibility with the new 16-bit μPs.
- **Double precision.** Blasco believes that double-precision (32-bit) words would be a desirable software option and should be available as macro commands.
- **Byte access.** Both bytes of a 16-bit word should be available to provide more memory use when 8-bit precision is required.
- **Expanded arithmetic capability.** The ALU should provide the full set of arithmetic, logical and bit-manipulation capability (as in modern μPs). Bit manipulation would simplify pseudorandom noise generators for speech synthesis and data scramblers.
- **User - defined macros.** Special registers would permit microcoding of macro instructions via the external port. Users could redefine these macro instructions to optimize each application.
- **Variable instruction-cycle length.** Although all the first-generation DSP chips have fixed instruction-cycle lengths, benchmarks on the 2811 suggest substantial improvement with variable-length instruction cycles. Instructions not requiring the full memory-to-memory cycle time could be executed in short cycles.
- **Self emulation.** Blasco believes this feature is the answer to the DSP-development-system dilemma. He says that all flags and registers should be readable and writeable via an external port. An extra bit should be added to the instruction word for hardware breakpoints.

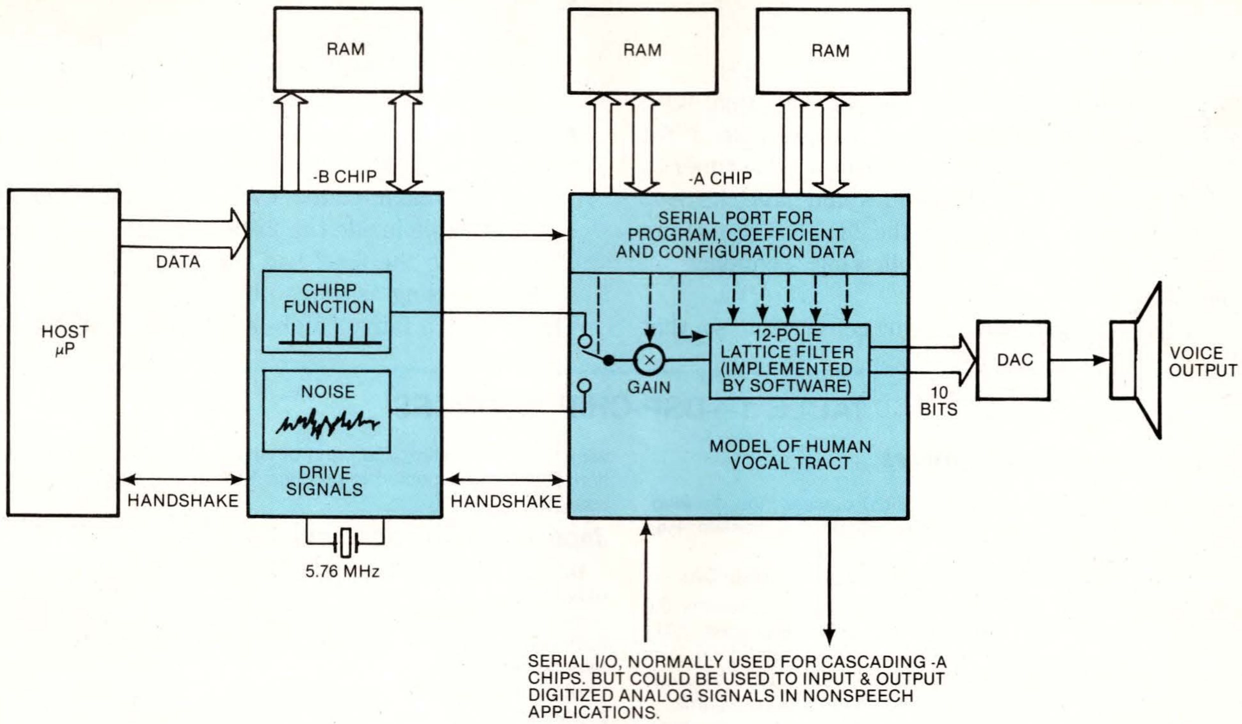

Fig 5—Some of the VLSI devices *being developed for speech-synthesis applications could also prove useful for general DSP uses. Here, the two chips of Telesensory Speech Systems' speech generator implement the popular linear-predictive-coding (LPC) synthesis method. The -A chip might be appropriate for general DSP uses because it's a programmable DSP computer—the host can vary both the filter structure and the filter coefficients. Thus, it might be applied to multimode (different filters), adaptive (different coefficients) applications.*

expensive tool than Intel's standard Intellec development station, which can run to $30,000, complete with 2920 disk-based software and programming accessories. This SDK unit is patterned after the SDK boards that Intel supplies for the 8080, 8085 and 8086 μPs; it surrounds an EPROM-based 2920 with enough intelligence (resident in an 8085) so that you can develop programs, burn them into the 2920 and then try them out by running the device.

Acknowledging that it wants to cater to the bias of today's EE students toward all things digital, Intel offers the 2920 SDK board at a lower price ($665) to schools. We suspect that if most students discover that they can perform "messy" analog functions in a "clean" digital manner, that's how they will always want to handle analog design. (This, incidentally, is yet another reason we are certain the digital takeover of analog functions will occur.) Intel is preparing a 50-pg lab notebook to accompany the kit, although budget cutbacks are slowing the project.

Complete DSP routines at your call

AMI's 2815 version of the 2811 is another product that should help designers gain familiarity with DSP chips. Its on-chip ROM is preprogrammed with a series of independent callable subroutines of general interest in signal processing:

- Two 32-tap transversal (FIR)-filter routines, cascadable into a single 64-tap filter
- Two recursive (IIR) biquadratic filters, providing a total of 16 filter sections
- Assorted computing functions: Two integrating, two rectifying, plus squaring and block-multiplication routines
- Conversion functions: μ-Law-to-linear, linear-to-μ-Law and linear-to-dB transformations
- Generator functions: sine and pseudorandom noise patterns.

With preprogrammed modules callable as subroutines resident in the 2815, you're past the obstacle of not having an emulator. And that's quite an obstacle, considering the dearth of 2811 emulators and the high cost ($20,000) of the ones that are available.

The 2815 will cost $300 initially, but its price will drop to $195 later this year and eventually approach $30. With this device, you can set up your application as shown in **Fig 3**, where the 2815 is driven as a peripheral to a standard μP such as the 6802. A 6846 combo chip provides the interfacing. And because the 2815 incorporates μ-Law-to-linear conversions, an inexpensive codec ADC (the 3507) can provide the interface to the analog world. The 6802 application program would reside in the 6846's ROM; it could make the 6802 set up the sequence of 2815 routines to be utilized in the DSP iterations. The analog data would go in and out through the 3507 codec/filter, feeding serially into the 2815.

Captive DSP chips are just as important as commercial units

Suppose you wanted to filter the analog signal with the 64-tap transversal-filter option, for example. First you would program the 6802 to set up the 6846 timer to define the sampling rate. Then you would have the 6802 set up the indirect-jump table in the 2815 RAM, making the jump table select the following sequence of preprogrammed 2815 routines:

- Choose the μ-Law-to-linear conversion so that the input from the codec would be "straightened out" to its full 12 bits.
- Call up the two 32-tap transversal filters in cascade (one after the other) to perform the filtering (the 6802 program would have loaded the coefficients into the 2815).
- Call the linear-to-μ-Law conversion routine so that the "signal" would be ready to go back out to the nonlinear codec DAC. You could make the jump table inside the 2815 loop back onto itself so that once the 6802 had set it up, the 2815 would keep cycling as driven by the 6846 timer.

The 2815 is a fairly "high-level" DSP building block,

TABLE 1—DSP-CHIP SOURCES[1]

US Semiconductor Suppliers

Intel (Phoenix, AZ)—Delivering 2920 devices and development tools and also conducting user educational classes. Has new products in definition phase.

American Microsystems Inc (AMI) (Santa Clara, CA)—Is finally delivering 2811 parts with two preprogrammed options: the 2814 FFT and the 2815 with assorted DSP subroutines. 2811 parts still in hard-to-produce VMOS, but second-generation follow-on processor in more conventional NMOS said to be under joint development with another, as-yet-unannounced source.

TRW/LSI Products (El Segundo, CA)—Various very-high-speed bipolar multiplier/accumulator MSI/LSI parts plus excellent application help (literature) for DSP.

Advanced Micro Devices (AMD) (Sunnyvale, CA)—Has recently announced bipolar DSP parts for 2900 family, and expects to announce NMOS parts similar to 2811 later this year.

Monolithic Memories Inc (MMI) (Sunnyvale, CA)—Has produced high-speed bipolar multiplier/accumulator parts. Possibly its PAL circuits could be used for semicustom approaches to DSP.

Texas Instruments (Houston)—Recognized leader in mass-produced speech applications (Speak & Spell learning toy); therefore, can be expected to have capability in DSP.

Motorola (Austin, TX)—Working on speech chips that will be announced later this year. Because it has both communications and military groups, can be expected to have strong interest in DSP.

National Semiconductor (Santa Clara, CA)—Currently supplying speech chips to consumer market; has group that is studying DSP market and defining products.

General Instrument (Hicksville, NY)—Has speech chips for consumer market that it says might have some DSP uses.

Signetics (Sunnyvale, CA)—Fast 250-nsec 8X300 bipolar μP has n-bit-shift capability as part of some instructions, so might be suitable for low-resolution (8-bit) filtering. To-be-announced version of 8X300-type controller might be faster for DSP.

Rockwell International (Anaheim, CA)—Should have interest in DSP, because of its LSI-modem products and because of Aerospace Div's expertise in real-time signal processing, also because of Collins Div's work in communications.

Intersil (Cupertino, CA)—Now that it is part of GE Co, might have resources and motivation to pursue DSP.

Mostek (Carrollton, TX)—Has been "studying" DSP market for more than a year now because of its interest in communications.

Fairchild (Mt View, CA)—The I^2L process used on 9445 μP would seem good candidate for DSP, especially if analog conversion circuits could be incorporated on same chip.

Analog Devices (Norwood, MA)—Has part interest in Signal Processing Circuits (Salt Lake City, UT), a small LSI house that has produced DSP circuits.

European Semiconductor Suppliers

Intermettal GmbH, ITT (Freiburg, West Germany)—MAA 1000 chip slated for end of this year or 1982; a stand-alone VLSI DSP device for audio uses such as stereo. Two versions, one with 16×8-bit multiplication and other with 16×16-bit multiplication. Pipelining expected to produce 150- to 200-nsec speed for instructions.

Japanese Semiconductor Suppliers

NEC (in US, Wellesley, MA)—The 7720 DSP chip is being used in Japan, but its US introduction has been delayed while support systems suitable for US market are developed. Expect further impressive DSP devices from this international leader in telecommunications.

Hitachi (Tokyo)—Engineers from Central Research Lab have presented papers on "Single-Chip Signal Processor for Speech Analysis."

Fujitsu (Kawasaki)

Toshiba (Kawasaki).

Corporate R&D centers

Bell Labs (Murray Hill, NJ)—Has been a leader both in theoretical research and production of actual devices (see **Table 2**) for several decades. Has interest in DSP for communication filtering, satellite echo canceling and speech.

IBM (Yorktown Heights, NY)—Has had active research program in DSP at Watson Research Center for many years; during past year, Federal Systems Div (Manassas, VA) has produced VLSI DSP part that it will use in Navy VHSIC program.

Aerospace Contractors

Westinghouse (Baltimore, MD)—Defense and Electronic Systems Center has been pursuing VLSI DSP development as part of military systems (radar and sonar).

Hughes Aircraft (El Segundo, CA)—Working on USAF VHSIC program, which has as one aim the production of very-high-speed devices for DSP.

Universities[2]

MIT (Cambridge, MA)—Some of the leading texts on DSP have come from MIT professors.

Stanford University (Palo Alto, CA)—In addition to offering courses in both DSP and DDC, has commenced a program of VLSI education that will permit students to use CAD approaches (based on text by Carver Mead and Lynn Conway) to implement architectures such as those suited to DSP. In some cases, students have actually fabricated devices for test and evaluation.

University of Illinois (Urbana)—Has offered courses in sampled-data systems for many years.

Concordia University (Montreal, Canada)—Example of smaller college that has been teaching courses in DSP.

[1]Just a partial list, ordered within each category in terms of viability of products. You can assume that all major aerospace contractors have an active interest in DSP; most are continually advertising for signal-processing specialists in their employment ads.

[2]List covers a scattered sampling of schools active in DSP. However, even a full list would show that as yet DSP is not properly covered as an undergraduate subject, but rather treated as a graduate specialty.

but it does have one limitation: You can't change the filter coefficients on the fly, so dynamic adaptation of the filter characteristics isn't possible. However, AMI is considering producing another preprogrammed version that will be suitable for adaptive equalization filters.

Captive devices are also important

Although the DSP chips originated by industrial giants such as AT&T's Bell Labs (Murray Hill, NJ) and IBM's Watson Research Center (Yorktown Heights, NY) might never be available to designers outside those organizations, they are nevertheless also important to understand. DSP by its very nature requires considerable research input at all levels—from basic mathematics to system applications. Many tradeoffs arise, and often only the large research operations have a full grasp of them. Some of the semiconductor suppliers won't be able to afford to investigate all implications thoroughly. The last column in **Table 2** indicates what Bell Labs is doing; we now examine IBM's effort.

Fig 4 shows the large (300×300-mil) chip that IBM has developed for DSP applications. The device embodies architectural concepts that have been evolving at Watson Research Center since the early 1970s. (The concepts have been the subject of a series of papers by IBM researchers over the past 5 yrs; see **Ref 7.**) The chip itself was designed and processed by IBM's Federal Systems Div (Manassas, VA) with the US Navy as the potential customer. IBM indicates that the Navy wants the device as part of sonar and radar signal processors.

The chip has several noteworthy features. Most obvious is its very large number—181—of off-chip pads around its edges. Compared with the other NMOS DSP chips **(Table 2)**, most of which come in 28-pin DIPs, this is a very large (and expensive) number of pins indeed.

IBM cites several reasons for employing this extensive pinout. Two groups of pins are needed to interface to the external program and data memories associated with each chip. (The designers felt that such external storage would provide much more flexibility than the small quantities of on-chip storage found in other LSI DSP chips.) The instruction memory requires 24 pins for code and 16 for addresses; the data memory, 16 pins for data and 16 for addresses.

The IBM chip also uses parallel I/O interfaces for the digitized analog signal interfaces, rather than serial channels as in the 2920, 2811 and 7720, to achieve the necessary speed. This structure calls for 16 pins for data and 16 for addressing, plus several pins for control and debugging.

The chip's architecture closely follows that of the TTL DSP research machines in use at IBM for several years. Word width is 16 bits, and instruction cycle time equals 200 nsec—achieved in part by using four levels of instruction pipelining. But despite the 200-nsec cycle time, the chip will probably always be slower than the 2811 or 7720 because IBM has elected to use a shift-and-add scheme for multiplication rather than expend the chip space required for a full hardware-multiplication operation. Because the shift-and-add multiplication scheme typically requires three to five instructions to approximate a multiplication, and because the multiplication occurs on fixed coefficients, machines employing this scheme must always be slower and less general than machines with full hardware multiplication. (Intel also uses such a shift-and-add scheme in the 2920, and according to IBM, Intel has from the start acknowledged that it obtained the idea from published IBM research reports. However, it's not clear whether Intel also uses IBM's "canonical signed digit" coding for the shift and add, which reduces the number of shifts and adds needed.)

One reason that IBM chose the shift-and-add approach is that it mates well with an FFT algorithm developed by the firm's S Winograd. This Winograd FFT trades off multiplications in favor of additions.

Evidently, because of its size, IBM is able to look beyond the simpler applications possible with single DSP chips to the larger ones that demand DSP-chip arrays. The experimental chip's many pinouts should facilitate forming such arrays; according to published IBM reports, researchers have configured at least five of the chips together in larger systems. Even larger arrays are realistic in DSP applications, because once analog signals are digitized, signal degeneration is no longer a concern, and it's thus possible to use very large filter structures—such as 1000-tap transversals—and obtain the selectivity desirable in many applications.

The problem of handling larger arrays is accompanied by the problem of software development. Again, thanks to its resources, IBM has apparently been able to devote considerable attention to developing programming aids. It has reported a high-level "assembly" language for host-computer/DSP-chip systems. In use since 1978, the language has evolved to the point where many DSP-hardware idiosyncracies need not concern users.

Other sources of DSP hardware

Another possible source of DSP hardware that you shouldn't overlook is the growing development effort for economical speech-synthesis (and perhaps speech-recognition) components (EDN, April 1, pg 45, and May 27, pg 100). Because the most popular method of computer synthesis of human speech uses a digital filter to model the human vocal tract, most speech systems have some DSP capability. And although in most cases the speech chips are highly customized for speech-system use, in at least one instance they have enough general-purpose capability to serve other uses as well.

Telesensory Speech Systems Inc (Palo Alto, CA) has developed such a programmable 2-chip set. **Fig 5** shows how the -A chip and the companion -B device implement the linear-predictive-coding (LPC) configuration, which is currently the most popular speech-synthesis method. LPC simulates the way human vocal chords drive the vocal tract.

The DSP part of the system occurs in the -A chip, where a digital filter simulates the vocal tract. The idea behind speech synthesis is to keep changing the filter coefficients and excitation options at rates fast enough to make the output to the audio speaker a close replica of actual human speech. Typically, these rates equal 10 to 20 msec. The filter is usually a multiple-section all-pole configuration in which the sections simulate the various cavities along the vocal tract. (Telesensory often uses a 12-pole lattice structure.)

This vocal-tract model gets driven by signals from the -B chip: pulses (chirps) for "voiced" utterances or white noise for "unvoiced" sounds. In the standard speech application, the -B chip also interfaces between the host μP and the -A chip.

The Telesensory -A chip exhibits a flexibility approaching that of a general-purpose DSP chip such as the AMI 2811. Telesensory gave it this flexibility to allow for reprogramming with different vocal-tract models to keep up with the continuous innovations in this active field. Thus, with the -A chip, not only can you change the filter-model coefficients, you can also implement different filter structures by downloading different program sequences. (The filter gets implemented in a true computer-programmed manner—ie, a program counter accesses a sequence of instructions out of memory.)

The catch is that the -A chip permits only 16 straight-through program steps. Fortunately, each of these steps has the power to implement two multiplications (the chip contains two separate multipliers), two additions and various data movements. Moreover, internal arithmetic is 18 bits wide, with 10-bit-wide coefficients. The 16 instruction steps execute in 100 μsec, so the sampling rate is 10 kHz.

In fairness to Telesensory, we note that the firm never intended its chips for anything but speech work. And even in speech work, it intended mainly to offer the chips at the board level (complete with sets of coefficients for the words in customer-specified vocabularies). But the firm has told us that it will supply chips, as available, to engineers capable of putting them to system-level use. Price will start at $250 per chip in single quantities but drop below $50 in high volume.

Jim Caldwell, architect of the chip set (which is made for Telesensory by Silicon Systems Inc) says that a designer who wishes to put the -A chip to other uses should understand its strengths and weaknesses. It's good at implementing IIR filters but not suited to FIR filters, for example. (IIR filters are digital equivalents of active-op-amp filters, and FIR configurations are transversal types.) Caldwell believes performing FFTs with the device might be out of the question. A good structure for the -A chip would be cascaded second-order sections, because each instruction contains the multiplications and additions to implement a second-order section. The device is of course also very good at implementing the lattice filters used in speech synthesis. Obviously, because it's intended for good-fidelity voice generation, it can handle bandwidths to 3 or 4 kHz.

Caldwell says that if the -A chip were processing digitized analog signals, you could enter the sampled-data words via its high-speed serial input port, which in speech work serves to pass the digitized analog signal between cascaded -A chips. For interfacing to the host μP, you could either employ the -B chip (not using the voiced and unvoiced excitation drives into the -A chip), or develop some outboarded TTL circuitry.

Considering the Telesensory chip set's capabilities in DSP applications, we advise designers to keep close tabs on the hardware being developed for speech systems. The current vitality of this bustling application area and the even greater vitality predicted for the future are sure to spawn many important DSP innovations, some of which will go into very high-volume production (for consumer products) and produce low-cost hardware for DSP uses.

Audio might drive high-performance market

After telecommunications and voice, the next mass market to use DSP techniques will probably be audio. As one of the chapters in **Ref 8** clearly explains, there are several reasons why the next gains in high-fidelity music can only come from the application of digital techniques. Interestingly, the various wide-band recording methods being perfected for the videodisk market could also have a profound effect on the growth of DSP for music recording, distribution and playback.

One semiconductor house that appears to be betting on DSP for audio is ITT's West German Intermettal operation. Its OEM catalog emphasizes LSI components for the telecommunications, auto and consumer audio markets, and it expects DSP processors to take digital signals from advanced PCM-encoded optical disks and perform the necessary filtering and other signal handling.

Intermettal likens its forthcoming MAA 1000 chip—it won't be in silicon till late this year or sometime next year—to the NEC 7720. But it says the device is intended more for stand-alone (single-chip) use in stereo audio systems (although it apparently has a somewhat general-purpose programmable architecture). Edmund Zahringer, designer of the MAA 1000 family, told us that at least two versions will be available: one with a 16×8-bit multiplier and the other with a full 16×16-bit unit. The multiplication and associated addition (or subtraction) for the basic sum-of-products operation will occur in one instruction cycle that will take place at a 150- to 200-kHz sampling rate and with a 14-bit signal. The chip will be a large NMOS device, and the multiplier will employ pipelining (as is usual in these DSP chips). Parallel data movement will be part of the basic instruction cycle.

TABLE 2 —COMPARISON OF DSP-CHIP FEATURES*

	INTEL 2920	AMI S2811	NEC μPD7720	BELL LABS
ARITHMETIC UNIT				
DATA-WORD SIZE (BITS)	25	16	16	20
COEFFICIENT (BITS)	(1)	16	13	16
ACCUMLATOR WIDTH (BITS)	28	16	16	40
SATURATION ARITHMETIC	HARDWARE	HARDWARE	SOFTWARE	HARDWARE
CONDITIONAL ARITHMENTIC?	YES	YES (2)	NO	YES
LOGIC OPERATIONS?	YES	NO	YES	YES
BIT-WISE OPERATIONS?	YES	NO	NO	NO
INPUT MODES	X,Y OR ACCUM	X,Y OR ACCUM	ACCUM ONLY	ACCUM ONLY
DOUBLE PRECISION?	NO	NO	YES	YES
ACCUMULATORS & SCRATCHPAD	1	9	2	1
SCALER CAPABILITY	2^2 THROUGH 2^{-13}	2^{-1}	2^3 THROUGH 2^{-1}(3)	2^3 THROUGH 2^{-3}
MULTIPLIER				
IMPLEMENTATION	SOFTWARE	HARDWARE	HARDWARE	HARDWARE
PRECISION (IN × IN = OUT)	(1)	12 × 12 = 16	16 × 16 = 31	20 × 16 = 36
MULTIPLICATION TIME (nSEC)	(1)	300	250	800
CONTROL				
INSTRUCTION WORD (BITS)	24	17	23	16
INSTRUCTION CYCLE (nSEC)	400	300	250	800
MEMORY TO MEMORY IN ONE INSTRUCTION?	YES	YES	NO	YES
SUBROUTINE LEVELS	NONE	1	4	1
ITERATION (LOOP) COUNTER?	NO	YES	NO	YES
CONDITIONAL JUMPS?	NO	YES	YES	YES
JUMP TABLES?	NO	YES	NO	YES
PROGRAMMING METHOD (ON CHIP)	EPROM	MASK	MASK	MASK
EXTERNAL CONTROL STORE?	NO	YES	NO	YES
MEMORY				
INSTRUCTION (CONTROL) ROM	192 × 24	256 × 17	512 × 23	1024 × 16
DATA RAM	40 × 25	128 × 16	128 × 16	128 × 20
COEFFICIENT ROM	(4)	128 × 16	512 × 13	(4)
INDEXED ADDRESSING?	NO	YES	YES	YES
AUXILIARY INDEX REGISTER?	NO	YES	NO	YES
Z^{-1} REGISTER?	NO	YES	YES	YES
LOOK-UP TABLES?	NO	YES	YES	YES
INPUT/OUTPUT				
ANALOG (RESOLUTION BITS)	9	NONE	NONE	NONE
PARALLEL (BITS)	4 IN/8 OUT	8	8	16
SERIAL PORTS	NO	YES	YES	YES
SERIAL SHIFT RATE (MAX)	—	3 MHz	200 kHz	3 MHz
SERIAL I/O CLOCKS	—	SYNCH/ASYNCH	SYNCH ONLY	SYNCH/ASYNCH
SERIAL PORT BUFFERING	—	DOUBLE	SINGLE	SINGLE
I/O SYNCRONIZATION METHOD	STROBE	FLAGS	FLAGS	FLAGS
BLOCK (DMA) TRANSFER?	NO	YES	YES	NO
MISCELLANEOUS				
FABRICATION TECHNOLOGY	EPROM	4.5-μm VMOS	3-μm HMOS	4.5-μm NMOS
DIE SIZE (MIL^2)	217	201	218	338
PACKAGE	28-PIN DIP	28-PIN DIP	28-PIN DIP	40-PIN DIP
DEVELOPMENT SUPPORT	SOFTWARE (8)	HARDWARE ICE (8)	SOFTWARE (8)	HARDWARE ICE (8)
BENCHMARKS (NO OF INSTR/SPEED IN μSEC)				
2ND-ORDER BIQUAD FILTER	14/5.6 (5)	7/2.1	9/2.25 (6)	4/3.2
TRANSVERSAL-FILTER TAP	3/1.2 (5)	1/0.3 (7)	1/0.25	1/0.8
32-POINT COMPLEX FFT	(9)	100/400	213/700	NOT AVAILABLE

NOTES:

*SOURCE: RICHARD BLASCO, R&L ASSOCIATES, SAN JOSE, CA. PRESENTED AT EDN-SPONSORED SESSION AT NEC CONFERENCE, CHICAGO, OCTOBER 1980 **(REF 3).**

1. THE INTEL 2920 USES A SHIFTING OR SCALE-AND-ADD MULTIPLICATION SCHEME. THIS APPROACH PROVIDES A MULTIPLICATION PRECISION OF 25 × 2N = 28, WHERE N REPRESENTS THE NUMBER OF SCALE-AND-ADD OPERATIONS PERFORMED. MULTIPLICATION TIME IS N × 400 nSEC FOR FIXED COEFFICIENTS, OR 4800 nSEC FOR A PRODUCT (PRECISION 12 × 25 = 28) OF TWO VARIABLES.
2. THE S2811 ARITHMETIC UNIT PROVIDES ABSOLUTE-VALUE AND LIMITER FUNCTIONS, WHICH ARE CONDITIONAL-ARITHMETIC OPERATIONS.
3. THE μPD7720 SCALER ALSO HAS THE CAPABILITY OF INTERCHANGING THE EIGHT MSBs OF A WORD WITH THE EIGHT LSBs OF THAT WORD. WHEN COMBINED WITH LOGICAL (MASK) OPERATIONS, A LIMITED BYTE ACCESS IS PROVIDED.
4. COEFFICIENTS IN THE INTEL AND THE BELL LABS PROCESSORS ARE PROVIDED AS PART OF THE CONTROL PROGRAM. THE CONTROL STORE INCLUDES INSTRUCTIONS AND FIXED COEFFICIENTS VALUES FOR THESE TWO PROCESSORS.
5. THE INTEL 2920 BENCHMARKS ASSUME THAT THREE SCALE-AND-ADD OPERATIONS PER FIXED COEFFICIENTS ARE ADEQUATE.
6. The μPD7720 DOES NOT PROVIDE SATURATION ARITHMETIC IN HARDWARE. ADDITIONAL INSTRUCTIONS AND PROCESSING TIME ARE REQUIRED TO IMPLEMENT A BIQUAD SECTION WITH SATURATION LIMITING.
7. THE S2811 TRANSVERSAL-FILTER TAP **PROCESSING** INCLUDES SAMPLE SHIFT Z^{-1} OPERATION WITHIN A SINGLE INSTRUCTION CYCLE. THIS IS POSSIBLE DUE TO THE AUTOMATIC LOADING OF THE S2811 Z^{-1} REGISTER.
8. DEVELOPMENT SUPPORT CONTINUES TO EVOLVE. INTEL APPEARS TO BE WELL AHEAD OF OTHERS IN THIS RESPECT AND HAS RECENTLY ADDED A LOWER COST SINGLE-BOARD DEVELOPMENT AID. AMI HOPES TO HAVE SOME SOFTWARE AIDS THAT WILL RUN ON ITS PHOENIX DEVELOPMENT SYSTEM. NEC's US MARKETING ARM (WELLESLEY, MA) IS STILL IN THE **PROCESS** OF DEFINING AND DEVELOPING SUPPORT FOR THE 7720, ALTHOUGH NEC HAS SUPPORT FOR 7720 IN JAPAN.
9. THE AUTHOR IS NOT AWARE OF ANY SUCCESSFUL ATTEMPTS TO PROGRAM A 32-POINT COMPLEX FFT ON THE INTEL 2920. (BUT INTEL SAYS THAT A CUSTOMER IS USING MULTIPLE 2920s FOR FTTs).

Audio chips could also herald DSP innovations

Zahringer predicts that both stereo channels will be handled in the DSP computation cycle. He foresees the 1-chip DSP device being less expensive than any analog approach because it eliminates much of the current bulky circuitry. Additionally, the digital approach could be programmed to detect some of the special mode-changing signals that would be part of future systems—the signals for the coding that indicates whether a signal is stereo or mono, for example. Although Intermettal intends the MAA 1000 primarily for audio uses, it could have nonaudio uses as well, although Zahringer cautions that the design's stand-alone nature means that it will not have the μP-bus interfaces of the NEC 7720 or AMI 2811. EDN

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(Note: ***Refs 3-6*** *are from an EDN-sponsored session at the NEC conference in Chicago last October. All but* ***Ref 5*** *are in the conference proceedings, obtainable from NEC, Oak Brook Executive Plaza 2, 1211 W 22nd St, Oak Brook, IL 60521. Contact R Cushman at EDN for copies of* ***Ref 5.****)*

7. Ruiz, Antonio, "Research Report RC 8669 (37893)," Obtain from IBM, Dept of Computer Science, IBM Watson Research Center, Yorktown Heights, NY 10598.
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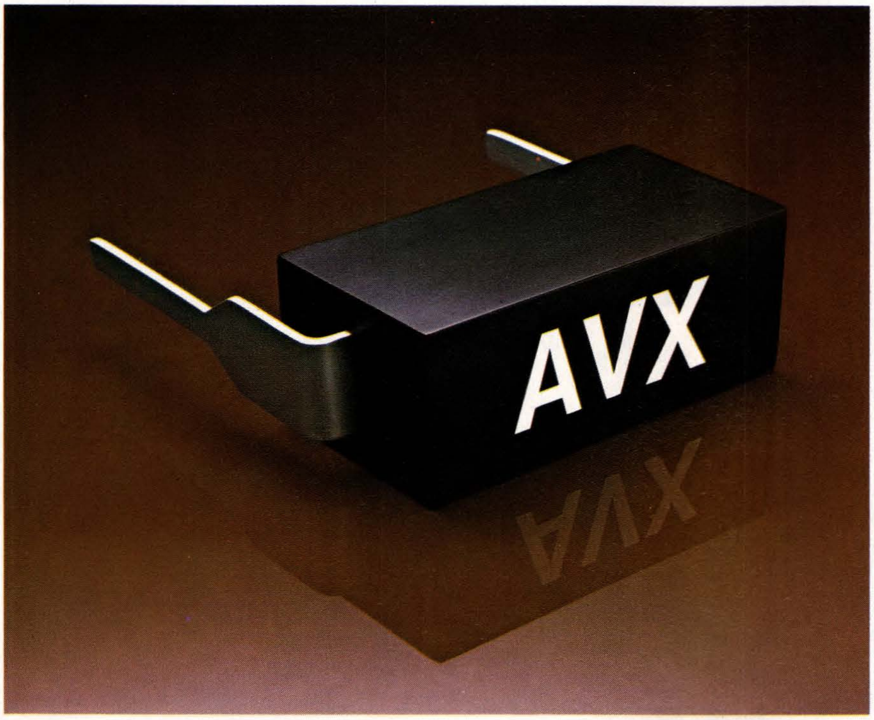

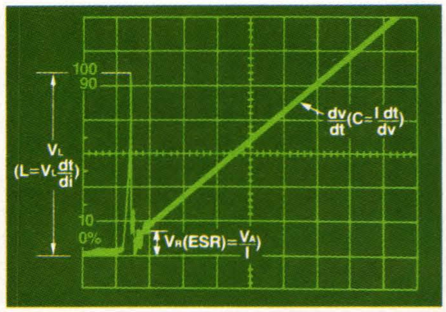

SCALE:
HORIZONTAL = 50NS DIV VERTICAL = 50MV DIV

Fig. 2. Scope trace of 0.22-μF film capacitor using test setup of Fig. 1 and 200mA/10 ns input.

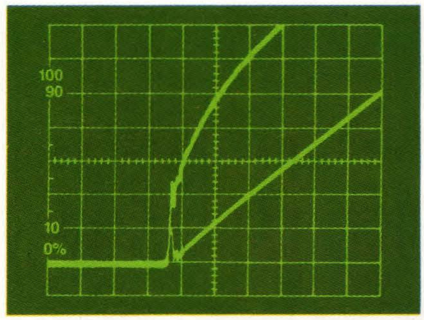

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Fig. 3. Scope traces of 0.1μF tantalum (top) and 0.1μF multilayer ceramic capacitor (bottom) using test setup shown in figure 1 and 200mA/10ns input.

Re-evaluating capacitor performance for today's ICs.

Capacitor performance specifications are still defined by technical standards of the 1930s—standards which reflect testing at low frequencies, under high DC voltages and to "Q"-type parameters.

However, modern circuits with faster edge rates, larger currents, and increased board densities have emphasized the need for more significant and appropriate capacitor performance criteria—especially for decoupling applications.

Test Setup

An effective method for defining capacitor performance is to simulate the conditions of actual operation. The test fixture shown in figure 1 was used by AVX to determine capacitor performance when subjected to high speed digital pulses. The HP 8012B generates pulses with edge rates of 200 mA/10ns or 200 mA/5ns and the voltage variations across the capacitor are exhibited on the high speed scope (figure 2). Using this setup, information regarding capacitance ($C = I\frac{dt}{dv}$), equivalent series resistance ($ESR = \frac{Va}{I}$ and inductance ($L = V_L\frac{dt}{di}$), can be derived for various capacitors.

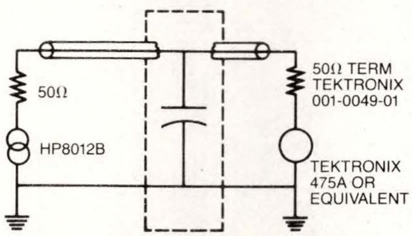

Fig. 1. High-frequency test schematic.

Initial results

The scope traces obtained from testing a .1μF multilayer ceramic capacitor (MLC) and a .1μF tantalum capacitor are compared in figure 3. These show that the tantalum capacitor does not recover due to its high internal resistance (ESR), as fast as the MLC capacitor. Additionally, the tantalum unit has only 50% of the capacitance of the MLC in the same time domain. The tantalum capacitor also has over 2.5 times the inductance of the MLC as shown by the initial voltage spike.

The scope trace used as an example in figure 2 is that of a .22 μF film capacitor. This capacitor shows recovery similiar to MLCs, but displays three times the inductance of an MLC.

Discussion

The low inductance of the MLC construction, along with its low internal resistance, means lower switching transients and faster capacitance recovery time during actual operation.

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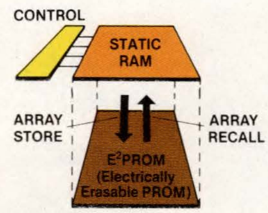

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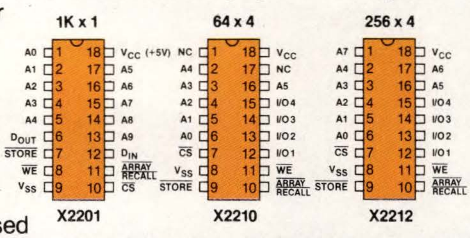

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CIRCLE NO 63

Amended patent/copyright law alters ownership rights, ups fees

The revised patent and copyright law will directly affect your work. But will it encourage innovation or merely place protection out of many inventors' reach?

Joseph S Iandiorio,
Patent, trademark and copyright attorney

Revisions in the patent law affect both the ownership of patents and the cost of that protection. This article reviews the amended law's provisions and analyzes its potential effects on innovation.

The law, designated PL-96-517, divides into four parts, covering:

- Patent fees
- Patent re-examination
- Patent rights to inventions made under federal contracts
- Amendments to the copyright law relating to computer software.

Processing costs boost fees

Under the pre-existing law, filing a patent application costs $65 for a fixed number of claims, which increases when you submit additional claims. In most cases, however, the cost doesn't exceed $100, and inventors can minimize the cost by limiting the number of claims included to that covered by the minimum price. An issue fee, typically $112 to $150, brings the total cost to $177 to $250.

Beginning October 1, 1982, and applicable to all patents filed after December 12, 1980, this fee system will change. Patent fees for processing an application from the filing through the issuance stages will strive to recover 25% of the estimated processing cost for utility patents and 50% for design patents. (See EDN, September 5, 1980, pg 189 for an explanation of patent types.) Based on some recent estimates that place the government's average utility-patent processing cost at approximately $1500, filing costs will initially escalate to $375.

Additionally, the law's additions establish a maintenance fee, which will serve to prevent a patent from lapsing and thus becoming unenforceable. Such fees, payable at 3½, 7½ and 11½ yrs after issuance, will be set to recover another 25% of the processing cost.

The maintenance-fee increase could make inventors' business decisions more difficult. For an invention known to be valuable 3½ yrs after patent issuance, the decision to maintain the patent can be easy. But for a pioneering invention, 3½ yrs might not be sufficient time to determine its worth. Many new inventions don't break into the market in such a short period of time. The maintenance fees, initially expected to be set at $375, could thus discourage inventors from filing for patent protection.

Furthermore, because the government's $1500 estimated processing cost is based on the cost of a patent application that matures into a patent and is maintained for the full 17 yrs, the actual fees charged a patent holder will probably rise even higher than initial estimates. Why? If only half the patents filed survive for the full 17 yrs—a likely occurrence—the fee burden on the remaining holders doubles.

The fees will continue to rise anyway, of course, because no ceiling applies to them: They are pegged to the government's processing costs. And like all government costs, they will increase with inflation.

Increased costs create other problems

The jump in application costs and the establishment of maintenance fees are only two problems with the new fee structure. Lawmakers have paid little atten-

Patent fees must cover processing costs

tion to how to fairly allocate fees between difficult cases that consume much time and effort and simpler cases that are easier to process. Fees for all services and materials will be set to recover their average estimated cost to the Patent and Trademark Office.

Opponents argue that this new fee structure will chill if not stifle innovation and invention disclosure by small businesses and individuals—both major sources of innovation. Some observers suggest applying the new Regulatory Flexibility Act (Public Law 96-354), which requires government agencies to draft regulations with an awareness of the differences in their purpose and burden when applied to large and small businesses and to make necessary adjustments in the interest of fairness.

During discussions of the patent bill on the floor of Congress, some members suggested that Congress monitor implementation of the regulations closely to ensure that they don't discourage small businesses and independent inventors. Because Congress didn't intend to raise fees to the point where financial burdens would prevent inventors from filing patent and trademark applications, some members additionally suggested that the Patent and Trademark Office set fees reflecting the lesser ability of small companies or individuals to pay them and thus consider several tiers of processing, filing and maintenance charges.

Who owns government patents?

In addition to the fee structure, Congress considered government ownership of patents. Many members maintained that policies regarding government ownership of inventions made under federal contract merely confused the protection issue. The number of policies on that subject has equaled the number of government agencies involved: 25 or more. Most of these agencies assigned patent title to the government with only a nonexclusive license for the inventor. But because the same license was available to all qualified parties—including the inventor's competitors—little government patent technology was utilized.

Obviously, you don't want to develop a product and market it if a competitor can jump in when your progress indicates that you've spawned a marketable endeavor. Thus, a nonexclusive licensing policy designed to encourage the broadest use and distribution of publicly funded technology actually had the opposite effect. Critics suggested that nonexclusive licenses suppressed contractors' enthusiasm for invention and innovation and lowered awareness and reporting of inventions.

The amended bill changes this policy. Now universities, other nonprofit organizations and small businesses can retain title to inventions made under government contracts if, within a reasonable time after an invention's disclosure to a government agency, the organization or business elects to do so. Title can revert to the government if the organization doesn't report an invention, elect to take title of it or apply for a patent within a reasonable time.

If the contractor chooses not to retain title to an invention, the Patent and Trademark Office can award title to its individual inventor or inventors. To protect the contractor's business, however, the government can require a report on the invention, which it will treat as confidential information. Further, it can treat any commercial and financial information that the report includes as privileged and confidential and not subject to disclosure under the Freedom of Information Act.

The government can also require a contractor to grant a license in any field of use if the organization hasn't taken steps to practically apply the invention or if such a course is advisable for national health and safety reasons. The applicable section of the law also establishes guidelines for licensing of federally owned inventions and gives small businesses first choice in licensing them.

Avoiding validity problems

In addition to ownership questions, patents must face validity tests. And although inventors, businessmen and attorneys try to avoid long, drawn-out and expensive litigation involving patent validity, the patent law has all too often led to such entanglements. Under that law, interested parties must initially deal with the Patent and Trademark Office, which is charged with issuing valid patents. Then, after a patent issues, if anyone presents new references to challenge its validity, a federal court must settle the question.

Therefore, to minimize this process's cost and burden, the amended law institutes a re-examination provision. It states that any person can at any time cite to the Patent and Trademark Office patents or publications related to the patentability of any claim and file a re-examination request. When a substantial new question of patentability arises, the Patent Commissioner orders re-examination proceedings, which must be conducted with special dispatch within the Office, from examination through appeal.

Supporters of the revised law herald this section as a boon to innovation and business. Whether it will be, however, remains unclear. The re-examination cost, for example, ranges from $1000 to $1500, and no provision mandates that the courts accept the Patent and Trademark Office's re-examination findings any more readily than they have accepted those for original examinations in the past.

Some recent cases, in fact, indicate that the courts don't easily accept such a substitute for their own investigation and consideration of a case's underlying facts. Consequently, the re-examination procedure could merely add to the expense of obtaining a patent.

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An area in which the law's revisions are more

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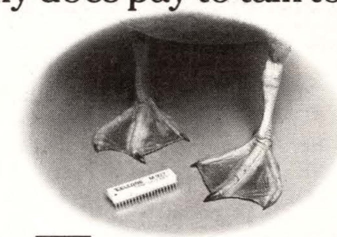

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CIRCLE NO 64

Copyright bill *implies* software protection

encouraging, however, is software protection. The Copyright Office has been accepting computer programs for registration, yet questions on whether they are or should be copyrightable and the scope of protection afforded them are unsettled. However, this new version of the law attempts to assure software's copyrightability, by implication at least, by referring to a computer program's owner as a copyright owner.

It also amends the copyright law to define a computer program as a set of statements or instructions to be used directly or indirectly in a computer to bring about a particular result. Further, the revisions explain certain acts that don't infringe on a copyrighted computer program. For instance, they establish that the owner of a software product can copy or authorize copying or adapting that product without infringing on the copyright owner's rights if either of two conditions applies:

- Such action constitutes an essential step in using the program with a machine
- The new copy will serve archival purposes only.

The law's copyright segment, although encouraging in many respects, could have little impact on the copyrightability of computer programs. And those sections that increase the cost of patent-application processing and enforcement could significantly affect the number of inventions reported and protected. Such increases could chill interest in both patent quality and innovation. All things considered, then, the portion of the law that places patent title in the hands of the inventor rather than the government holds the greatest potential for stimulating invention and innovation. **EDN**

Author's biography

Joseph S Iandiorio is an attorney specializing in patent, trademark, copyright and trade-secret law, practicing in Waltham, MA. Chairman of the Massachusetts Small Business Task Force, he serves on the Advisory Council to the University of Massachusetts Business School and is on the faculty of the Center for Entrepreneurial Management. Joe is also a director of the Smaller Business Association of New England and the Massachusetts Technology Development Corp and serves on congressional task forces.

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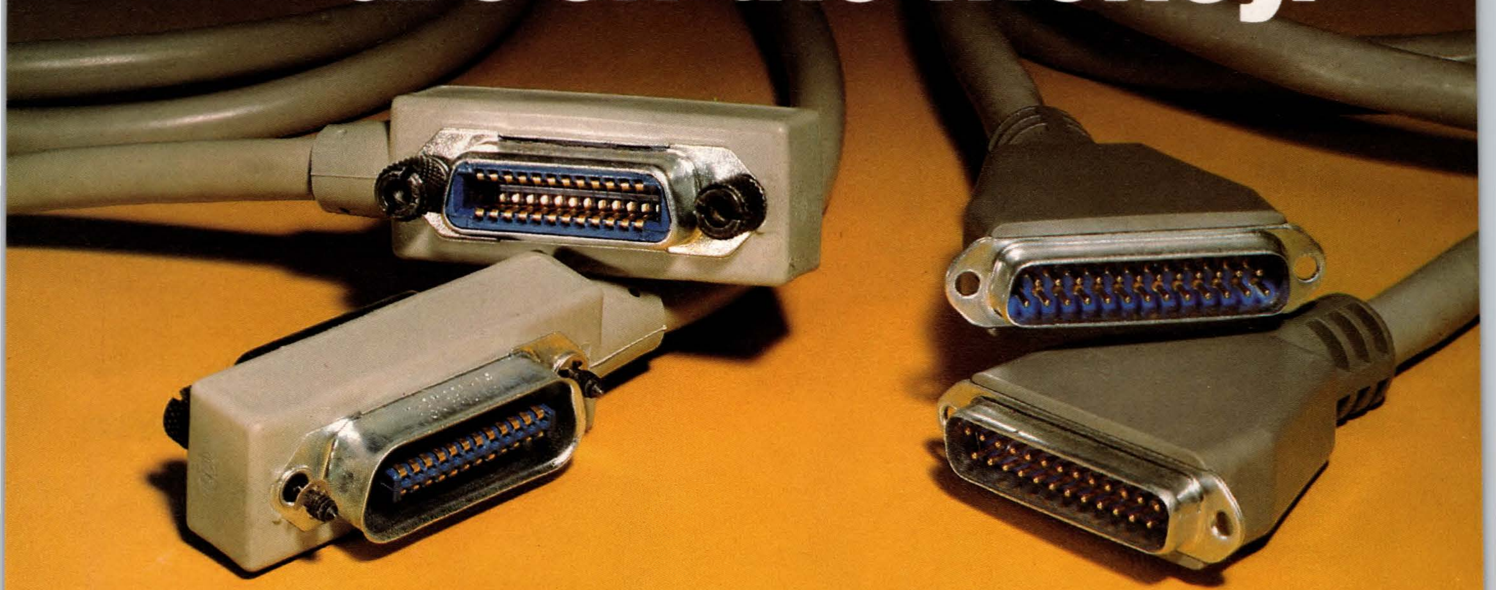

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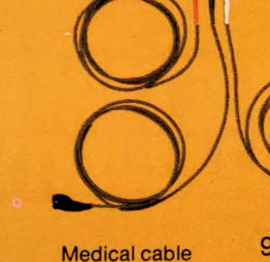

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CIRCLE NO 67

Display-list processor extends color-graphics tools

Combining point and line primitives with basic geometric transformations permits execution of graphics functions as if they were machine instructions.

Robert D Grappel, Consultant,
and **Jack E Hemenway,** Consulting Editor

The previous article in this series (EDN, May 27, pg 131) discussed the basic point and line primitives for color graphics, using the Radio Shack TRS-80 Color Computer as a hardware foundation. Here, we extend these primitives, drawing arbitrary shapes and moving them around the screen. The result is a small yet powerful display-list processor—a sort of metaprocessor that handles graphics.

Extending the primitives

The primitive operations permit placing points and lines at particular screen coordinates. Generalizing these operations would permit moving shapes around the screen without having to worry about absolute locations. Some basic mathematics helps with the generalization. Specifically, three transformation operations perform all possible movements in a plane: translation, scaling and rotation. In combination, these operations provide any graphics function needed in this simple model.

Translation **(Fig 1a)** shifts points by adding constants to their coordinates. If T_x and T_y are the constants of translation, two formulas describe the operation:

$$x' = x + T_x$$
$$y' = y + T_y.$$

Scaling **(Fig 1b)** multiplies a figure's coordinates by a specified factor, enlarging or shrinking the coordinate scales. If S_x and S_y are the scaling constants, two formulas describe this operation:

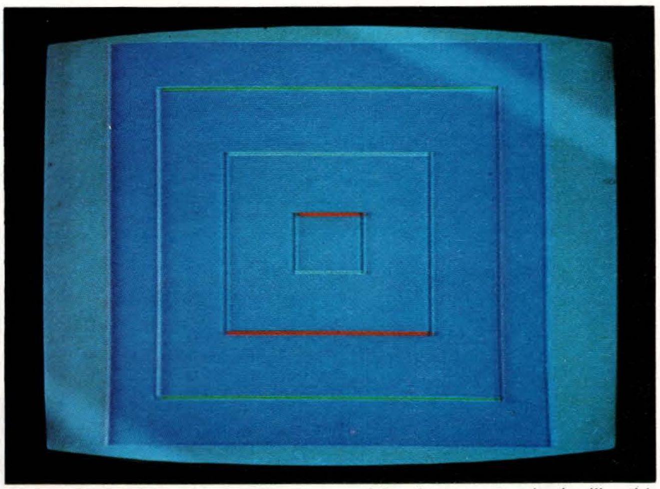
$$x' = xS_x$$
$$y' = yS_y.$$

Because S_x and S_y need not be equal, scaling can produce distortions, such as converting circles into ellipses. And if $S_x = -1$, the result is a mirror image of the original object.

Rotation **(Fig 1c)** is the most complicated of the three transformations; it describes a clockwise turning of the coordinate axes through a specified angle θ:

$$x' = x\cos\theta + y\sin\theta$$
$$y' = y\cos\theta - x\sin\theta.$$

Unlike translation and scaling, rotation is described by one parameter. And for a given angle, you need calculate the trigonometric functions only once. Note, however, that this description is limited to rotations about the origin.



The output of Fig 3's software graphics interpreter *looks like this when the interpreter utilizes the DATA statements in lines 45 to 51. This photo illustrates how you can build up a complex drawing using* ***Fig 2****'s 11 graphics commands, much as you would execute complex mathematical functions as combinations of a μP's machine-language instructions.*

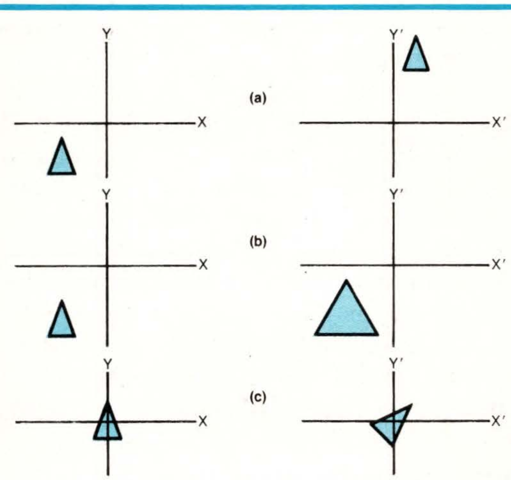


Fig 1—Three types of transformations *represent all movements in 2-dimensional space: translation* ***(a)****, scaling* ***(b)*** *and rotation* ***(c)****.*

Three transformations provide all 2-dimensional movements

Graphics "instructions" build pictures

To increase graphics capabilities, you must combine the basic graphics primitives of point and line with the three transformations. The concept of a graphics "instruction" helps with this task; it allows you to build a more powerful computer that's able to perform transformations, draw lines, plot points and perform other graphics tasks as though they were actual machine instructions. However, the approach taken here is not to build a new μP to do this job (although that could be done in hardware). Instead, we construct a graphics-language interpreter in software. The use of such software interpreters to build new "machines" out of old ones is common: The P machine used by many PASCAL implementations, the pseudostack machine used in FORTH-type languages and even BASIC are examples that extend machine languages.

A possible first-cut attempt at designing the instruction set of a graphics machine appears in **Fig 2.** The set consists of 11 instructions and is by no means exhaustive; we ignore such thorny problems as the size and type of instruction parameters and how the instructions get stored. The choice of instructions is merely illustrative—no doubt many other instruction sets would have advantages compared with this one. After all, no "best" μP instruction set exists, either.

Display lists—memory for the graphics machine

Just as μP instructions reside in memory locations, so the graphics machine's instructions must occupy a space. Assume that each instruction takes up one to four locations, depending on how many parameters it requires. Instructions get stored sequentially in display lists, which you can think of as descriptions of the steps required to draw a particular object on the screen. In other words, just as a μP program is a description of how to perform some task (written in instructions that the μP understands), a display list is a description of an object (written in graphics instructions).

Fig 2's graphics instruction set divides into six "families," described as Machine Control, Absolute Addressing, Move, Draw and Plot, Subroutine Support and Transformations. A look at each is in order.

Instructions 1 (CLEAR-SCREEN) and 11 (EXIT) form the Machine Control family. The first wipes the slate clean in preparation for a new picture; it requires a single parameter—the color desired for the background. The second indicates to the interpreter, which actually executes the display list, that the end of the list is at hand. (Recall that handling display lists is only one of the tasks of the μP operating under all this software.)

Instruction 2 (HOME) is the only Absolute Addressing instruction. To be able to easily move around the screen, every line and point shouldn't be absolutely specified. Rather, it's more efficient to specify them relative to something. (This process is analogous to position-independent programs resulting from relative addressing.) Another view of this process is that the translation transformation gets built into the structure of the graphics machine. That is, the machine has a sort of "register," called the "current position" or "cursor," and all graphics operations get defined relative to this cursor position. Thus, only one absolute instruction provides an anchor in display space—a way to place the cursor at a known point. HOME serves this function, placing the cursor at the origin of the coordinate axes (a logical place to start from).

With the anchor defined, all subsequent moves around the screen occur through the MOVE-RELATIVE instruction (number 3). This instruction requires two parameters: the X- and Y-move steps relative to the cursor, which gets updated to the new position. MOVE-RELATIVE is like a relative-branch instruction in a μP; it causes processing to move to some new location relative to the branch's location. MOVE-RELATIVE is the only instruction (other than HOME) that changes the cursor position.

Instructions 4 and 5 (PLOT-POINT and DRAW-LINE), the other Move-family instructions, actually put something visible on the screen. These instructions are the hooks to the basic primitives developed in the previous article. PLOT-POINT takes three parameters: the relative X and Y steps from the cursor, which define the desired point, and the point's color. DRAW-LINE also takes these same three parameters, except that in its case a line of the specified color gets drawn between the cursor and the specified point. Neither instruction moves the cursor.

Instructions 6 and 7 (CALL and RETURN) form the Subroutine Support family. The graphics machine needs subroutines every bit as much as a μP does. For example, you might frequently want to draw the same object at more than one spot on the screen. Because every object (set of lines and points) is defined relative to the cursor, moving the cursor to the desired spot allows the entire object to be drawn there. With a set of frequently used objects built up as subroutines, you can draw them whenever and wherever you wish, merely by calling the appropriate subroutine.

CALL takes as its parameter the location in the display list where such a subroutine begins. RETURN

	MNEMONIC	PARAMETERS
1.	CLEAR-SCREEN	BACKGROUND COLOR (0-8)
2.	HOME	
3.	MOVE-RELATIVE	X, Y DISPLACEMENTS
4.	PLOT-POINT	X, Y DISPLACEMENTS, COLOR (0-8)
5.	DRAW LINE	X, Y DISPLACEMENTS, COLOR (0-8)
6.	CALL	ADDRESS OF SUBROUTINE
7.	RETURN	
8.	SET-ANGLE	ROTATION ANGLE (RADIANS)
9.	SCALE-X	X SCALING FACTOR
10.	SCALE-Y	Y SCALING FACTOR
11.	EXIT	

Fig 2—A proposed set of 11 instructions *for a graphics machine provides a large amount of graphics power when interpreted by appropriate software or built into a special hardware processor.*

ends the subroutine and returns to the next instruction following the CALL. These instructions require that the graphics machine have a stack on which to save subroutine return addresses; you want the ability to nest subroutines as you build up complex pictures.

One immediate example of the use of subroutines in graphics involves placing characters on the screen. You don't want to be limited to specific screen locations or orientations, and you might want different character sizes, characters oriented at various angles and mirrored characters, to name a few options. To gain this flexibility, you can define each character as a subroutine with points and lines plotted relative to a cursor position at the character's lower left. Then you can precisely control the character's placement.

The last three instructions (SET-ANGLE, SCALE-X and SCALE-Y) form the Transformations family and add the scaling and rotation transformations to the graphics machine. SET-ANGLE defines the desired angle of rotation for subsequent operations; SCALE-X and SCALE-Y define the desired scaling components for those operations. Providing these transformations requires that every relative operation include computations that incorporate scaling and rotation values. In this machine, we assume that the following equations describe the scaling and rotation transformations (recall that translation is already built in):

$$x' = S_x(x\cos\theta + y\sin\theta)$$

$$y' = S_y(y\cos\theta - x\sin\theta)$$

This treatment isn't entirely general because it always scales after rotation. But generalizing the transformation mechanism to accommodate scaling before rotation, while desirable, requires more complex mathematics and will be ignored here.

```
1 ' SIMPLE GRAPHICS-MACHINE LANGUAGE INTERPRETER
2 ' FOR THE TRS-80 COLOR COMPUTER
3 ' WRITTEN IN EXTENDED COLOR-BASIC
4 '
5 PMODE 1,1: SCREEN 1,1: ' SET UP FOR HIGH RES.
10 DIM STACK(100), DLIST(200)
20 XOFF=128: YOFF=96: SP=1
25 FOR J=1 TO 100: ' LOAD THE DISPLAY LIST
30 READ DLIST(J)
35 NEXT J
40 IP=1: GOSUB 850: STOP: ' DISPLAY THE LIST
42 '
43 ' DISPLAY LIST FOR 3 CONCENTRIC SQUARES
44 '
45 DATA 1,7,2,10,0.75,3,100,100,5,-200,0,2
46 DATA 3,-200,0,5,0,-200,5,3,0,-200,5,200,0,6
47 DATA 3,200,0,5,0,200,4,2,3,60,60,5,-120,0,5
48 DATA 3,-120,0,5,0,-120,2,3,0,-120,5,120,0,4
49 DATA 3,120,0,5,0,120,6,2,3,20,20,5,-40,0,4
50 DATA 3,-40,0,5,0,-40,6,3,0,-40,5,40,0,5,3,40
51 DATA 0,5,0,40,2,11,0,0,0,0,0

200 '
210 ' PUSH "V" ONTO STACK
220 '
230 STACK(SP)=V: SP=SP+1: RETURN

300 '
310 ' POP "V" FROM STACK
320 '
330 SP=SP-1: V=STACK(SP): RETURN

400 '
410 ' COMPUTE MIDPOINTS OF M1 AND M2
420 ' MD=ROUNDED DOWN, MU=ROUNDED UP
430 '
440 M=(M1+M2)/2
450 MU=INT(M+0.9): MD=INT(M): RETURN

500 '
510 ' PLOT A LINE FROM (X1,Y1) TO (X2,Y2) COLOR C
520 '
530 TSP=SP: ' INIT. STACK POINTER
540 IF X1<>X2 THEN 610
550 IF Y1<>Y2 THEN 610
560 PSET(X1+XOFF,Y1+YOFF,C): ' PLOT THIS POINT
570 IF SP=TSP THEN RETURN: ' IF STACK EMPTY, THEN DONE!
575 ' ELSE POP LAST LINE SEGMENT
580 GOSUB 300: Y1=V: GOSUB 300: X1=V: ' POP START-PNT.
590 GOSUB 300: Y2=V: GOSUB 300: X2=V: ' POP END-PNT.
600 GOTO 540
610 V=X2: GOSUB 200: V=Y2: GOSUB 200: ' PUSH END-PNT.
620 M1=X1: M2=X2: GOSUB 400: ' COMPUTE MIDPOINT-X
630 IF X2>X1 THEN 650
640 X2=MU: V=MD: GOSUB 200: GOTO 660
650 X2=MD: V=MU: GOSUB 200
660 M1=Y1: M2=Y2: GOSUB 400: ' COMPUTE MIDPOINT-Y
670 IF Y2>Y1 THEN 690
680 Y2=MU: V=MD: GOSUB 200: GOTO 540
690 Y2=MD: V=MU: GOSUB 200: GOTO 540

800 '
810 ' PROCESS DISPLAY LIST HERE
820 ' "IP" IS THE INSTRUCTION POINTER
825 ' (CX,CY) IS THE CURSOR POSITION
830 ' SX,SY ARE THE SCALING PARAMETERS
835 ' ST,CT ARE THE ROTATION VALUES
840 '
850 I=DLIST(IP): ' GET THE INSTRUCTION (1-11)
855 ON I GOTO 900,920,940,960,980,1000,1020,1040,
        1060,1080,1100
860 STOP: ' ERROR IF IT GETS HERE

900 ' PROCESS "CLEAR-SCREEN" INSTRUCTION
905 SX=1: SY=1: CT=1: ST=0
910 PCLS(DLIST(IP+1)): IP=IP+2: GOTO 850

920 ' PROCESS "HOME" INSTRUCTION
930 CX=0: CY=0: IP=IP+1: GOTO 850

940 ' PROCESS "MOVE RELATIVE" INSTRUCTION
945 X1=DLIST(IP+1): Y1=DLIST(IP+2)
950 GOSUB 2000: ' TRANSFORM (X1,Y1)
955 CX=CX+X2: CY=CY-Y2: IP=IP+3: GOTO 850

960 ' PROCESS "PLOT-POINT" INSTRUCTION
962 X1=DLIST(IP+1): Y1=DLIST(IP+2)
964 GOSUB 2000: ' TRANSFORM (X1,Y1)
966 X2=CX+X2: Y2=CY-Y2
968 C=DLIST(IP+3): ' GET COLOR OF POINT
968 PSET(X2+XOFF,Y2+YOFF,C)
970 IP=IP+4: GOTO 850

980 ' PROCESS "DRAW-LINE" INSTRUCTION
982 X1=DLIST(IP+1): Y1=DLIST(IP+2)
984 GOSUB 2000: ' TRANSFORM (X1,Y1)
986 X2=CX+X2: Y2=CY-Y2
988 C=DLIST(IP+3): ' GET COLOR OF LINE
990 X1=CX: Y1=CY: GOSUB 530: ' DRAW LINE
995 IP=IP+4: GOTO 850

1000 ' PROCESS "CALL SUBROUTINE" INSTRUCTION
1010 V=IP+2: GOSUB 200: ' STACK RETURN ADDRESS
1015 IP=DLIST(IP+1): GOTO 850

1020 ' PROCESS "RETURN FROM SUBROUTINE" INSTRUCTION
1025 GOSUB 300: ' UNSTACK RETURN ADDRESS
1030 IP=V: GOTO 850

1040 ' PROCESS "SET-ANGLE" INSTRUCTION
1045 TH=DLIST(IP+1): ST=SIN(TH): CT=COS(TH)
1050 IP=IP+2: GOTO 850

1060 ' PROCESS "SCALE-X" INSTRUCTION
1065 SX=DLIST(IP+1): IP=IP+2: GOTO 850

1080 ' PROCESS "SCALE-Y" INSTRUCTION
1085 SY=DLIST(IP+1): IP=IP+2: GOTO 850

1100 ' PROCESS "EXIT" INSTRUCTION
1105 RETURN

2000 '
2010 ' SUBROUTINE TO ROTATE AND SCALE (X1,Y1)
2020 '
2030 X2=INT(SX*(X1*CT+Y1*ST))
2040 Y2=INT(SY*(Y1*CT-X1*ST))
2050 RETURN
```

Fig 3—A software interpreter *for the instruction set shown in* **Fig 2** *is implemented in Extended Color BASIC for the TRS-80 Color Computer. The subroutines in line 200 to 800 are almost identical to those in* **Fig 7** *of the previous article in this series (EDN, May 27, pg 131).*

A display list tells the steps required to draw an object

Implementing the graphics machine

Following our policy from the previous article, **Fig 3** illustrates an interpreter for **Fig 2**'s graphics instructions, written in BASIC on the TRS-80 Color Computer. This program uses the machine's Extended Color BASIC and requires at least 16k of memory. As we stated in the previous article, though, nobody would seriously consider writing a graphics machine in BASIC; it's much too slow and cumbersome for the task. Thus, we include **Fig 3**'s program only as an illustration.

Note that the previous article's stack subroutines and line-drawing subroutine are part of the interpreter. The stack routines serve in CALL and RETURN instruction processing as well as in the line-drawing routine—a fact that calls for some small changes in the line-drawing routine at the point where it checks to see that it has completely plotted a line. We've also enlarged the STACK array because it now serves two purposes.

The array DLIST forms the display list. An instruction-pointer pseudoregister resides in IP. Instructions get defined by their number from **Fig 2** and are interpreted by the subroutine starting at line 800. Calling that subroutine with IP set to the desired starting point in DLIST is like turning on the graphics machine. The multibranch GOTO instruction at line 850 decodes each instruction and calls the appropriate instruction handler, which jumps back to line 850. The only way out is to encounter an EXIT instruction, which causes a subroutine return back to the program that initially called the graphics-machine interpreter.

The subroutine at line 2000 performs the scaling and rotation transformations; all calculations of a relative location go through it. The scaling values SX and SY are set by SCALE-X and SCALE-Y instructions; the rotation values CT and ST, by the SET-ANGLE instruction. (CT is the cosine of the angle, and ST is its sine.) Note that this BASIC program requires specification of angles in radians. The CLEAR-SCREEN instruction initializes these values so that both scaling values are unity and the rotation angle is zero.

The remainder of the graphics-machine interpreter is fairly clear. Some of the special TRS-80 Color BASIC commands, such as PSET and PCLS, are merely extensions of the 4k BASIC commands used in the previous article. Statements such as PMODE and SCREEN, on the other hand, are specific to Extended Color BASIC; they are required to set up display mapping and program the internal 6847 graphics controller for increased screen resolution.

Get the static out

This graphics machine omits many features. Its most important failing is the lack of any dynamic instructions; every instruction takes its parameters from the display list, and once that list is written, the graphics machine displays it. Thus, there's no facility for changing the display dynamically.

That capability can prove useful. For example, suppose you want to draw a circle. It would be nice to be able to write a program for the graphics machine like the one shown in **Fig 4.** Note in this hypothetical program that the SET-ANGLE instruction takes its parameter value from a variable. And note the loop construct, which allows one SET-ANGLE and one PLOT-POINT instruction to form an entire circle. With capabilities like these, the graphics machine approaches a μP in complexity; it needs some form of internal registers, addressing modes, jump instructions and similar features. Additionally, some form of assembler proves useful when writing programs for it. In sum, the machine becomes quite complicated.

Hardware or software?

There must be some hardware/software tradeoff regarding how much of this graphics machine should be implemented in software and how much in hardware. Our interpreter program in BASIC is the software extreme: Recoding it in assembly language is the first step toward practicality. (Extended Color BASIC contains all the features of our graphics machine as internal primitives.) The interpreter overhead isn't too bad when you consider that most of the time is spent in the line-drawing and plotting code. The transformation routines involve a fair amount of math, so they are the next spot to attack. At first, the sine and cosine functions might seem difficult, but algorithms exist to speed them up, even on μPs. (EDN, March 18, pg 186 presents a CORDIC-algorithm solution to sine and cosine generation in less than 200 bytes of 8086 code.)

```
PI=3.14159: DTR=2*PI/360
FOR R1=0 TO 360: ' CIRCLE IS A SET OF POINTS
SET-ANGLE (R1 * DTR)
PLOT-POINT (RADIUS,0,COLOR)
NEXT R1
```

Fig 4—Adding loop constructs and dynamic instructions *to the graphics machine provides additional capabilities. This routine shows how easy it would be to draw circles using such features.*

At the other extreme, many commercial graphics computers move the entire display-list processor into hardware. Using bit-slice μPs with custom microcoding, they achieve the performance necessary to generate complex pictures in real time. And as an alternative to building a special μP, some designers use a multiprocessor approach, with a μP or minicomputer building the display list and a second μP interpreting it.

More than meets the eye

This article and the previous one might appear to have covered a lot of ground, but graphics is a much broader subject than could be possibly covered in less than a hefty book. Consider for a moment the set of concepts we've omitted.

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Dynamic instructions and other refinements add power

the screen? In our BASIC implementation, you get an FC (function call) error, and the program aborts—not a good way to handle the situation. As an alternative, you could check every point to ensure that it's on the screen. An extension of this concept is termed "clipping;" it allows the display-list objects to move around but displays only the points that actually lie on the screen. Extending this concept still further, suppose you had a "window" that could move around; you could arrange matters so the screen showed just what is visible through that window. It's not easy: The objects in the display list and the window itself might be moving, yet the screen must show a "snapshot" of the objects as they would appear through the window. You might also want the window to change shape, independent of the scaling occurring in the display.

So far, all operations have taken place in two dimensions. But what happens when two or more objects collide? In the TRS-80 Color Computer (and most machines using raster-scan graphics), the last pixel plotted wipes out any older one. Hence, the order in which you plot objects is important. In effect, the last-plotted items lie "in front" of older items. Thus, although this analysis considers a 2-dimensional plot, we are actually producing "3-dimensional" objects—a consideration that adds a whole layer of complications.

Additionally, everything done so far has used only lines and points. But what if you want to add color in areas? In that case, the graphics machine needs some FILL or PAINT instructions. Determining whether a given point is inside or outside a specified region is no easy task for a μP. Adding these instructions to the graphics machine while maintaining generality thus proves difficult, and some compromises are usually required.

Finally, true 3-dimensional (perspective) graphics adds still further complications. Issues such as perspective, hidden lines and complex curved surfaces make the 2-dimensional problems seem easy by comparison. As expected, this is an area encompassing much new work and research.

Do it yourself

Considering the rich possibilities, these two articles on color graphics have probably only whetted your appetite for information. And the program examples presented are only a starting point. Articles describing the creative use of graphics with μPs are sure to appear in the pages of EDN and elsewhere in the future. EDN

Author's biography

Robert D Grappel is vice president of Hemenway Associates Inc, Boston, MA.

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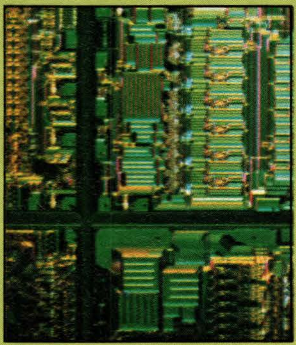

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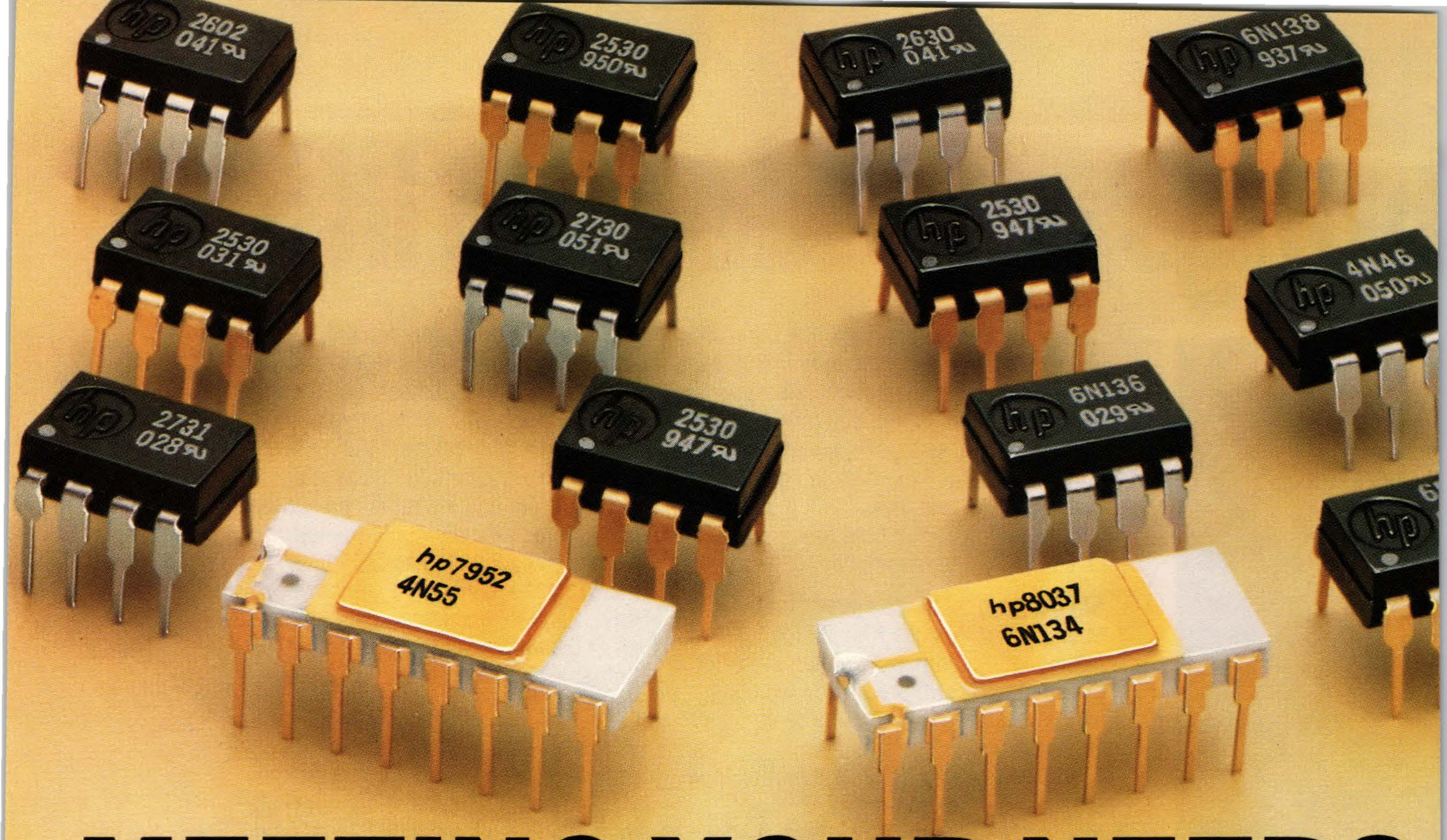

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Piezoceramics plus fiber optics boost isolation voltages

Overcoming traditional magnetic-transformer drawbacks, a novel isolation-amplifier design hikes voltage-breakdown limits more than tenfold by incorporating a piezoceramic-based acoustic transformer and a fiber-optic link.

Jim Williams, National Semiconductor Corp

When standard parametric or isolation amplifiers don't adequately isolate or protect your analog measurement systems, the circuit design described in this article can help. Although typical isolation amplifiers achieve about a 2.5-kV max isolation voltage, this one can handle 20- to 100-kV breakdown limits. It incorporates a piezoceramic material structured as an acoustic transformer and a fiber-optic lightpipe.

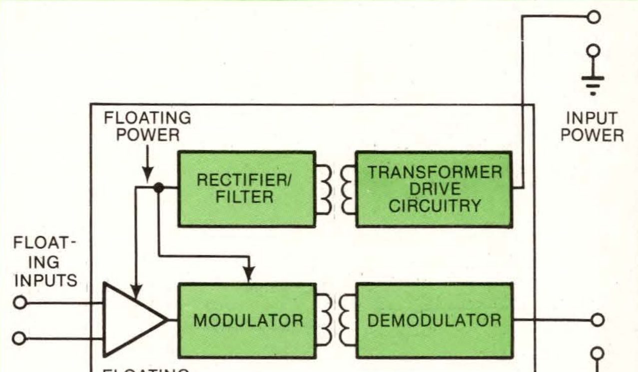


Fig 1—A traditional isolation amplifier *uses dual transformers to separate the input-signal line from the power and output-signal lines. This approach typically results in about a 2.5-kV max input-isolation voltage.*

Isolation amplifiers find use mainly in assuring safe and reliable analog measurements. They surmount the problems of high common-mode voltages in applications such as medical test instruments and completely isolate or interrupt ground loops or paths in equipment such as that used in industrial process-control systems.

Designing isolation amplifiers mandates careful attention to two key factors: isolating the power supply from the input-signal line and galvanically separating the input- and output-signal lines. The first half of the task generally involves the most effort.

Input isolation proves complex

Conventional isolation amplifiers employ a magnetic transformer to convey power to the circuit's floating front end **(Fig 1).** Although this transformer galvanically separates the power supply from the input terminals, it increases in size and cost when common-mode voltages exceed about 2.5 kV. Moreover, its leakage currents can total as much as 2 μA.

To separate the input- and output-signal lines, conventional isolation amplifiers modulate the floating front end's output onto a carrier signal. This signal traditionally passes via another magnetic transformer to the circuit's output terminals. Modulation schemes include pulse width, pulse amplitude and voltage to frequency. Here again, though, magnetic transformers become bulky and inefficient as common-mode voltages and leakage currents rise. And isolation limits depend

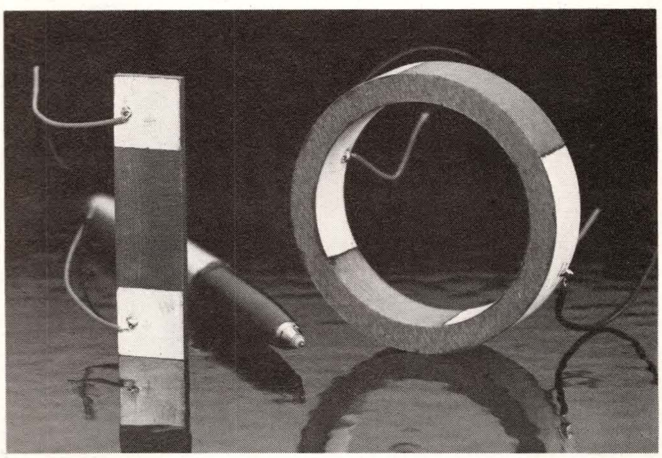


Fig 2—Able to perform as acoustic transformers, *piezoceramic materials come in various sizes and shapes, such as this thin bar and thick toroid (shown with a ballpoint pen for dimensional reference). Observe that two pairs of leads make input and output connections to each piece of piezoceramic material.*

Traditional isolation amplifiers employ magnetic transformers

on the transformer's breakdown rating.

Even when an optoisolator replaces the modulation transformer with a frequency- or light-intensity-coding approach, power requirements for operating the floating front end still require the power transformer. What's more, optoisolators arc under excessive common-mode voltages.

Other methods for transmitting electrical energy with high isolation exist, such as using microwave devices and solar cells, but they prove expensive, inefficient and impractical. Batteries are an alternative power source, but they have maintenance and reliabiliy limitations.

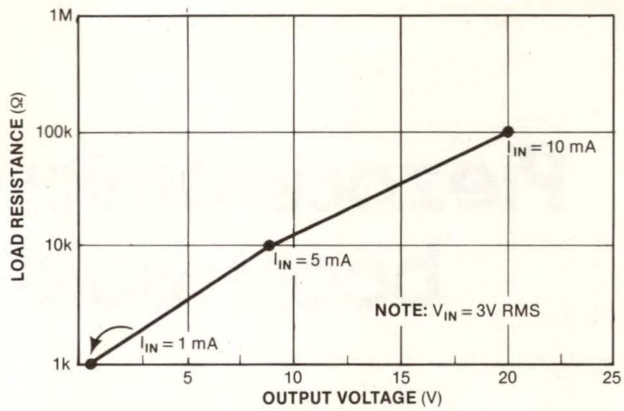
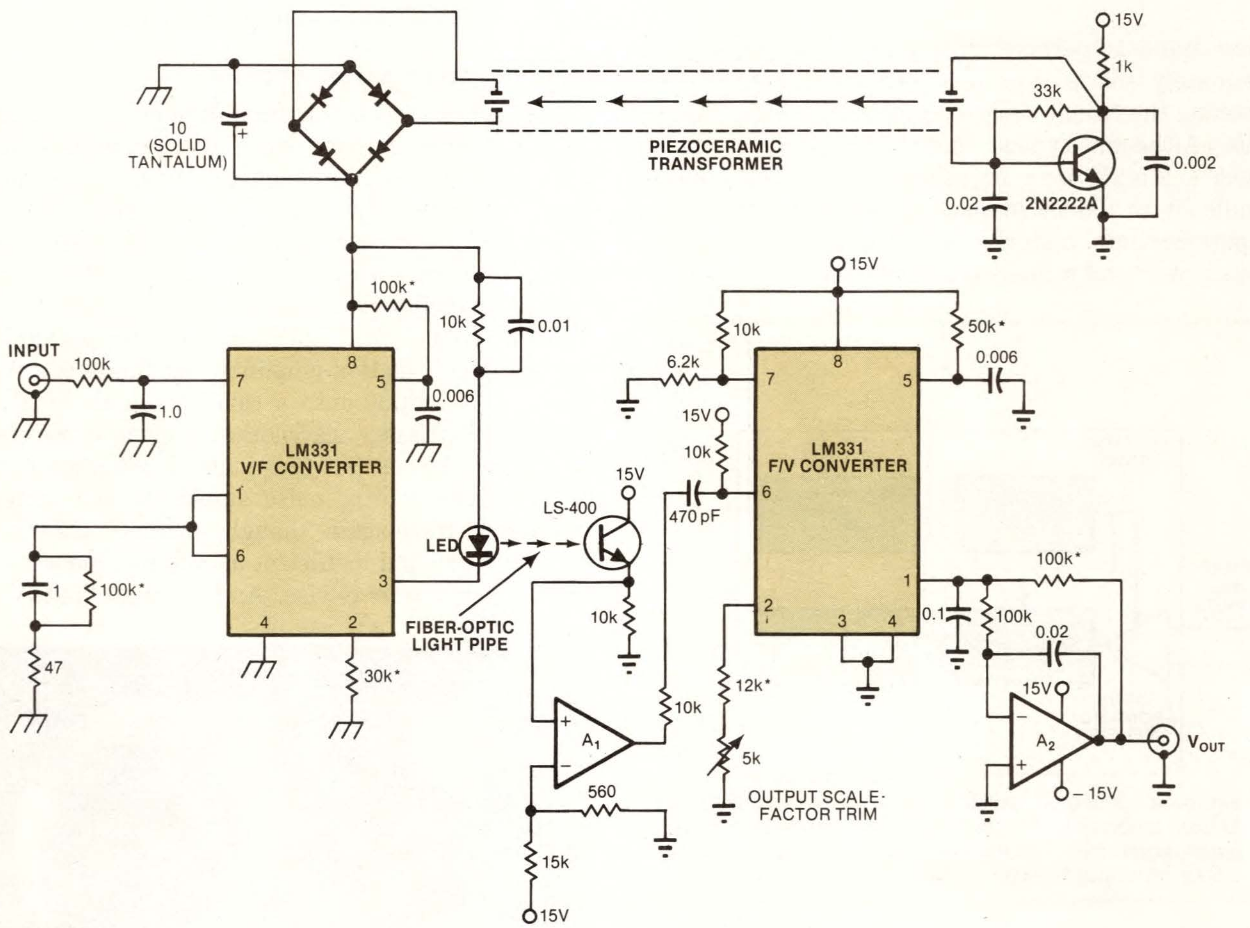


Fig 3—This typical load line *traces an acoustic transformer's performance at resonance. Note that for a constant 3V rms drive voltage and a varying 1- to 100-kΩ load resistance, the acoustic transformer draws up to 10 mA as its output voltage increases to 20V.*



NOTES:
A_1, A_2 = LF353 DUAL
ALL DIODES = 1N4148
* = 1% METAL-FILM RESISTOR
= FLOATING COMMON
= AMPLIFIER GROUND
CAPACITORS IN μF UNLESS NOTED

Fig 4—An innovative isolation-amplifier design *employs piezoceramic material as an acoustic transformer and a fiber-optic lightpipe to separate the input-signal line from the power and output-signal lines, respectively. In this approach, breakdown-voltage limits escalate to 20 to 100 kV.*

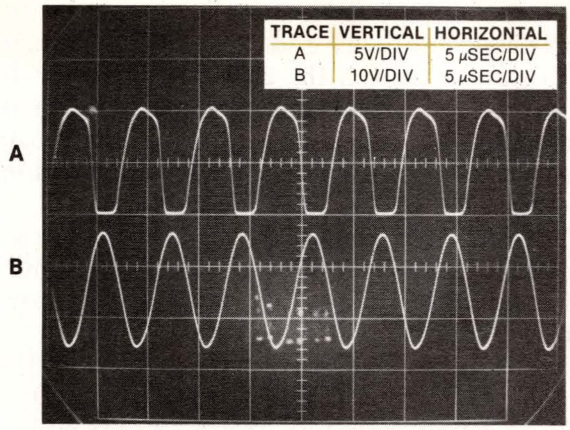


Fig 5—The 2N2222A transistor's output *(from **Fig 4**'s circuit) shows an irregularly shaped sine wave (trace **A**) delivered to the acoustic transformer's input. The transformer's high-Q properties cause it to filter and amplify the waveform into a smooth sinusoid **(B)** at its output.*

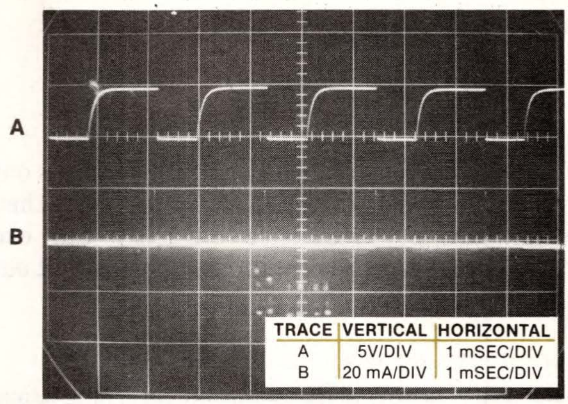


Fig 6—Trace A depicts the LM331 voltage-to-frequency converter's output *(from **Fig 4**'s circuit). This output drives the LED that couples to the fiber-optic lightpipe. Trace **B** indicates the LED's current waveform. Whenever the converter's output is LOW, the LED saves power by passing an extremely narrow (20 mA) light-encoded pulse.*

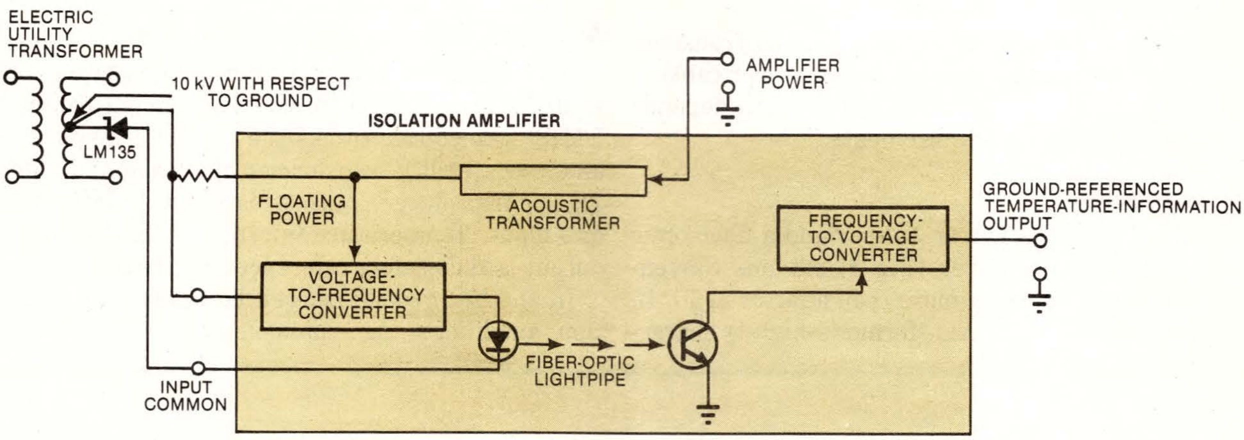


Fig 7—To monitor an electric-utility transformer's winding temperature, *this acoustic-transformer-based isolation amplifier permits the LM135 temperature sensor—which floats at 10 kV—to generate a safe ground-referenced output.*

Acoustic transformers surpass magnetic types

To achieve very high common-mode voltage but extremely low leakage current, the ideal electrical energy transfer device should permit easy implementation, operate efficiently and inexpensively and provide virtually complete isolation.

An acoustic transformer meets these goals by taking advantage of certain ceramic materials' piezoelectric characteristics. Although piezoelectric materials have long been recognized as electric-to-acoustic and acoustic-to-electric transducers (eg, microphones and buzzers), their use for electric-to-acoustic-to-electric energy conversion has not been emphasized. This conversion sequence capitalizes on ceramic materials' unique conductive nature; they furnish excellent electrical-insulation and acoustic-conduction properties.

In an acoustic transformer, acoustic waves and nonconducting piezoceramics serve in place of a conventional transformer's magnetic flux and conductive core. **Fig 2** shows two acoustic-transformer types; you make either type by merely bonding a pair of leads to each end of the piezoceramic material.

Tests reveal that this material's electrical resistance exceeds $10^{12}\Omega$; primary-to-secondary capacitance typically measures a few picofarads. The material's physical properties and configuration determine its resonant frequency as a transformer.

In operation, an acoustic transformer employs an oscillator-driven piezoelectric resonator at one end of the ceramic material. The resonator sends acoustical energy along the material at about 150 kHz. At the other end, an identical resonator receives the acoustical energy and converts it back to electrical energy. After rectification and filtering, the electrical energy powers the isolation amplifier's front end.

With this approach, isolation amplifiers can achieve breakdown limits greater than 20 kV, using piezoceramic material 0.25 to 12 in. long. In fact, meticulous designs have achieved isolation voltages as high as 100 kV.

As an additional advantage, acoustic transformers cost less than their magnetic counterparts. Further, they possess higher operating efficiency because the piezoceramic material is tuned to its natural resonance

An acoustic transformer isolates the power supply from the input

point.

Fig 3 depicts a typical acoustic transformer's output characteristics when driven at resonance. Note that the transformer's power-transfer efficiency can exceed 75%, depending on load conditions. Short-circuit output current for this device equals 35 mA.

Fiber optics upgrades input/output isolation

The other key design factor in designing isolation amplifiers—nearly total input-to-output line separation—is accomplished via fiber optics by stretching both lines further apart than an optoisolator can. This optical-encoding method works as it would in a typical optoisolator, but with an increased distance between transmitter and receiver yielding higher isolation voltages.

In practice, a light-emitting diode (LED) transmits optically encoded signals through a single-fiber cable to a photodiode receiver. The exact cable length depends on the particular circuit requirements.

Put it all together

Combining an acoustic transformer and a fiber-optic link in an isolation amplifier **(Fig 4)** extends conventional breakdown limits by more than a factor of 10. In this circuit, the acoustic transformer's high-Q characteristics allow self resonance in a manner similar to that of a quartz crystal. Resonance eliminates the need for a stable oscillator to drive the acoustic transformer.

To start operation, the 2N2222A transistor excites the piezoceramic transformer's primary **(Fig 5)**. At the secondary, four diodes and a capacitor rectify and filter the transformer's electrical output. This output in turn energizes the LM331 V/F converter.

The converter transforms its amplitude-based input signal into a frequency-based output. This signal then drives an LED, whose output travels along a fiber-optic cable.

Each time the V/F converter's output goes LOW, a narrow (20-mA) spike passes through the LED via the 0.01-μF capacitor **(Fig 6)**. This short duty cycle keeps the average current value small, minimizing power requirements.

At the receiver end, a photodiode detects the light-encoded signals. It in turn passes the signals to the LM331 for demodulation.

Amplifier accommodates varied uses

An acoustic-transformer/fiber-optic isolation amplifier finds use in diverse applications. In one example, an LM135 transducer tracks the winding temperature of an electric-utility transformer operating at 10 kV **(Fig 7)**. The transducer's output biases the isolation amplifier's input. Temperature information at the amplifier's output is thus safely referenced to ground.

In another ground-referenced application, the isolation amplifier's high-common-mode voltage blocking

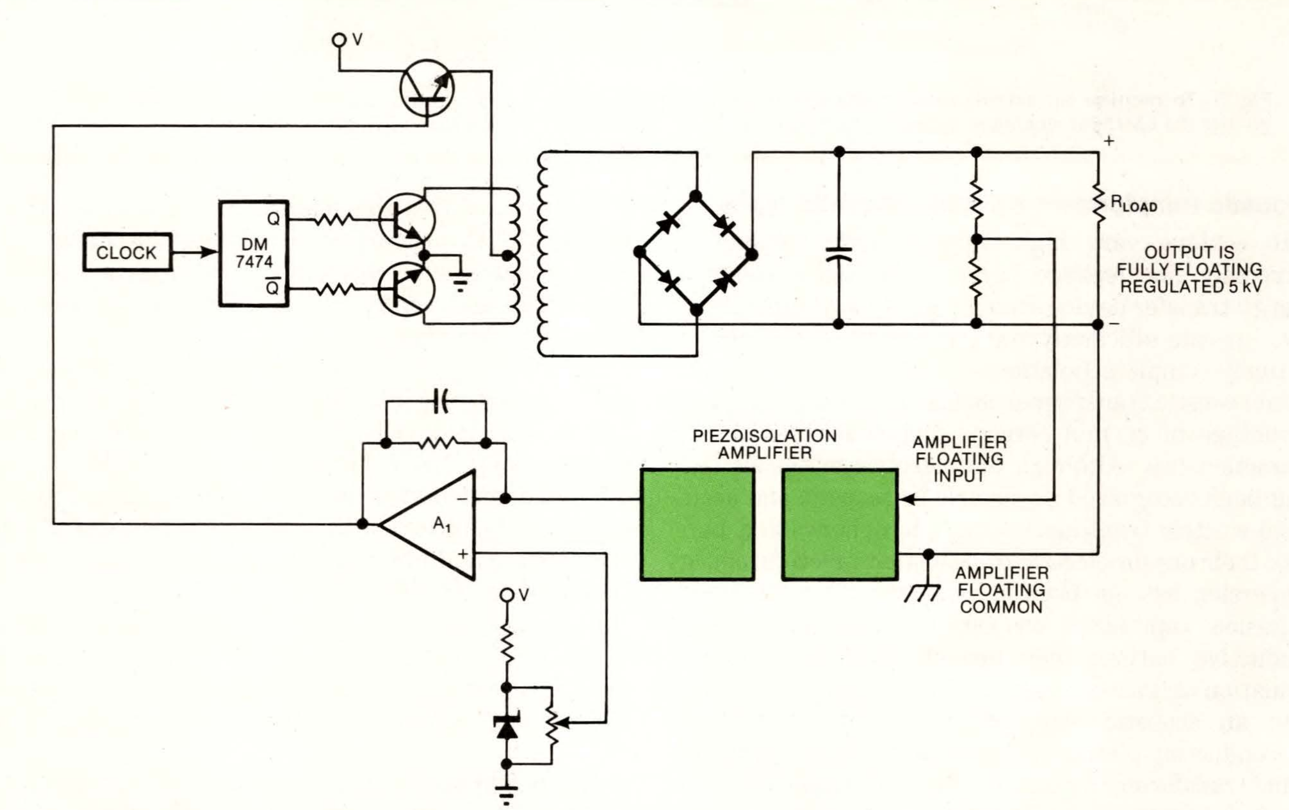
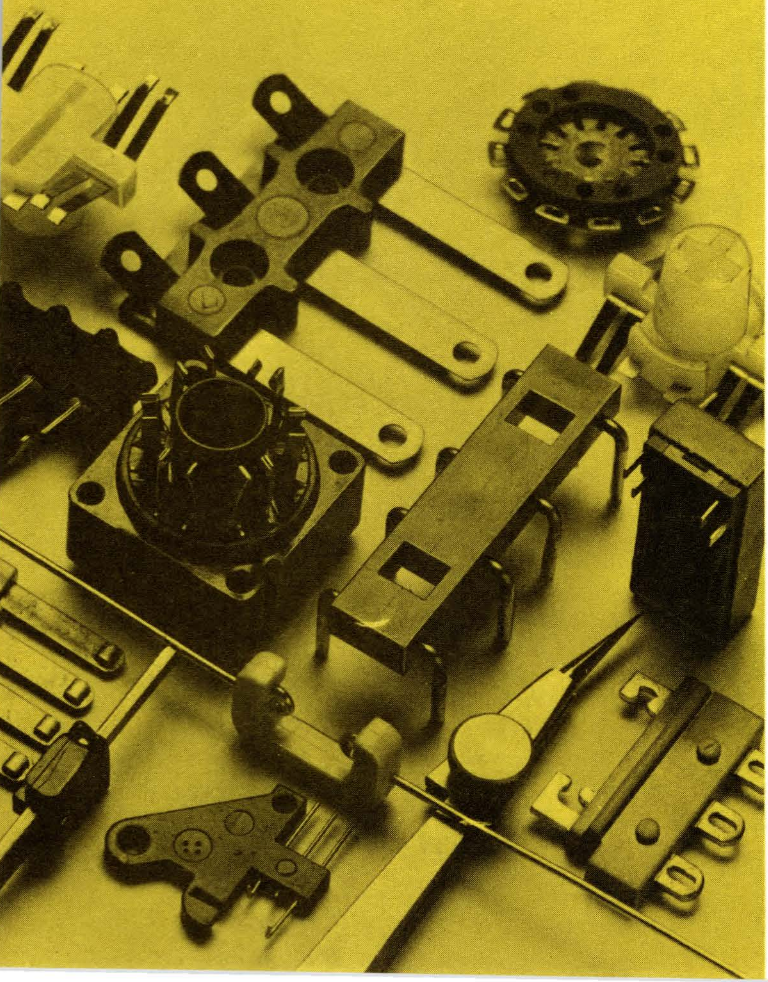


Fig 8—The piezoisolation amplifier *in this application provides a ground-referenced feedback path for the 5-kV regulated power supply. The power supply's output thus fully floats.*



A fiber-optic link galvanically separates output and input lines

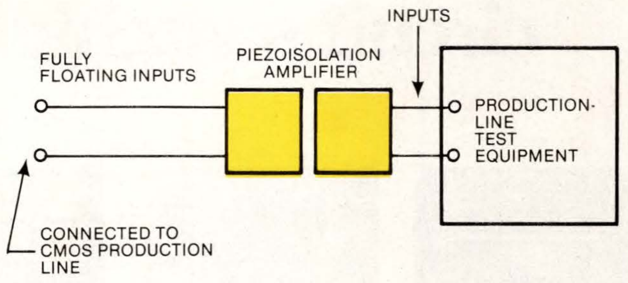


Fig 9—Production-line test equipment *for checking CMOS products is fail-safe isolated via a piezoisolation amplifier. This amplifier keeps static discharge away from the sensitive CMOS parts even when the test equipment develops a substantial charge.*

allows a 5-kV regulated power supply's output to fully float **(Fig 8).** Here, a push/pull dc/dc converter generates the high-voltage output. The isolation amplifier provides a ground-referenced output-feedback signal to op amp A_1, which controls the transformer's drive, completing the feedback loop.

For a fail-safe test application, an acoustic/fiber-optic amplifier isolates instrument inputs connected to CMOS ICs on a production line **(Fig 9).** This arrangement prevents static-discharge damage, even when the instruments have accumulated a substantial charge. **EDN**

References

Transducer Interfacing Handbook, Analog Devices Inc, Norwood, MA, 1980, pg 175.

Piezoceramic Catalog 761-01, Channel Industries Inc, Santa Barbara, CA, 1980.

Author's biography

Jim Williams, applications manager with National Semiconductor's Linear Applications Group (Santa Clara, CA), specializes in analog-circuit design and instrumentation development. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

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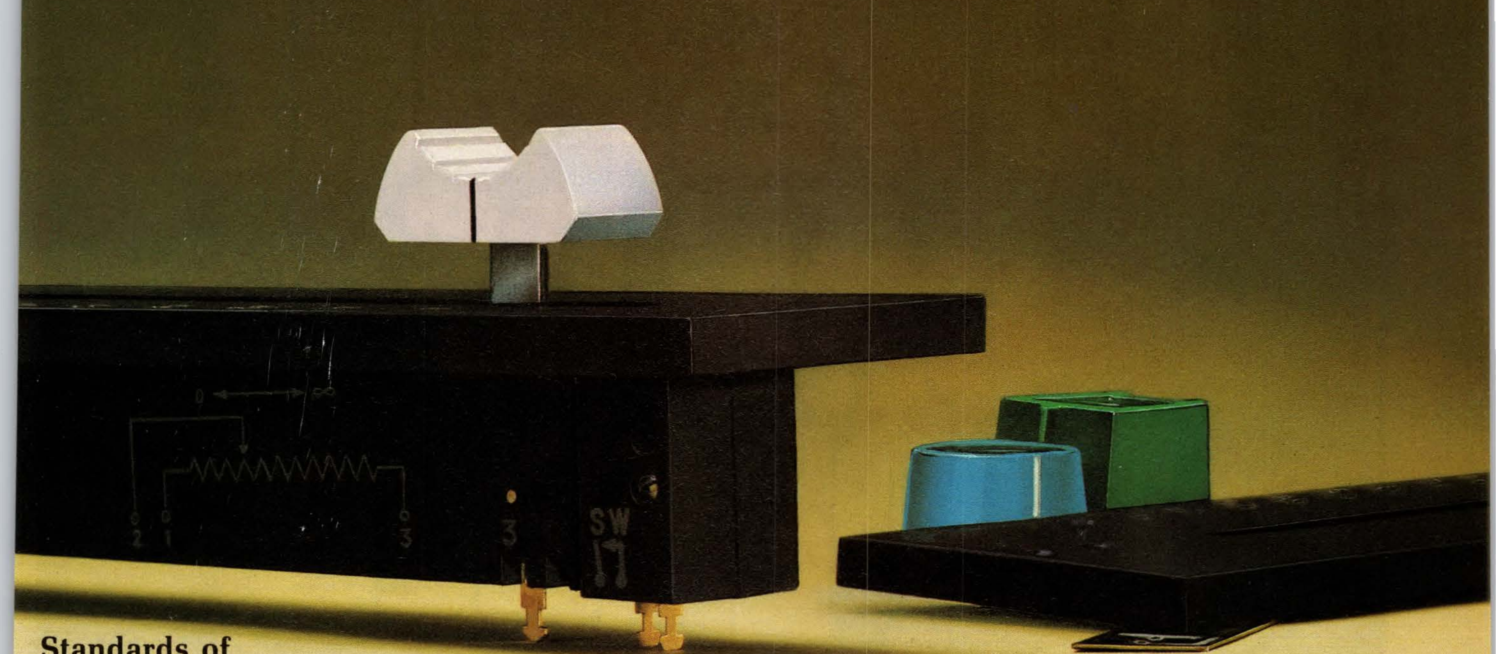

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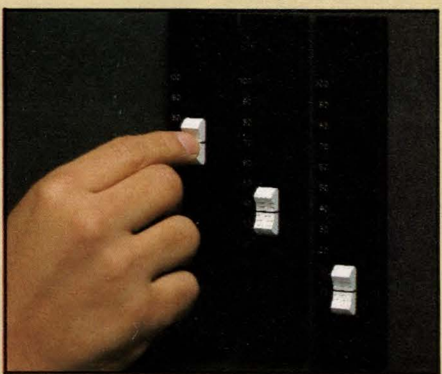

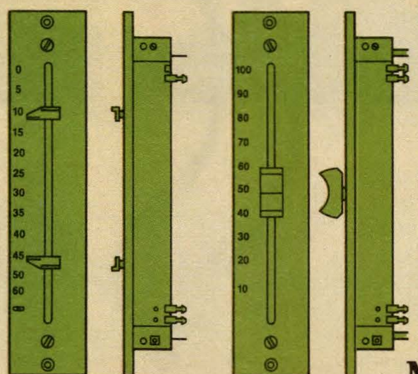

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CIRCLE NO 75

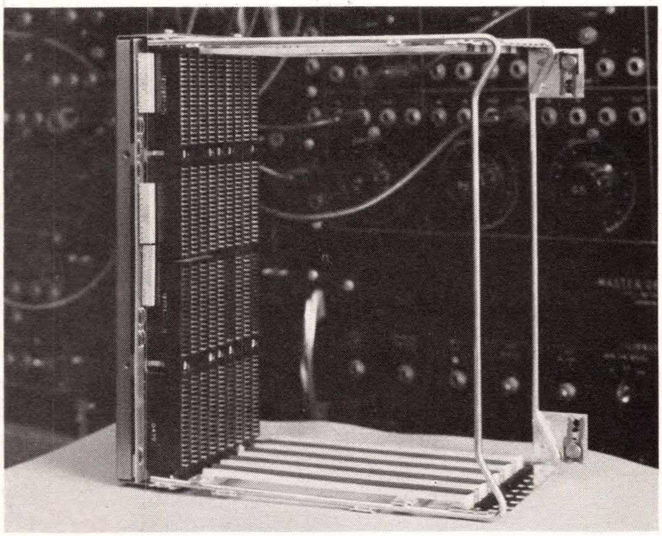
High-performance buses clear a path for future μCs

Forward-looking system designers can take advantage of the versatile high-performance-bus features described here to ease the transition from 8- to 16- to 32-bit μCs.

Carl Warren, Western Editor

Continuing the listing of μC-bus specs begun in Part 2, this third and final installment covers high-performance designs.

The four buses included here range from the well-proven Multibus to the proposed P896 futurebus. Because both these buses and the Versabus and Z-Bus permit word sizes from eight to 32 bits, they provide the means to handle current and future μCs. They thus deserve special attention from designers who wish to implement systems today that will also solve tomorrow's problems.



Symbolizing the evolution from analog systems to digital-bus-based solutions, *this Digital Equipment Corp H-9275A backplane appears in front of an analog computer.*

MULTIBUS (IEEE-796)

SOURCE

Intel Corp
5200 NE Elam Young Parkway
Hillsboro, OR 97123
Phone (503) 640-7112

GENERAL INFORMATION

The Intel Multibus (IEEE-796) supports two independent address spaces, memory and I/O. During memory cycles, it can directly address up to 16M bytes using 24-bit addressing. During I/O bus cycles, it can address up to 64k via I/O ports using 16-bit addressing. Both memory and I/O cycles can support 8- or 16-bit data transfers.

The Multibus structure employs the master-slave concept (see the nearby **figure**), where the master device in the system takes control of the bus; the slave device, upon decoding its own address, acts upon the command provided by the master. This handshake between master and slave devices allows modules running at different speeds to interface via the bus and bus data rates of up to five million transfers per sec (bytes or words).

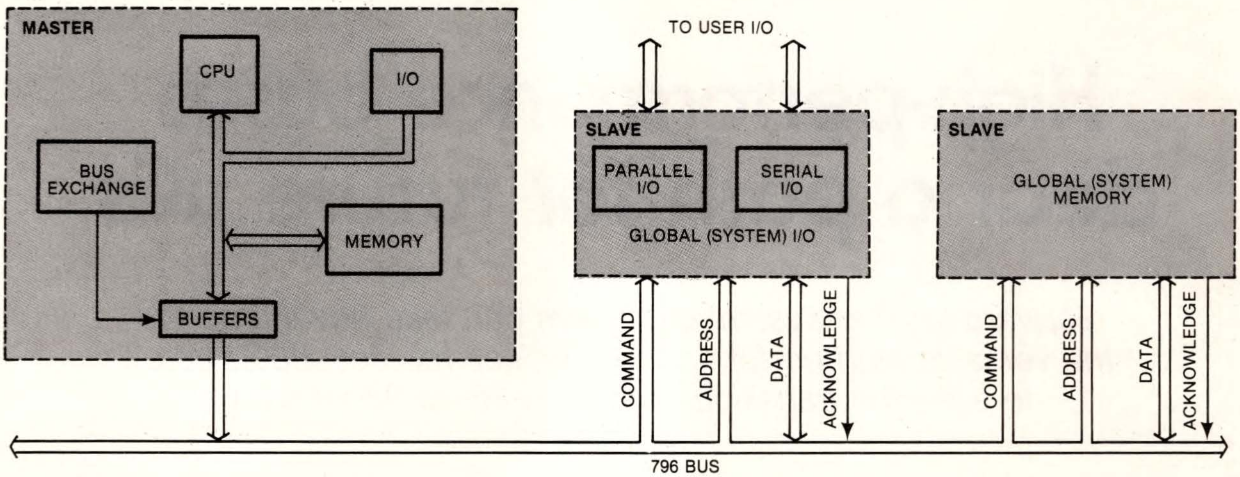
Additionally, the Multibus can support μPs ranging in word size from eight to 32 bits, and multiple processors can operate on a single backplane.

BUS SIGNALS

In general, bus signals are grouped as control lines, address and inhibit lines, data lines, interrupt lines and bus-exchange lines. The following definitions apply:

CLASS	FUNCTION	SIGNAL	DEFINITION
Clocks	Constant clock	CCLK	Periodic signal of constant frequency—used as master
	Bus clock	BCLK	Periodic signal used to synchronize bus-contention logic
COMMANDS	Memory write	MWTC	Communication element between masters and slaves—indicates valid bus data
	Memory read	MRDC	Indicates master has received data from slave
	I/O write	IOWC	Performs same as MWTC
	I/O read	IORC	Performs same as MRDC
Acknowledge	Transfer ack	XACK	Used by slaves to acknowledge commands from master

MULTIBUS MASTER AND SLAVE EXAMPLE



BUS SIGNALS (Cont)

CLASS	FUNCTION	SIGNAL	DEFINITION
Initialize		INIT	Used to reset entire system to a known internal state
Lock		LOCK	Generated by bus master to extend mutual exclusion to multiple-port RAM designs
ADDRESS	Address lines	ADR0-ADR17	Specifies address or referenced memory or I/O location (max 16M bytes and up to 64k devices)
	Byte high enable	BHEN	Byte-control line used to enable the upper byte (bits 8 through F) of a 16-bit word
INHIBIT	Inhibit lines	INH1&INH2	Can be invoked for any memory-read operation; used by a slave to inhibit another slave's bus access
DATA	Data lines	DAT0-DATF	16 bidirectional data lines transmit and receive data (DATF is MSB)
INTERRUPT	Interrupt rqst	INT0-INT7	Used to request an interrupt by activating one of eight lines (INT_0 is highest priority, INT_7 is lowest)
	Interrupt ack	INTA	Used to freeze the interrupt status and request placement of interrupt vector on bus
BUS EXCHANGE	Bus clock	BCLK	See above
	Bus request	BREQ	Used by bus masters in a priority-resolution circuit to indicate request for bus control
	Bus priority	BPRN, BPRO	Permits masters to break deadlocks; BPRN shows that no higher priority master wants the bus, and BPRO serves in daisy-chained schemes
	Bus busy	BUSY	Indicates that bus is busy and prevents other masters from controlling bus
	Common bus rqst	CBRQ	Maximizes a master's data-transfer rate to the bus by sensing the absence of other bus requests, and notifies the bus master that it must relinquish bus control

TIMING SPECIFICATIONS

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS	REFERENCE
t_{AH}	ADDRESS HOLD TIME	50		nSEC	3.2.1, 3.2.2, 3.2.4
t_{AIZ}	ADDRESS TO INHIBIT HIGH DELAY	0	100	nSEC	3.2.3
t_{AS}	ADDRESS SETUP TIME (AT SLAVE BOARD)	50		nSEC	3.2.1, 3.2.2, 3.2.4
t_{BCY}	BCLK* PERIOD	100	∞	nSEC	3.2.5
t_{BPRNO}	BPRN* TO BPRO*	0	30	nSEC	3.2.5

TIMING SPECIFICATIONS (Cont)

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS	REFERENCE
t_{BPRNS}	BPRN* TO ↓BCLK* SETUP TIME	22		nSEC	3.2.5
t_{BPRO}	↓BCLK* TO BPRO*	0	40	nSEC	3.2.5
t_{BREQH}	↓BLCK* TO BREQ* HIGH DELAY	0	35	nSEC	3.2.5
t_{BREQL}	↓BCLK* TO BREQ* LOW DELAY	0	35	nSEC	3.2.5
t_{BSYO}	CBRQ*•BUSY* TO ↑BUSY	—	12	μSEC	3.2.5
t_{BUSY}	BUSY* DELAY FROM ↓BCLK*	0	70	nSEC	3.2.5
t_{BUSYS}	BUSY* TO ↓BCLK SETUP TIME	25		nSEC	3.2.5
t_{BW}	BCLK* WIDTH	$0.35t_{BCY}$	$0.65t_{BCY}$		3.2.5
t_{CBRO}	↓BCLK* TO CBRQ*	0	60	nSEC	3.2.5
t_{CBRQS}	CBRQ* TO ↓BCLK* SETUP TIME	35		nSEC	3.2.5
t_{CCY}	CCLK* PERIOD	100	110	nSEC	3.2.6
t_{CMD}	COMMAND PULSE WIDTH	100	t_{TOUT}	nSEC	3.2.1, 3.2.2
t_{CMPH}	COMMAND HOLD TIME	20		nSEC	3.2.1, 3.2.2
t_{CPM}	CENTRAL PRIORITY MODULE RESOLUTION DELAY (PARALLEL PRIORITY)	0	t_{BCY}-t_{BREQ} -2t_{PD} -t_{BPRNS} -t_{SKEW}		3.2.5
t_{CSEP}	COMMAND SEPARATION	100		nSEC	3.2.4, 3.2.6
t_{CW}	CCLK* WIDTH	$0.35t_{CCY}$	$0.65t_{CCY}$	nSEC	3.2.6
t_{DHR}	READ DATA HOLD TIME	0	65	nSEC	3.2.1, 3.2.4
t_{DHW}	WRITE DATA HOLD TIME	50		nSEC	3.2.2
t_{DS}	WRITE DATA SETUP TIME	50		nSEC	3.2.2
t_{DXL}	READ DATA SETUP TIME TO XACK*	0		nSEC	3.2.1, 3.2.4
t_{IAD}	XACK* DISABLE FROM INHIBIT (INTERNAL PARAMETER ON AN INHIBITED SLAVE; USED TO DETERMINE t_{XACKA}min)	0	100 (ARBITRARY)	nSEC	2.3.2
t_{ID}	INHIBIT DELAY	0	100 (RECOMMEND <100 nSEC)	nSEC	3.2.3

TIMING SPECIFICATIONS (Cont)

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS	REFERENCE
t_{INIT}	INIT* WIDTH	5		mSEC	3.2.6, 3.2.7
t_{INTA}	INTA* WIDTH	250		nSEC	3.2.4
t_{LCKH}	LOCK* HOLD TIME FROM COMMAND ACTIVE	100		nSEC	3.2.6
t_{LCKS}	LOCK* TO COMMAND SETUP TIME	100		nSEC	3.2.6
t_{LOCK}	LOCK* WIDTH		12	μSEC	3.2.6
t_{OUT}	TIMEOUT DELAY	1	DC(∞)	mSEC	—
t_{PD}	STANDARD BUS PROPAGATION DELAY		3	nSEC	3.1.2, 3.2.5
t_{SKEW}	BCLK* SKEW		t_{PD}		3.2.5
t_{XACK}	XACK* TIME (FOR SLAVES WITHOUT INHIBIT FUNCTION)	0	8	μSEC	3.2.1, 3.2.2, 3.2.4
t_{XACKA}	XACK* TIME OF AN INHIBITED SLAVE	t_{IAD} + 50 nSEC	1500	nSEC	3.2.3
t_{XACKB}	XACK* TIME OF AN INHIBITING SLAVE	1500	8000	nSEC	3.2.3
t_{XAH}	XACK* HOLD TIME	0	65	nSEC	3.2.1, 3.2.2, 3.2.4

ELECTRICAL SPECIFICATIONS

POWER-SUPPLY SPECIFICATIONS

	STANDARD[1]			
PARAMETER	GROUND	+5	+12	−12
MNEMONIC	GND	+5V	+12V	−12V
BUS PINS	P1-1,2,11,12, 75,76,85,86	P1-3,4,5,6 81,82,83,84	P1-7,8	P1-79,80
TOLERANCE (%)	REF	±1	±1	±1
COMBINED LINE & LOAD REG (%)	REF	0.1	0.1	0.1
RIPPLE (P-P) (mV)	REF	50	50	50
TRANSIENT RESPONSE (50% LOAD CHANGE) (μSEC)		100	100	100

[1]POINT OF MEASUREMENT IS CONNECTION POINT BETWEEN MOTHERBOARD AND POWER SUPPLY. AT ANY CARD EDGE CONNECTOR A DEGRADATION OF 2% MAXIMUM (EG VOLTAGE TOLERANCE ±2%) IS ALLOWED.

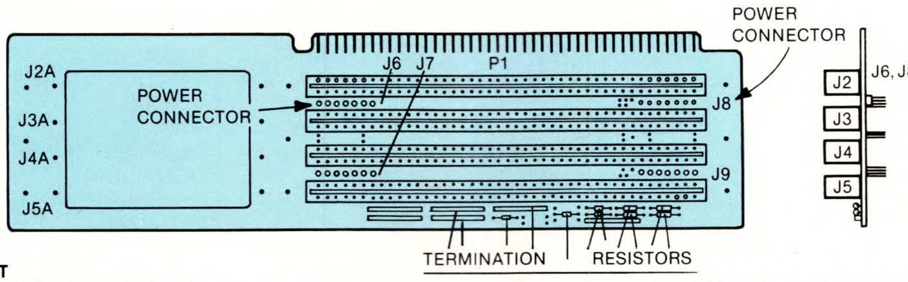
IN-USE SIGNAL-LINE REQUIREMENTS

During normal use, signal rise and fall times depend on the type of driver used. Typical rise and fall times are:

	OPEN COLLECTOR	TOTEM POLE	3-STATE
RISE TIME	—	10 nSEC	10 nSEC
FALL TIME	10 nSEC	10 nSEC	10 nSEC

MECHANICAL SPECIFICATIONS

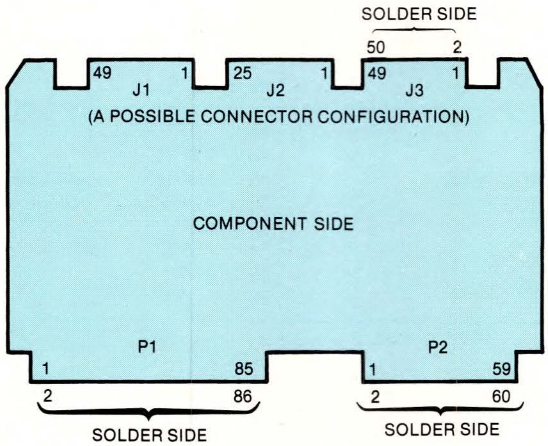
TYPICAL BACKPLANE

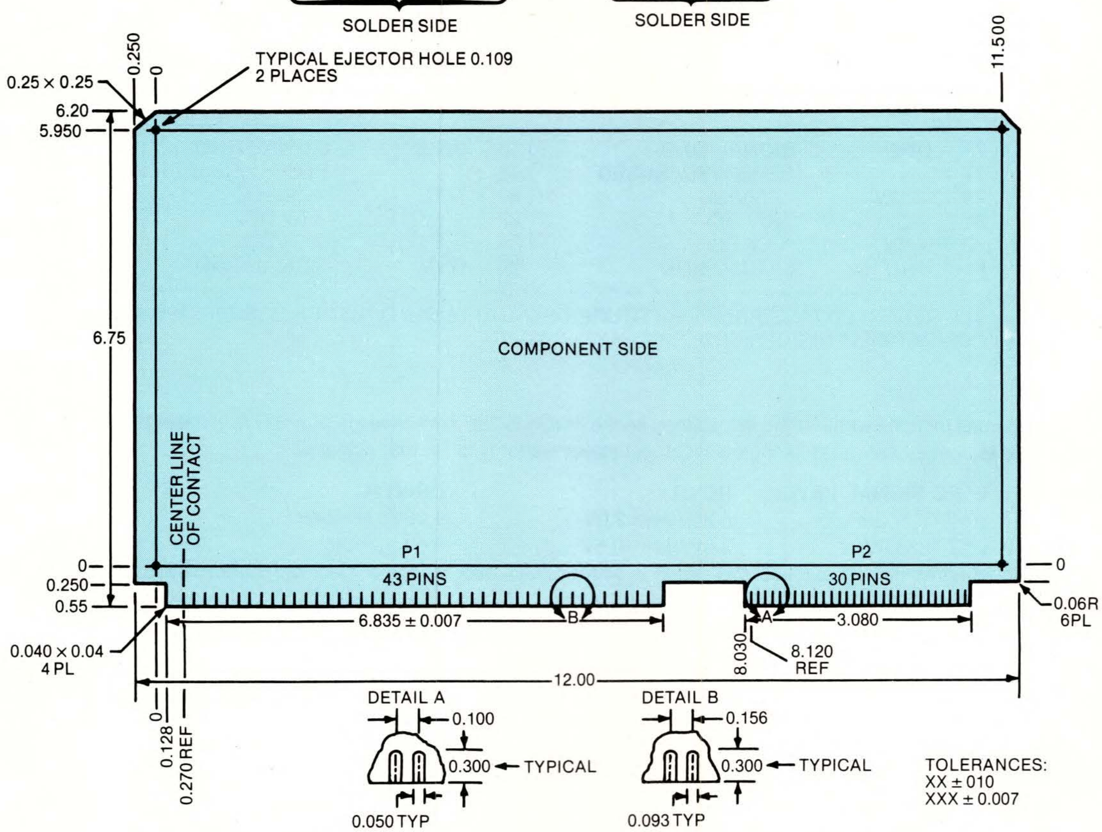


PARTS LIST

1 PWB TERMINATION BACKPLANE
2 7-POST WAFER CONNECTORS (0.156-IN. PIN CENTERS) (J6 AND J8)
4 EDGE BOARD CONNECTORS, 43/86 PINS ON 0.156-IN. CENTERS (J2-J5)
12 WIRE WRAPPING POSTS
4 10-PIN 2.2k 9-RES, 1.5W RESISTOR PACKS (RP1-RP4)
1 10-PIN, 1k, 9-RES, 1.5W RESISTOR PACK (RPS)
1 10-PIN, 1.1k, 9-RES, 1.5W RESISTOR PACK (RP6)
1 1k RESISTOR, ⅛W, ± 5% (R1)
1 2.2k RESISTOR, ⅛W, ± % (R5)
2 220Ω RESISTORS, ¼W, ± 5% (R9, R11)
2 330Ω RESISTORS, ¼W, ± 5% (R10, R12)
2 510Ω RESISTORS, ⅛W, ± 5% (R7, R8)

PIN NUMBERING AND PC-BOARD OUTLINE





PIN ASSIGNMENTS

	PIN	COMPONENT SIDE		PIN	CIRCUIT SIDE	
		MNEMONIC	DESCRIPTION		MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	SIGNAL GND	2	GND	SIGNAL GND
	3	+5V	+5V DC	4	+5V	+5V DC
	5	+5V	+5V DC	6	+5V	+5V DC
	7	+12V	+12V DC	8	+12V	+12V DC
	9		RESERVED, BUSED	10		RESERVED, BUSED
	11	GND	SIGNAL GND	12	GND	SIGNAL GND
BUS CONTROLS	13	BCLK*	BUS CLOCK	14	INIT*	INITIALIZE
	15	BPRN*	BUS PRI IN	16	BPRO*	BUS PRI OUT
	17	BUSY*	BUS BUSY	18	BREQ*	BUS REQUEST
	19	MRDC*	MEM READ CMD	20	MWTC*	MEM WRITE CMD
	21	IORC*	I/O READ CMD	22	IOWC*	I/O WRITE CMD
	23	XACK*	XFER ACKNOWLEDGE	24	INH1*	INHIBIT 1 (DISABLE RAM)
BUS CONTROLS AND ADDRESS	25	LOCK*	LOCK	26	INH2*	INHIBIT 2 (DISABLE PROM OR ROM)
	27	BHEN*	BYTE HIGH ENABLE	28	AD10*	
	29	CBRQ*	COMMON BUS REQUEST	30	AD11*	ADDRESS
	31	CCLK*	CONSTANT CLK	32	AD12*	BUS
	33	INTA*	INTR ACKNOWLEDGE	34	AD13*	
INTERRUPTS	35	INT6*	PARALLEL	36	INT7*	PARALLEL
	37	INT4*	INTERRUPT	38	INT5*	INTERRUPT
	39	INT2*	REQUESTS	40	INT3*	REQUESTS
	41	INT0*		42	INT1*	
ADDRESS	43	ADRE*		44	ADRF*	
	45	ADRC*		46	ADRD*	
	47	ADRA*	ADDRESS	48	ADRB*	ADDRESS
	49	ADR8*	BUS	50	ADR9*	BUS
	51	ADR6*		52	ADR7*	
	53	ADR4*		54	ADR5*	
	55	ADR2*		56	ADR3*	
	57	ADR0*		58	ADR1*	
DATA	59	DATE*		60	DATF*	
	61	DATC*		62	DATD*	
	63	DATA*	DATA	64	DATB*	DATA
	65	DAT8*	BUS	66	DAT9*	BUS
	67	DAT6*		68	DAT7*	
	69	DAT4*		70	DAT5*	
	71	DAT2*		72	DAT3*	
	73	DAT0*		74	DAT1*	
POWER SUPPLIES	75	GND	SIGNAL GND	76	GND	SIGNAL GND
	77		RESERVED, BUSED	78		RESERVED, BUSED
	79	−12V	−12V DC	80	−12V	−12V DC
	81	+5V	+5V DC	82	+5V	+5V DC
	83	+5V	+5V DC	84	+5V	+5V DC
	85	GND	SIGNAL GND	86	GND	SIGNAL GND

ALL RESERVED PINS ARE FOR FUTURE USE AND SHOULD NOT BE USED IF UPWARD COMPATIBILITY IS DESIRED.

Note: The signal names indicate whether the signal lines on the Multibus/796 are active HIGH or LOW. If the signal name ends with an asterisk, the signal is active LOW, and its logical electrical-state relationship for that signal is:

LOGIC STATE	ELEC SIGNAL LEVEL	RCVR	DRIVER
ZERO	H=TTL HIGH	5.25V≥H≥2.0V	5.25V≥H≥2.4V
ONE	L=TTL LOW	0.8V≥L≥−0.5V	0.5V≥L≥0V

However, if the signal name has no asterisk, the signal is active HIGH, and its logical electrical-state relationship is:

LOGIC STATE	ELEC SIGNAL LEVEL	RCVR	DRIVER
ZERO	L=TTL LOW	0.8V≥L≥−0.5V	0.5V≥L≥0V
ONE	H=TTL HIGH	5.25V≥H≥2.0V	5.25≥H≥2.4V

FUTUREBUS P896 (PROPOSED)

SOURCE

Andrew Allison, Chairman
P896 Working Group
27360 Natoma Rd
Los Altos Hills, CA 94022
Phone (415) 941-6065
or
Prof J D Nicoud, Vice Chairman
LAMI-EPFL
Bellerive 16
CH-1007 Lausanne, Switzerland

GENERAL INFORMATION

The P896 bus, intended to be a manufacturer- and processor-independent bus, offers 32-bit multiplexed address and data paths while supporting 8- and 16-bit data paths.

The bus will also support full-handshake bus transfers and distributed bus arbitration for at least 32 bus masters. Multitask and resource management and interrupts are aided by both parallel and serial mechanisms.

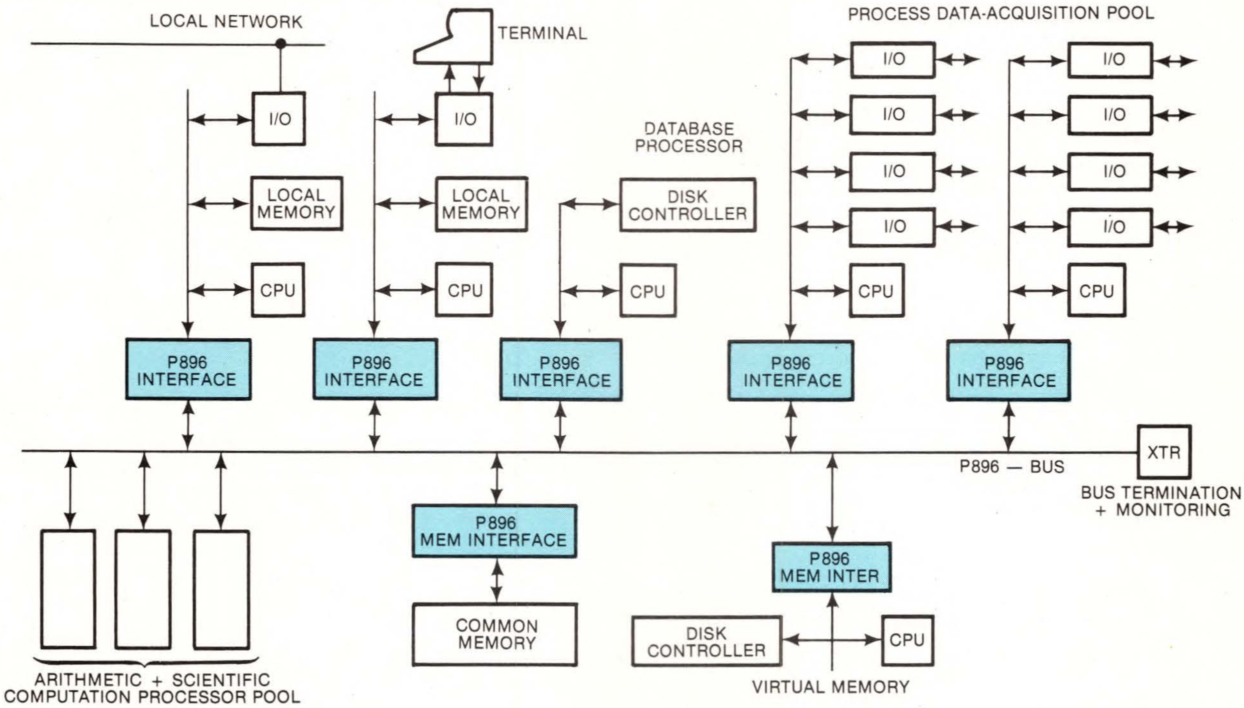
The working committee is specifying International Electrotechnical Commission standards for modules, backplanes and racks to minimize signal count and thus reduce overall system costs.

The P896 backplane encompasses a family of upwardly compatible technology- and processor-independent bus structures. This backplane includes two configurations supporting Level 1 32-bit multiplexed address and data operations on a 64-pin connector.

Implementation with 8-bit-data/16-bit-address or 16-bit-data/24-bit-address paths are possible but might not be fully compatible with 32-bit versions. Level 2 provides additional control capability and error detection on a 96-pin fully compatible extension. This level still requires additional refinement.

The P896 backplane is designed to let several processors share a common memory (see the nearby **figure**). Additionally, the P896 works with networking designs, both internally and externally.

FUTUREBUS SYSTEM-CONFIGURATION EXAMPLE



BUS SIGNALS

For the P896, four sets of lines make up the backplane: The power bus provides multiple-ground signal return and 5V lines; the parallel data bus consists of 32 multiplexed address and data lines plus mode/status lines and timing lines; the parallel arbitration bus consists of priority lines plus control lines (bus arbitration occurs in parallel with data transfers and allows a single master to take control of the parallel data bus); and the serial bus consists of one serial line and a clock that allows completely separate information transfers in addition to those on the parallel bus.

CLASS	FUNCTION	SIGNAL	DEFINITION
Clocks	System clock	CK	Periodic signal of constant frequency—used as master
COMMANDS	Transfer data	C0-C6	Used to encode control information to indicate the function of the transfer and its nature
	Bus priority	BP0-BP5	Used to give bus control to another master or slave
	Supervisor	SC	Used to inhibit transfers or disable buffers; permits using a memory manager
	Error control	EC0-EC7	Used for error detection and control
ADDRESS	Address lines	AD0-AD31	Specify the address or referenced memory or I/O location
DATA	Data lines	AD0-AD31	Multiplexed with address

Note: The information presented here is general in nature and subject to revision.

ELECTRICAL SPECIFICATIONS

POWER-SUPPLY UNIT LOADS

ALL P896-COMPATIBLE MODULES WILL SPECIFY, IN ADDITION TO THE DC LOAD ON THE SIGNAL LINES, A POWER SUPPLY LOAD IN TERMS OF THE POWER UNIT LOAD, WHICH IS DEFINED TO EQUAL 1A ON THE +5V LINE.

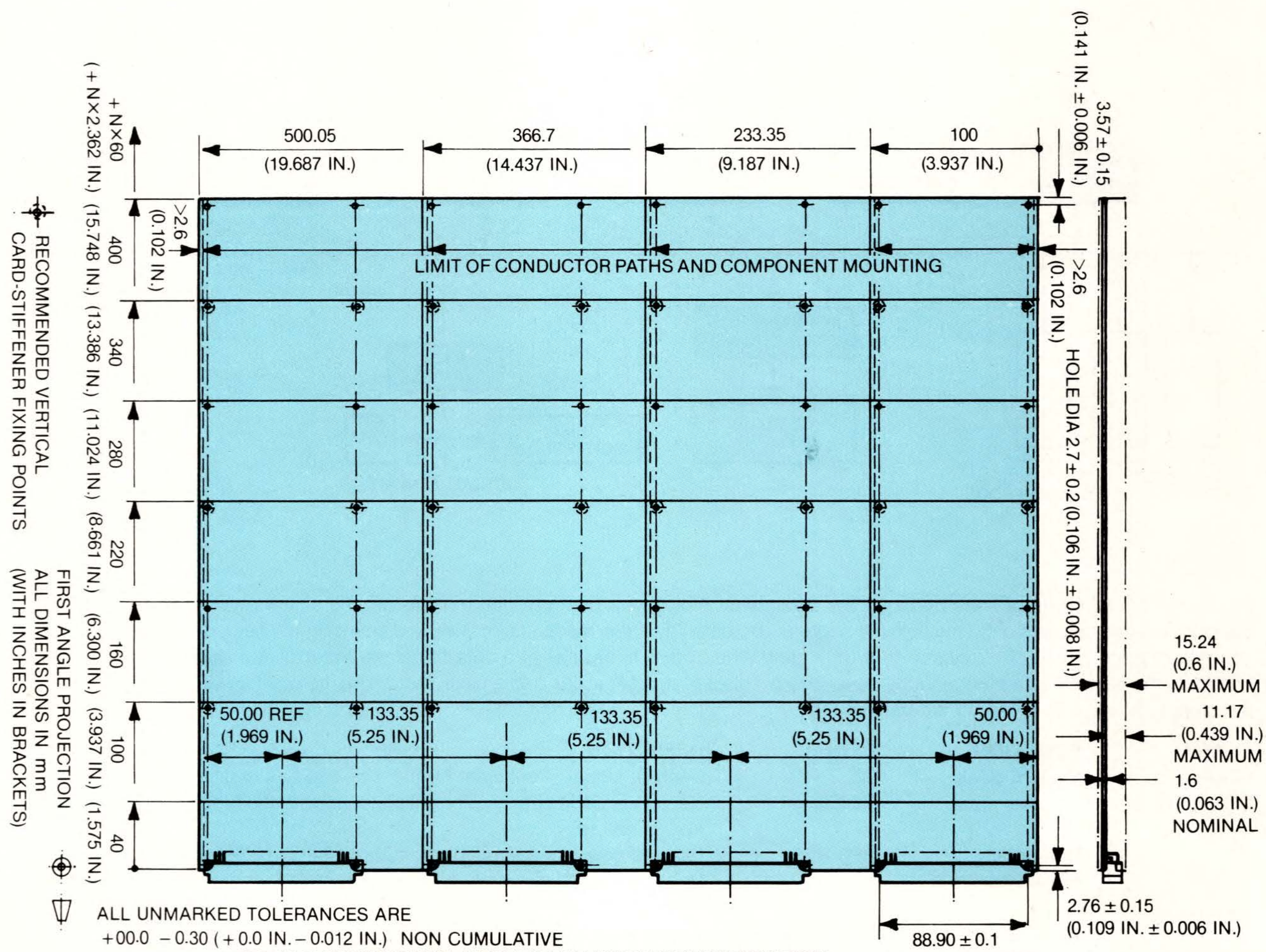
CHARACTERISTIC RESISTANCE TERMINATION	MINIMUM	TYPICAL	MAXIMUM
RT(Ω)	100	110	125
MAXIMUM ALLOWABLE LOAD (HIGH) TO KEEP SIGNAL LINE ABOVE 28V DC WHEN UNDRIVEN (mA)	8	7.3	6.4
DRIVER CURRENT TAKEN BY TERMINATIONS (LOW) (mA)	48	43.6	38.4
DRIVER CURRENT LEFT FOR UNIT LOADS (LOW) (mA)	52	56.4	61.6
MAXIMUM NUMBER OF LEVEL 1 UNIT LOADS (HIGH)	40	36	32*
MAXIMUM NUMBER OF LEVEL 2 UNIT LOADS (HIGH)	200	182	160
NUMBER OF LEVEL 1 UNIT LOADS (LOW)	32*	35	38
MAXIMUM NUMBER OF LEVEL 2 UNIT LOADS (LOW)	130	141	154

NOTE

* INDICATES P896 LIMITS FOR THE PURPOSE OF CALCULATING RESISTANCE AND TERMINATION REGULATOR VOLTAGE.

MECHANICAL SPECIFICATIONS

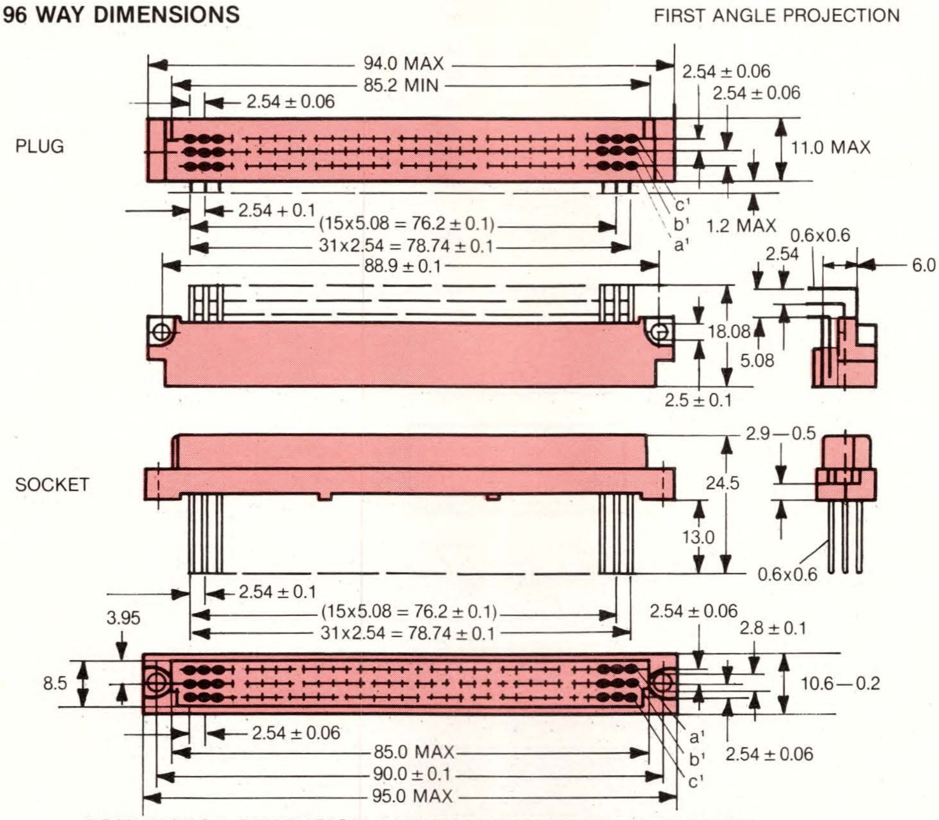
PC-BOARD OUTLINE AND CONNECTOR SIZES



MODULE DIMENSION AND TOLERANCE SPECIFICATION

PC-BOARD OUTLINE AND CONNECTOR SIZES (Cont)

96 WAY DIMENSIONS



CONNECTOR DIMENSION AND TOLERANCE SPECIFICATION

PINOUTS FOR A DIN 41612 CONNECTOR (PRELIMINARY—SUBJECT TO REVISION)

	A	B	C	
1	GND	GND	GND	GND = power return
2	+5	+5	+5	
3	CK		IL*	
4	gnd		gnd	gnd = signal return
5	BPO*	gnd	BP1*	
6	BP2*	BP6*	BP3*	
7	BP4*	BP7*	BB*	
8	AS*		SI*	
9	DS*	gnd	SC*	
10	C4*		AK*	
11	C2*		C3*	
12	C0*		C1*	
13	gnd	gnd	gnd	
14	AD0*	C5*	AD1*	
15	AD2*	C6*	AD3*	
16	AD4*		AD5*	

	A	B	C
17	AD6*		AD7*
18	AD8*	gnd	AD9*
19	AD10*		AD11*
20	AD12*		AD13*
21	AD14*		AD15*
22	gnd	gnd	gnd
23	AD16*	EC6*	AD17*
24	AD18*	EC5*	AD19*
25	AD20*	EC4*	AD21*
26	AD22*	EC3*	AD23*
27	AD24*	gnd	AD25*
28	AD26*	EC2*	AD27*
29	AD28*	EC1*	AD29*
30	AD30*	EC0*	AD31*
31	+5	+5	+5
32	GND	GND	GND

NOTE
*ACTIVE LOW

VERSABUS

SOURCE

Motorola Microsystems
3102 N 56th St
Phoenix, AZ 85018
Phone (602) 244-5557

GENERAL INFORMATION

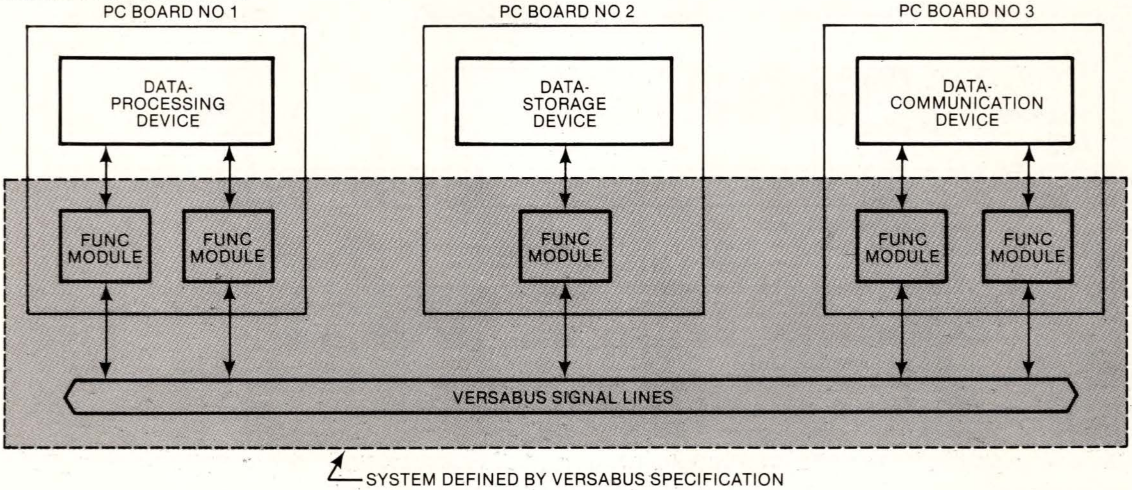
Motorola refers to the Versabus as a system-level computer bus. It's geared to support large-word-size μPs (16, 32 bits) as well as 8-bit devices.

To meet the growing demand for higher capability system designs that incorporate wide-word μPs, the Versabus implements the following objectives: providing a means of communication between two devices on the bus without disturbing other devices and allowing broad design latitude so system designers can optimize cost without affecting system compatibility.

In addition, Versabus permits 5-MHz data-transfer rates. Moreover, multiple processors can operate on one backplane, employing the local/system-bus concept.

Currently, the bus is single sourced through Motorola. However, because of its ability to support several vendors' component devices, designers should find developing Versabus-compatible products easy.

VERSABUS SYSTEM ELEMENTS



BUS SIGNALS

As with other bus architectures, Versabus signals are defined according to the functions they perform. However, because the Versabus is designed to meet varying needs, signal-size options are important. Both data and address buses have size options that permit logical addressing of 2^{24} or 2^{32} bytes and a 16- or 32-bit data bus. For the Versabus, the following bus definitions apply:

CLASS	FUNCTION	SIGNAL	DEFINITION
Clocks	System clock	SYSCLK	A constant 16-MHz clock signal that's independent of the μP speed; used for general system timing
	AC clock	ACCLK	A totem-pole input clock signal that indicates power-line frequency and zero-voltage transition points
COMMANDS	Write	WRITE	3-state output signal that defines the cycle type as read or write (HIGH=read, LOW=write)
	Acknowledge in	ACKIN	Forms daisy-chained ACK; tells board that an ACK cycle is in progress
	Acknowledge out	ACKOUT	In daisy-chain, tells next board an ACK cycle is in progress
	AC failure	ACFAIL	Indicates power levels are not being met
	System fail	SYSFAIL	Indicates a board has failed the test program
	System reset	SYSRESET	Causes entire system to reset
	Secondary reset	SECRESET	A LOW on this line causes user (slave) reset—selective
BUS EXCHANGE	Bus busy	BBSY	Signal generated by current master to indicate it has bus
	Bus error	BERR	Active-LOW signal generated by peripheral device indicating an unrecoverable error
	Bus clear	BCLR	Removes current master from bus if higher priority master is requesting
	Bus grant IN	BG0IN BG4IN	Indicates to a board it might be next master—daisy chained
	Bus grant OUT	BG0OUT BG4OUT	In a daisy-chained grant, tells next board it might be next master
	Bus request	BRO-BR4	Indicates that a master requires the bus
	Bus release	BREL	Emergency signal to tell current master to release the bus in 16 data-transfer cycles
	Long word	LWORD	3-state signal specifying that cycle is byte/word when HIGH or word/long word when LOW

BUS SIGNALS (Cont)

CLASS	FUNCTION	SIGNAL	DEFINITION
INTERRUPT	Interrupt request	IRQ1-IRQ7	Active LOW generates a prioritized interrupt
	Secondary interrupt	SECIEN	Enable interrupts from a secondary map
ADDRESS	(J1 pins 36-58)	A01-A23	Specifies a memory address
	(J2 pins 89-96)	A24-A31	Specifies extended address
	Address modifier	AMO-AM7	Provides data about address bus, size, cycle type, slave/master ID
	Address parity 0	APARITY0	Odd parity bit for address bits A_{01-23} and LWORD
	Address parity 1	APARITY1	Odd parity bit for address bits A_{24-31}; used for 32-bit expansion
	Address strobe	AS	Indicates valid address
DATA	Data lines	D00-D15	Bidirectional lines between master and slave
		D16-D31	Bidirectional lines between master and slave for extended data bus
	Data parity 0	DPARITY0	Odd parity bit for data bits D_{00-07}
	Data parity 1	DPARITY1	Odd parity bit for data bits D_{08-15}
	Data parity 2	DPARITY2	Odd parity bit for data bits D_{16-23}
	Data parity 3	DPARITY3	Odd parity bit for data bits D_{24-31}
	Data strobe 0	DS0	Indicates a data transfer will occur on byte 0 of data bus (D_{00-07}, D_{16-23})
	Data strobe 1	DS1	Indicates a data transfer will occur on byte 1 of data bus (D_{08-15}, D_{23-31})
	Data transfer ack	DTACK	Indicates that valid data is on the bus during a read cycle or data has been accepted during a write cycle

TYPICAL BUS-MASTER READ CYCLE

NUMBER	PARAMETER	MIN	MAX
1	Address Setup	30	
2	DTACK* LOW to invalidate address	0	
3	AS* HIGH	40	
4	DTACK* LOW to AS* HIGH	0	
5	AS* to DS"A"* skew	0	
6	WRITE* setup	30	
7	DTACK* LOW to invalidate WRITE*	0	
8	DATA 3-state to DS"A" LOW	0	
9	DS"A"* to DS"B" skew	0	20
10	DTACK* LOW to DS"A"* HIGH	0	
11	DS"A"* HIGH	40	
12	DS"B"* HIGH to DS"A" LOW	0	
13	DTACK* HIGH to DS"A" LOW	0	
14	DTACK* LOW to DS"B" HIGH	0	
15	DS"A"* HIGH to DS"B" LOW	40	
16	DS"B"* HIGH	40	
17	Data setup	20	
18	Data 3-stated to DTACK* HIGH	0	
19	DS"A"* HIGH to invalidate data	0	

TYPICAL BUS-MASTER WRITE CYCLE

NUMBER	PARAMETER	MIN	MAX
1	Address Setup	30	
2	DTACK* LOW to invalidate address	0	
3	AS* HIGH	40	
4	DTACK* LOW to AS* HIGH	0	
5	AS* to DS"A"* skew	0	
6	WRITE* setup	30	
7	DTACK* LOW to invalidate WRITE*	0	
8	DTACK* HIGH to activate data bus	0	
9	data setup	30	
10	DTACK* LOW to invalidate data	0	
11	DS"A"* to DS"B"* skew	0	20
12	DTACK* LOW to DS"A"* HIGH	0	
13	DS"A"* HIGH	40	
14	DS"B"* HIGH to DS"A"* LOW	40	
15	DS"B"* HIGH	40	
16	DS"A"* HIGH to DS"B"* LOW	40	
17	DTACK* LOW to DS"B"* HIGH	0	
18	DS"B"* HIGH to DTACK* HIGH		

ELECTRICAL SPECIFICATIONS

POWER-SUPPLY SPECIFICATIONS

MNEMONIC	DESCRIPTION	VARIATION (%)	RIPPLE & NOISE (P-P) (mV)	CONNECTOR P_1 PIN NUMBER	CONNECTOR P_2 PIN NUMBER
+5V	+5V DC POWER	±2.5	25	1, 2, 129-132	7-10
+12V	+12V DC POWER	±3.0	25	125-128	11-12
−12V	−12V DC POWER	±3.0	25	121-122	15-16
+5V STDBY	+5V DC STANDBY	±2.5	25	133-134	—
+15V	ANALOG POWER	±3.0	10	—	69-70
−15V	ANALOG POWER	±3.0	10	—	67-68
GND	GROUND	REF	REF	3, 4, 23-24, 27-28, 31-32, 61-62, 67-68, 71-72, 119-120, 123-124, 139-140	1-2, 3-4, 5-6, 97-98, 101-102
15V GND	±15V GROUND RETURN	REF	REF	—	13-14

BUS-RECEIVER SPECIFICATION

PARAMETER	MIN	MAX	UNIT	TEST CONDITION
LOW INPUT VOLTAGE (V_{IL})		0.8	V	
HIGH INPUT VOLTAGE (V_{IH})	2.0		V	
LOW INPUT CURRENT (I_{IL})		−400	μA	INPUT VOLTAGE = 0.5V
HIGH INPUT CURRENT (I_{IH})		*50	μA	INPUT VOLTAGE = 2.7V

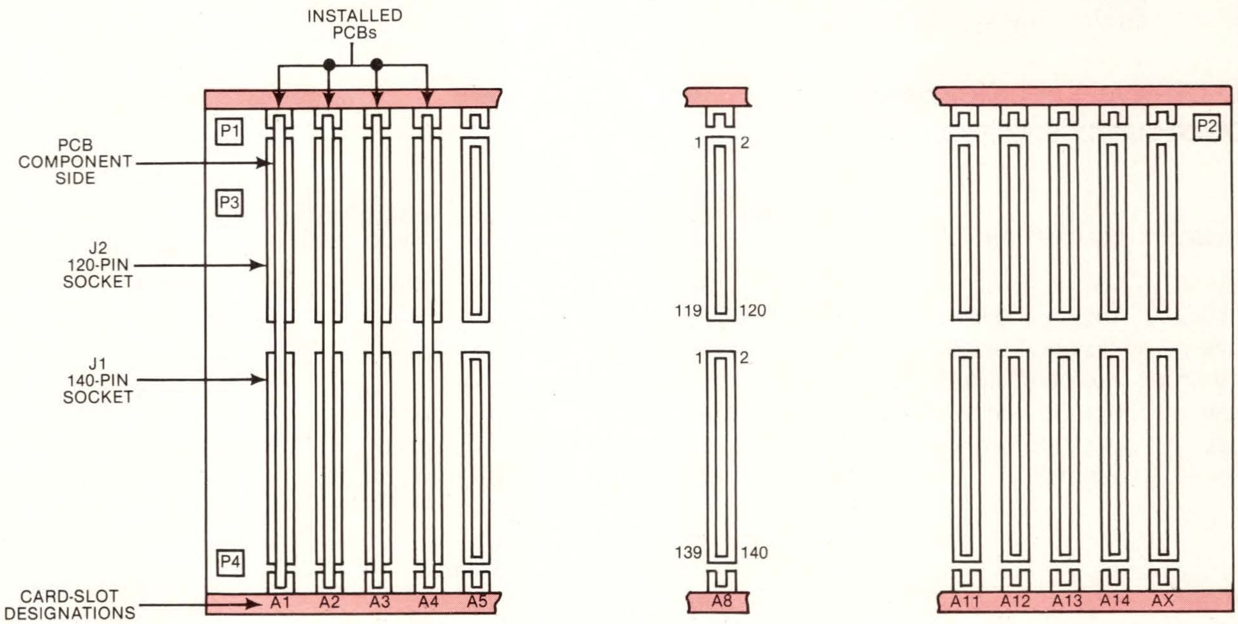
*HIGH INPUT CURRENT I_{IH} SHOULD BE LIMITED TO 20 μA FOR LOW-CURRENT TOTEM-POLE DRIVE LINES. THIS SPECIFICATION REPRESENTS A STANDARD LSTTL INPUT.

BUS-DRIVER SPECIFICATIONS

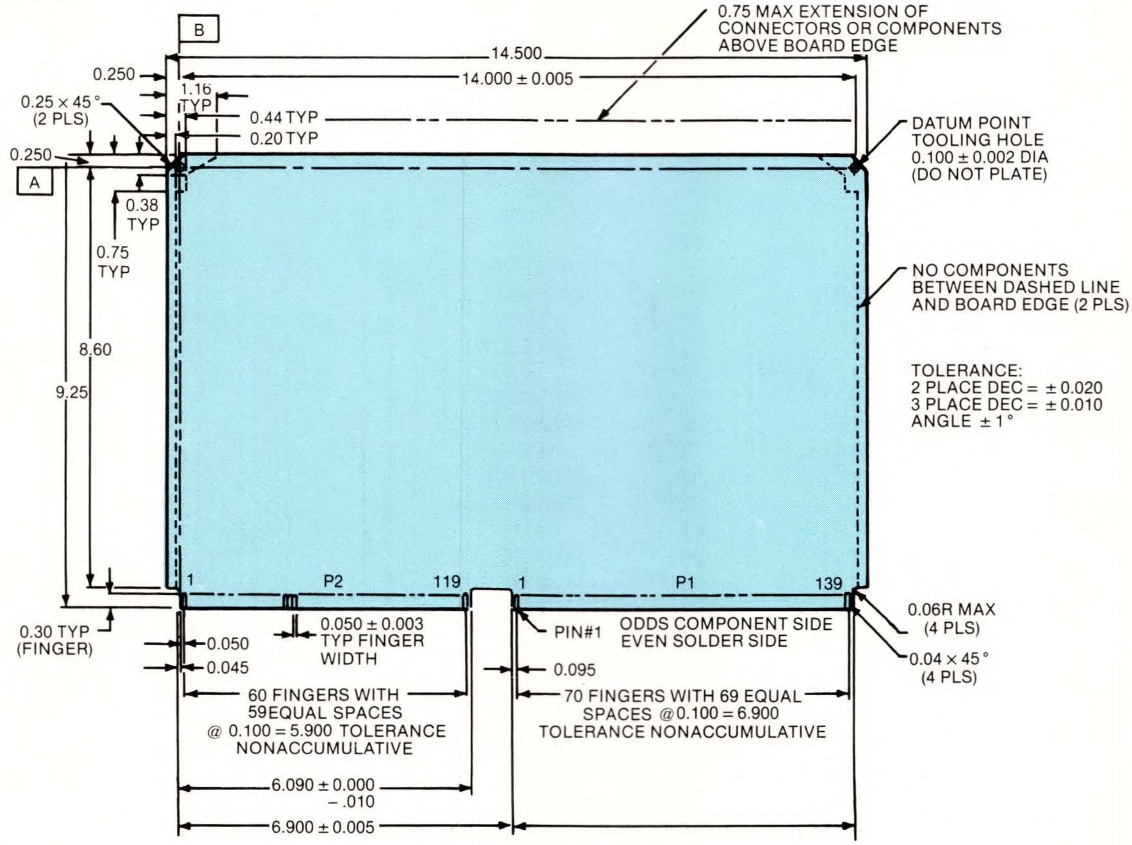
DRIVER TYPE	PARAMETERS	MIN	MAX	UNIT	TEST CONDITION
TOTEM-POLE	LOW (V_{OL})		0.55	V	SINK 64 mA FOR TERMINATED LINE
(HIGH CURRENT)	HIGH (V_{OH})	2.0 2.4		V V	SOURCE 15 mA TERMINATED SOURCE 3 mA LINE
TOTEM-POLE	LOW (V_{OL})		0.5	V	SINK 8 mA FOR UNTERMINATED LINE
(LOW CURRENT)	HIGH (V_{OH})	2.7		V	SOURCE 400 μA FOR UNTERMINATED LINE
3-STATE	LOW (V_{OL})		0.55	V	SINK 64 mA FOR TERMINATED LINE
	HIGH (V_{OH})	2.0 2.4		V V	SOURCE 15 mA TERMINATED SOURCE 3 mA LINE
	OFF OUTPUT CURRENT (I_{OZ})		±50	μA	2.4V or 0.5V APPLIED
OPEN COLLECTOR	LOW (V_{OL})		0.7	V	SINK 40 mA
	HIGH OUTPUT CURRENT (I_{OH})		50	μA	5.0V APPLIED

MECHANICAL SPECIFICATIONS

TYPICAL BACKPLANE



PIN NUMBERING AND PC-BOARD OUTLINE



COMPONENT SIDE

J1/P1 PIN ASSIGNMENTS

ODD PIN NUMBER (P1 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P1 SOLDER SIDE)	SIGNAL MNEMONIC
1	+5V	2	+5V
3	GND	4	GND
5	D00*	6	D01*
7	D02*	8	D03*
9	D04*	10	D05*
11	D06*	12	D07*
13	D08*	14	D09*
15	D10*	16	D11*
17	D12*	18	D13*
19	D14*	20	D15*
21	DPARITY0*	22	DPARITY1*
23	GND	24	GND
25	DS0*	26	DS1*
27	GND	28	GND
29	DTACK*	30	AS*
31	GND	32	GND
33	APARITY0*	34	WRITE*
35	LWORD*	36	A01*
37	A02*	38	A03*
39	A04*	40	A05*
41	A06*	42	A07*
43	A08*	44	A09*
45	A10*	46	A11*
47	A12*	48	A13*
49	A14*	50	A15*
51	A16*	52	A17*

J1/P1 PIN ASSIGNMENTS (Cont)

ODD PIN NUMBER (P_1 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P_1 SOLDER SIDE)	SIGNAL MNEMONIC
53	A18*	54	A19*
55	A20*	56	A21*
57	A22*	58	A23*
59	AM4*	60	AM7*
61	GND	62	GND
63	AM3*	64	(RESERVED)
65	(RESERVED)	66	(RESERVED)
67	GND	68	GND
69	ACCLK	70	SYSCLK
71	GND	72	GND
73	SECRESET*	74	SYSRESET*
75	(RESERVED)	76	(RESERVED)
77	SECIEN*	78	ACFAIL*
79	(RESERVED)	80	SYSFAIL*
81	BERR*	82	(RESERVED)
83	AM0*	84	AM1*
85	AM2*	86	AM6*
87	IRQ1*	88	IRQ2*
89	IRQ3*	90	IRQ4*
91	IRQ5*	92	IRQ6*
93	IRQ7*	94	AM5*
95	ACKIN*	96	ACKOUT*
97	BG0IN*	98	BG0OUT*
99	BG1IN*	100	BG1OUT*
101	BG2IN*	102	BG2OUT*
103	BG3IN*	104	BG3OUT*
105	BG4IN*	106	BG4OUT*
107	BR0*	108	BR1*
109	BR2*	110	BR3*
111	BR4*	112	BBSY*
113	BCLR*	114	BREL*
115	(RESERVED)	116	(RESERVED)
117	(RESERVED)	118	(RESERVED)
119	GND	120	GND
121	−12V	122	−12V
123	GND	124	GND
125	+12V	126	+12V
127	+12V	128	+12V
129	+5V	130	+5V
131	+5V	132	+5V
133	+5V STDBY	134	+5V STDBY
135	GND	136	GND
137	GND	138	GND
139	GND	140	GND

NOTE
*ACTIVE LOW

J2/P2 PIN ASSIGNMENTS FOR 32-BIT EXPANSION

ODD PIN NUMBER (P_2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P_2 SOLDER SIDE)	SIGNAL MNEMONIC
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND (±15V)	14	GND (±15V)
15	−12V	16	−12V
17	(I/O PIN)	18	(I/O PIN)
19	(I/O PIN)	20	(I/O PIN)

"Our instruments must be more reliable than anything they test. It starts with additive boards."

J. W. Jaroszewski, Plant Manager, Dynascan Corporation

"Our goal in manufacturing B&K-Precision test equipment is to make them all an order of magnitude more reliable than anything they test. Several years ago we traced a number of potential reliability problems back to the soldering line where we had up to twenty different boards running at the same time. Photocircuits additive helped solve the problems.

"**As additive came in, touchup went down.**

"Because we had heard that additive boards enhanced solderability, we turned to Photocircuits Riverhead. We worked many Photocircuits additive boards into our product line. As they came in, touchup went down and reliability up.

"Today, no matter how we optimize our flow solder process, we know that the additive boards will properly solder with a high degree of tolerance to any process changes.

"**Additive means economical reliability.**

"Through use of microprocessors and large scale integration we are constantly packing more features into smaller, more portable units. The Photocircuits two-sided additive boards provide a highly reliable way to meet our design goals. They give the production economies and reliability we need in this highly competitive market.

"**Photocircuits plays a continuing part...**

"There's a fringe benefit in working with Photocircuits Riverhead. There's always an interchange with engineering before solidifying a new design. Our prototypes come in as fast as with a prototype house. And even though their plant is a thousand miles away, we've had troubleshooting help there within a day."

Whether you make test equipment—or are among the tested—the ease of soldering, reliability and service that come with our additive boards can help. Write or call Photocircuits Riverhead, Riverhead, N.Y. 11931. Or call (516) 722-4107. A Division of Kollmorgen Corporation.

Photocircuits Riverhead

Industry's largest additive capability

CIRCLE NO 78

J2/P2 PIN ASSIGNMENTS FOR 32-BIT EXPANSION (Cont)

ODD PIN NUMBER (P_2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P_2 SOLDER SIDE)	SIGNAL MNEMONIC
21	(I/O PIN)	22	(I/O PIN)
23	(I/O PIN)	24	(I/O PIN)
25	(I/O PIN)	26	(I/O PIN)
27	(I/O PIN)	28	(I/O PIN)
29	(I/O PIN)	30	(I/O PIN)
31	(I/O PIN)	32	(I/O PIN)
33	(I/O PIN)	34	(I/O PIN)
35	(I/O PIN)	36	(I/O PIN)
37	(I/O PIN)	38	(I/O PIN)
39	(I/O PIN)	40	(I/O PIN)
41	(I/O PIN)	42	(I/O PIN)
43	(I/O PIN)	44	(I/O PIN)
45	(I/O PIN)	46	(I/O PIN)
47	(I/O PIN)	48	(I/O PIN)
49	(I/O PIN)	50	(I/O PIN)
51	(I/O PIN)	52	(I/O PIN)
53	(I/O PIN)	54	(I/O PIN)
55	(I/O PIN)	56	(I/O PIN)
57	(I/O PIN)	58	(I/O PIN)
59	(I/O PIN)	60	(I/O PIN)
61	(I/O PIN)	62	(I/O PIN)
63	(I/O PIN)	64	(I/O PIN)
65	(I/O PIN)	66	(I/O PIN)
67	−15V	68	−15V
69	+15V	70	+15V
71	(RESERVED)	72	(RESERVED)
73	(RESERVED)	74	(RESERVED)
75	(RESERVED)	76	(RESERVED)
77	(RESERVED)	78	(RESERVED)
79	(RESERVED)	80	(RESERVED)
81	(RESERVED)	82	(RESERVED)
83	(RESERVED)	84	(RESERVED)
85	(RESERVED)	86	(RESERVED)
87	(RESERVED)	88	APARITY1*
89	A24*	90	A25*
91	A26*	92	A27*
93	A28*	94	A29*
95	A30*	96	A31*
97	GND	98	GND
99	(RESERVED)	100	(RESERVED)
101	GND	102	GND
103	DPARITY2*	104	DPARITY3*
105	D16*	106	D17*
107	D18*	108	D19*
109	D20*	110	D21*
111	D22*	112	D23*
113	D24*	114	D25*
115	D26*	116	D27*
117	D28*	118	D29*
119	D30*	120	D31*

NOTE:
PINS 17 THROUGH 66 ARE NOT CONNECTED TO THE BUS.

J2/P2 PIN ASSIGNMENTS FOR EXPANDED I/O

ODD PIN NUMBER (P_2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P_2 SOLDER SIDE)	SIGNAL MNEMONIC
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND

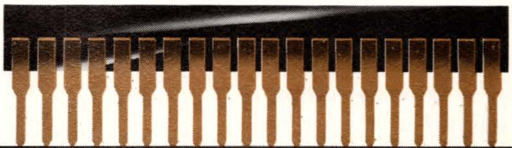
J2/P2 PIN ASSIGNMENTS FOR EXPANDED I/O (Cont)

ODD PIN NUMBER (P_2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P_2 SOLDER SIDE)	SIGNAL MNEMONIC
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND (±15V)	14	GND (±15V)
15	−12V	16	−12V
17	(I/O PIN)	18	(I/O PIN)
19	(I/O PIN)	20	(I/O PIN)
21	(I/O PIN)	22	(I/O PIN)
23	(I/O PIN)	24	(I/O PIN)
25	(I/O PIN)	26	(I/O PIN)
27	(I/O PIN)	28	(I/O PIN)
29	(I/O PIN)	30	(I/O PIN)
31	(I/O PIN)	32	(I/O PIN)
33	(I/O PIN)	34	(I/O PIN)
35	(I/O PIN)	36	(I/O PIN)
37	(I/O PIN)	38	(I/O PIN)
39	(I/O PIN)	40	(I/O PIN)
41	(I/O PIN)	42	(I/O PIN)
43	(I/O PIN)	44	(I/O PIN)
45	(I/O PIN)	46	(I/O PIN)
47	(I/O PIN)	48	(I/O PIN)
49	(I/O PIN)	50	(I/O PIN)
51	(I/O PIN)	52	(I/O PIN)
53	(I/O PIN)	54	(I/O PIN)
55	(I/O PIN)	56	(I/O PIN)
57	(I/O PIN)	58	(I/O PIN)
59	(I/O PIN)	60	(I/O PIN)
61	(I/O PIN)	62	(I/O PIN)
63	(I/O PIN)	64	(I/O PIN)
65	(I/O PIN)	66	(I/O PIN)
67	−15V	68	−15V
69	+15V	70	+15V
71	(I/O PIN)	72	(I/O PIN)
73	(I/O PIN)	74	(I/O PIN)
75	(I/O PIN)	76	(I/O PIN)
77	(I/O PIN)	78	(I/O PIN)
79	(I/O PIN)	80	(I/O PIN)
81	(I/O PIN)	82	(I/O PIN)
83	(I/O PIN)	84	(I/O PIN)
85	(I/O PIN)	86	(I/O PIN)
87	(I/O PIN)	88	(I/O PIN)
89	(I/O PIN)	90	(I/O PIN)
91	(I/O PIN)	92	(I/O PIN)
93	(I/O PIN)	94	(I/O PIN)
95	(I/O PIN)	96	(I/O PIN)
97	(I/O PIN)	98	(I/O PIN)
99	(I/O PIN)	100	(I/O PIN)
101	(I/O PIN)	102	(I/O PIN)
103	(I/O PIN)	104	(I/O PIN)
105	(I/O PIN)	106	(I/O PIN)
107	(I/O PIN)	108	(I/O PIN)
109	(I/O PIN)	110	(I/O PIN)
111	(I/O PIN)	112	(I/O PIN)
113	(I/O PIN)	114	(I/O PIN)
115	(I/O PIN)	116	(I/O PIN)
117	(I/O PIN)	118	(I/O PIN)
119	(I/O PIN)	120	(I/O PIN)

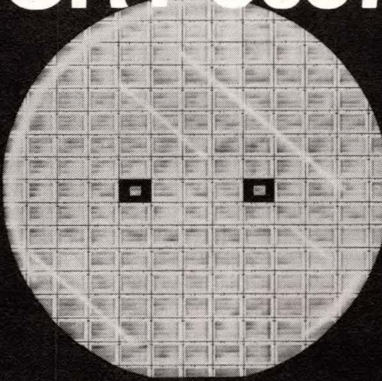
NOTE:
PINS 17 THROUGH 66 ARE NOT CONNECTED TO THE BUS.

Standard Microsystems creates two new standards from an old standard.

SMC UPDATE NO. 1



CRT 5047
CRT 5057



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STANDARD MICROSYSTEMS CORPORATION

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CIRCLE NO 80

Z-BUS BACKPLANE INTERCONNECT (ZBI)

SOURCE

Zilog Corp
10460 Bubb Rd
Cupertino, CA 95014
Phone (408) 446-4666

GENERAL INFORMATION

The Zilog Z-Bus is a shared system bus that links the various components of the Z8000 family. All family components have a standard interface and commonality of features.

The Z-Bus comprises five bus structures: a memory bus, an I/O bus, an interrupt bus and two resource-request buses. These buses share some data and control signals.

The general features of the Z-Bus include:

- Juxtaposition of five different buses
- Transparent bus where peripherals can be asynchronous from the CPU's clock
- Overlapped I/O and memory bus using multiplexed address and data
- Address can be 16 bits or extended using segmentation
- Data can be eight or 16 bits
- Interrupt bus uses daisy chain for detection, and execution priority-interrupt protocol uses vectors for peripheral identification
- Resource-request buses also use daisy chains
- A general-purpose command structure exists for all peripherals.

As with the previously described high-performance buses, the Z-Bus is considered a bus for the '80s and beyond. Moreover, it also incorporates the master/slave concept for development of a system network.

BUS SIGNALS

The Z-Bus, or ZBI, consists of 96 lines: 32 bidirectional address/data lines with four parity lines, nine interrupt lines, 28 control lines, 21 power-supply lines for ±12V, ±5V and ground and two reserve lines. The pin layout was defined to provide the most convenient connection from the board and the backplane, with signals collected into logical groups for placement on the connector. The following table defines the signal necessary to the ZBI structure:

NOTES

LOW≤0.5V
HIGH≤+2.4V

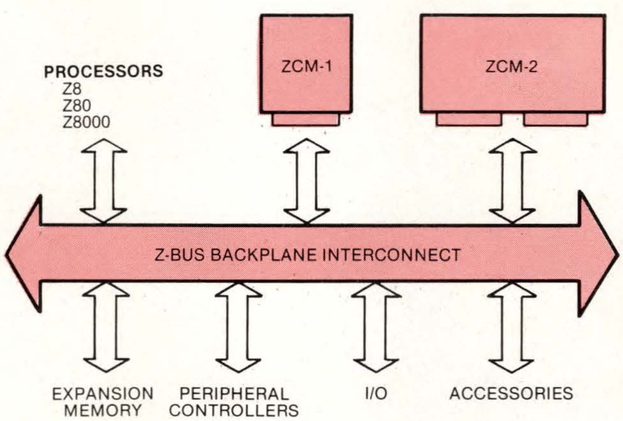
Any exception to this standard is noted in the table. Naming conventions are as follows:

NAME\	An active-LOW single line
NAME	An active-HIGH single line
NAME<0:n>	n active-HIGH lines
NAME1/NAME2\	A double-named line, HIGH/ LOW voltage levels

The abbreviations used to describe signal-driver types are:

TS	3-state driven lines
OC	Open collector
HC	High-current driver line, not 3-state
DC	Daisy-chained signal—OUT on one board connects to IN of the next board

Z-BUS BACKPLANE INTERCONNECT



BUS SIGNALS (Cont)

Signal Name	Number of Lines	Driver Type	Function
AD<0:31>	32	TS	Address and Data Lines
	Address and data information is time-multiplexed onto these lines. The times they are valid are defined by address strobe (AS\) and data strobe (DS\). Additional information can be derived from the BLCK signal for synchronous operation. For 8-bit transfers, data is aligned in the lower byte ($AD_{0\text{-}7}$) of the data field, while for 16-bit transfers, data is word aligned on the lower word of the data field ($AD_{0\text{-}15}$).		

SYSTEM-INTEGRITY LINES

Signal Name	Number of Lines	Driver Type	Function
P<0:3>	4	TS	Parity Check Bits
	For bus-transfer integrity, one parity bit is provided for each byte of the 32-bit address/data bus. Even parity ensures that a read from a nonexistent resource will generate a parity fault, because the bus terminators will pull the undriven data lines to an odd (incorrect) parity state. The parity bits are generated by the module placing data on the bus. The parity bits are checked by the module receiving data from the bus.		
PE\	1	OC	Parity Error
	Indicates to the bus master that a parity error in a data transfer on the bus has been caught by the parity-check logic on the module receiving the data. Parity is not checked on address transfers. The bus master's response to PE\ is arbitrary. It might, for example, cause a nonmaskable interrupt; it might retry the bus transaction, or it might continue with no action.		

STATUS LINES

Signal Name	Number of Lines	Driver Type	Function
ST<0:4>	5	TS	Status Lines
	These lines designate the type of transaction occurring on the bus.		
R/W\	1	TS	Read/Write
	If this line is HIGH, the current operation is a read; if LOW, a write		
N/S\	1	TS	Normal/System
	Indicates the mode of the CPU controlling the bus—normal User mode (HIGH) or System mode (LOW) (able to execute privileged instructions).		
B/W\	1	TS	Byte/Word Select
	Used in conjunction with W/LW\ to define data-access width.		
W/LW\	1	TS	Word/Long-Word Select
	Used in conjunction with B/W\ to define the data-access width.		

TRANSACTION-CONTROL LINES

Signal Name	Number of Lines	Driver Type	Function
AS\	1	TD	Address Strobe
	The AS\ line is driven LOW by the bus master to initiate a bus transaction. The trailing (rising) edge indicates that Address and Status are valid.		
DS\	1	TS	Data Strobe
	Data is transmitted on the AD bus lines when DS\ is LOW.		
WAIT\	1	OC	WAIT
	The WAIT\ line implements a means by which a responding module can suspend the bus master while a slow operation (eg, memory read or write) completes.		
STOP\	1	OC	Stop line
	Stops the processor in control of the bus for synchronization of activities.		

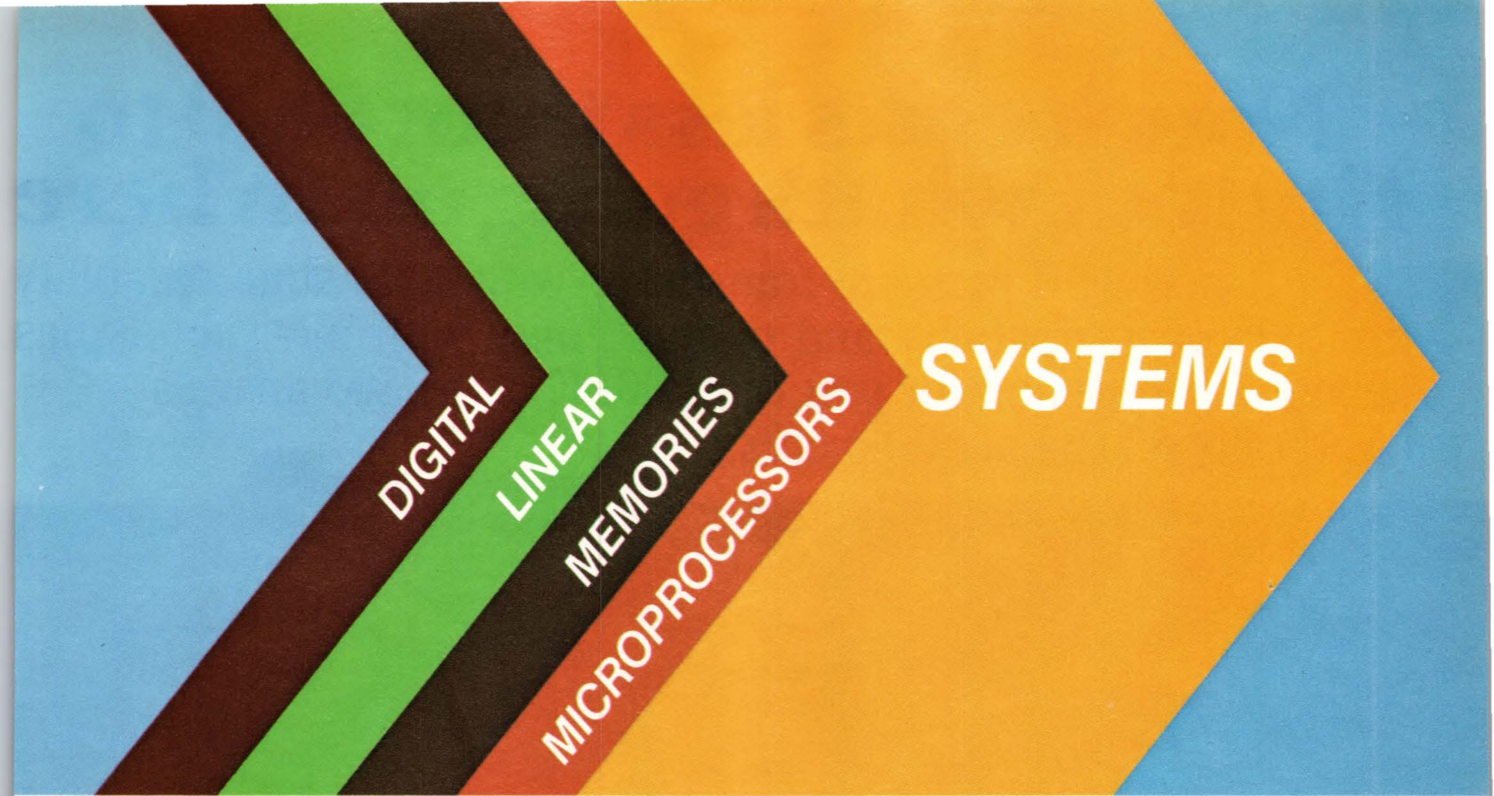
REQUEST LINES
BUS-ARBITRATION LINES
BUS-REQUEST LINES

Signal Name	Number of Lines	Driver Type	Function
BAI\	1	DC	Bus Acknowledge In From Priority Chain
	This signal and BAO\ form the bus-priority chain.		
BAO\	1	DC	Bus Acknowledge Out to Priority Chain
	Completes the circuit to the next module in the bus-priority chain.		
BUSREQ\	1	OC	Bus Request
	Used to request access to the bus; a request to a bus controller to relinquish the bus. This signal is used with BAI\ and BAO\ signals to control bus sharing by DMA modules.		

EXTENDED-ARBITRATION LINES

These lines are not fully defined in this version of the bus specification. They are reserved for the functions given below.

Signal Name	Number of Lines	Driver Type	Function
CAI\	1	DC	CPU Acknowledge In
CAO\	1	DC	CPU Acknowledge Out
CPUREQ\	1	OC	CPU Request
CAVAIL	1	TS	CPU Available



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For the past few months we've been telling you about all the benefits of chip carrier IC devices — benefits like reliability, ease of use, versatility, increased densities, board space and weight and production cost savings. We've talked about leadless ceramic chip carriers (LCCCs) for TI digital, linear, memory, and microprocessor ICs — and now, all the features, functions and many benefits of the individual components mean dramatic improvements in systems production, size, cost, and, of course, performance. The system solution for VLSI ... and beyond.

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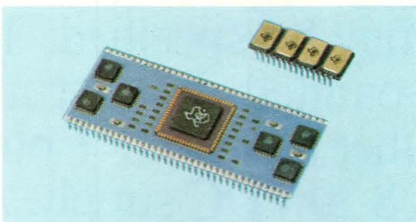
Compared with conventional IC devices, TI LCCCs provide many system production advantages. They can be placed automatically on PC boards by magazine-fed machines, always properly aligned, with address board pins top or bottom. So, production is faster because fewer assembly steps are required.



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TEXAS INSTRUMENTS
INCORPORATED

82930

CIRCLE NO 82

BUS SIGNALS (Cont)

INTERRUPT LINES

Signal Name	Number of Lines	Driver Type	Function
INT1\	1	OC	Level 1 Interrupt
	Highest priority interrupt in the system. If a nonmaskable interrupt is present, it must be here.		
INT2\	1	OC	Level 2 Interrupt
	Second highest priority interrupt in the system. If a vectored interrupt is present, it should be here.		
INT3\	1	OC	Level 3 Interrupt
	Lowest priority in the system. If a nonvectored interrupt is present, it should be here.		
IEI1	1	DC	Level 1 Interrupt Enable In
	1	DC	Level 1 Interrupt Enable Out
IEI2	1	DC	Level 2 Interrupt Enable In
IE02	1	DC	Level 2 Interrupt Enable Out
IEI3	1	DC	Level 3 Interrupt In
IE03	1	DC	Level 3 Interrupt Out
	These signals form the daisy chain for each of the three interrupt levels.		

RESOURCE-REQUEST LINES

Signal Name	Number of Lines	Driver Type	Function
MMREQ\	1	OC	Multimicro Request
	A software request to another processor for software synchronization.		
MMAI\	1	DC	Multimicro Acknowledge In
	Forms the logical chain among processors to perform software arbitration, in conjunction with the MMA0\ signal.		
MMA0\	1	DC	Multimicro Acknowledge Out
	Completes the logical chain to the next processor in the resource-request priority chain.		

SYSTEM-CONTROL LINES

Signal Name	Number of Lines	Driver Type	Function
PWRBAD\	1	OC	Power Bad
	An early-warning signal that the dc power for the system will soon disappear. This signal is generated by the power supply to give the processor enough time to store the machine state (if appropriate storage is available) before power drops below critical levels.		
MCLK	1	HC	Master Clock
	System master clock—Frequency is a 4× multiple of the BCLK frequency. MCLK is normally supplied by the bus controller.		
BCLK	1	HC	Bus Clock
	Bus-transaction clock. Derived from master clock and used by all synchronous elements in the system. BCLK is normally supplied by the bus controller.		
RESET\	1	OC	Reset
	Connected to the debounced master reset switch and power-up reset circuit. RESET initializes the entire system.		

TIMING CHARACTERISTICS

The following diagrams and tables give the timing for each kind of transaction (except null transactions). The full transaction consists of the following:

1) A requester gains control of the bus via the BUSREQ\ sequence if it is not already the bus master

2) The bus master lowers AS\.

3) The bus master gates Address and Status onto the bus.

4) The bus master raises AS\.

WRITES (Memory or I/O):

W5) The bus master gates DATA onto the bus.

W6) The bus master lowers DS\.

W7) The responder lowers WAIT\ if its response time exceeds the maximum.*

W8) The responder reads in the data the bus master is sending to it over the bus.

W9) The responder raises WAIT\ to indicate that it has accepted the data (if it lowered WAIT\ in step W7).

W10) The bus master raises DS\. This is the moment that the bus master samples the PE\ line. (See the definition of PE\ for an explanation of responses to a parity error.)

W11) The bus master removes the data from the bus.

W12) The bus master relinquishes control of the bus (3-states its address/data, status, word select and strobes), if it is not the bus controller.

READS (Memory, I/O, Interrupt Acknowledge)

R5) The bus master removes Address and Status from the bus (3-states its drivers).

R6) The bus master lowers DS\.

R7) The responder lowers WAIT\ if its response time is longer than the required maximum.*

R8) The responder gates the data onto the bus.

R9) The responder raises WAIT\ (if it was lowered in step R7)

R10) The bus master inputs the data from the bus.

R11) The bus master checks parity and removes DS\.

R12) The responder removes the data from the bus (3-states its drivers).

R13) The bus master relinquishes control of the bus, if it is not the bus controller.

NULL OPERATIONS (Memory Refresh, NOP, Aborted Reads)

N5) The bus master removes Address and Status from the bus.

N6) The bus master relinquishes control of the bus, if it is not the bus controller.

Note

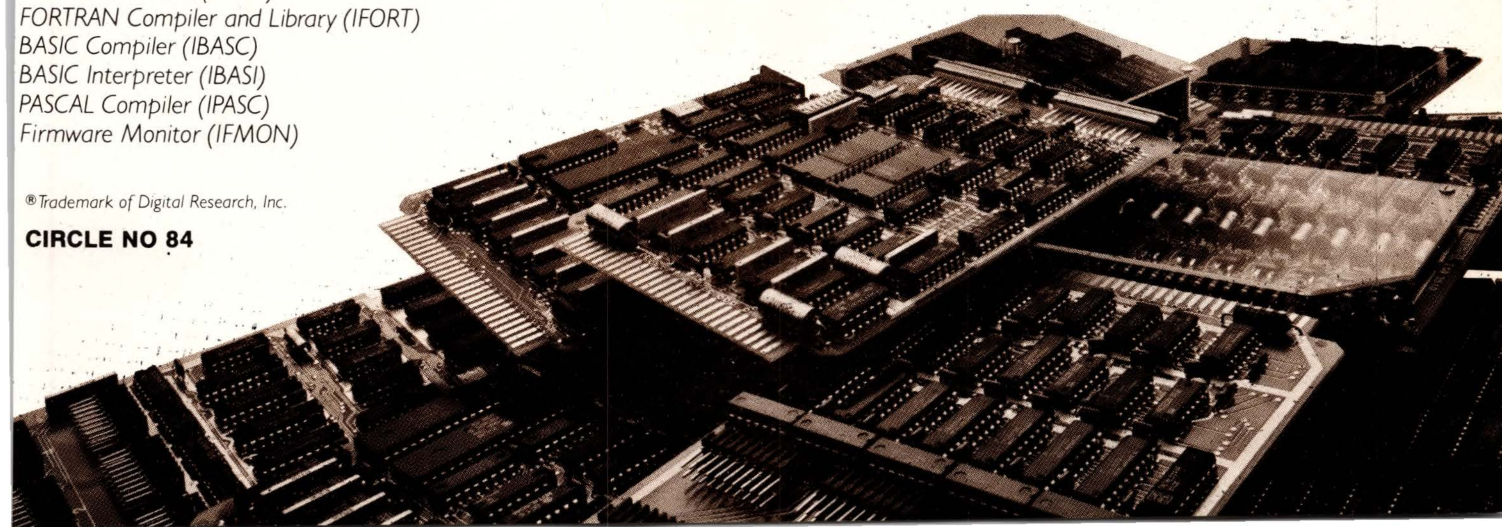
*A responder module need not use the WAIT\ line if it is in a system where the maximum access time of all modules is matched so that the minimum response-time requirement of each bus master is greater than the maximum response time of each responder, or the maximum response time of the responder is less than one clock cycle.

			4 MHz		6 MHz		8 MHz	
#	SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX
		MEMORY TRANSACTIONS	(nSEC)	(nSEC)	(nSEC)	(nSEC)	(nSEC)	(nSEC)
M1	TwDSR	DS\(READ) LOW WIDTH	250	185	166	125	125	95
M2	TdC(DSR)	T2 ↑ TO DS\(READ) ↓ DELAY	0		0		0	
M3	TdA(DSR)	ADDRESS NOT VALID TO DS\(READ) ↓ DELAY	0		0		0	
M4	TwDSW	DS\(WRITE) LOW WIDTH	150		100		75	
M5	TdC(DSW)	T2 ↑ TO DS\(WRITE) ↓ DELAY	0	250	0	166	0	125
M6	TsWT(C)	WAIT\ ↓ TO T3 ↓ SETUP TIME	50		30		25	
M7	TdC(WT)	T3 ↓ TO WAIT\ ↑ DELAY	25		25		25	
M8	TdAS(A)	AS\ ↑ TO ADDRESS NOT ACTIVE DELAY	10		10		10	
M9	TsA(C)	ADDRESS VALID TO T2 ↑ SETUP TIME	10		10		10	
		I/O TRANSACTIONS						
P1	TdAS(A)	AS\ ↑ TO ADDRESS NOT ACTIVE DELAY	50		30		25	
P2	TdA(DSI)	ADDRESS TO DS\(I/O) ↓ DELAY	0		0		0	
P3	TwDSI	DS\(I/O) LOW WIDTH	400		265		200	
P4	TdC(DSI)	T2 ↓ TO DS\(IO) ↓ DELAY	0	185	0	125	0	95
P5	TsWT(C)	WAIT\ ↓ TO Tw ↓ SETUP TIME	50		30		25	
P6	TdC(WT)	Tw ↓ TO WAIT\ ↑ DELAY	25		25		25	
		INTERRUPT ACKNOWLEDGE						
I1	TdAS(DSA)	AS\ ↑ TO DS\(ACK) ↓ DELAY	1000		665		500	
I2	TwDSA	DS\(ACK) LOW WIDTH	450		300		250	
I3	TdDSA(DI)	DS\(ACK) ↓ TO READ DATA VALID DELAY		375		250		190
I4	TdDSA(WT)	DS\(ACK) ↓ TO WAIT\ ↓ DELAY		95		65		50
I5	TsWT(C)	WAIT\ ↓ TO Tw ↓ SETUP TIME	50		30		25	
I6	TdC(WT)	Tw ↓ TO WAIT\↑ DELAY	25		25		25	
		ALL TRANSACTIONS	(nSEC)	(nSEC)	(nSEC)	(nSEC)	(nSEC)	(nSEC)
A1	TdcMC	MCLK DUTY CYCLE TIME	26	36	16	26	11	21
A2	TdMC(C)	MCLK ↑ TO BCLK ↑ DELAY	−7	7	−7	7	−7	7
A3	TcC	BCLK PERIOD	250		166		125	
A4	TdcC	BCLK DUTY CYCLE TIME	120	130	78	88	58	68
A5	TrC	BCLK RISE TIME		10		10		10
A6	TfC	BCLK FALL TIME		10		10		10
A7	TwAS	AS\ LOW WIDTH	80		55		40	
A8	TsASf(C)	AS\ ↓ TO T1 ↓ SETUP TIME	10	125	10	83	10	62
A9	TdC(AS)	T1 ↓ TO AS\ ↑ DELAY	20		20		20	
A10	TsASr(C)	AS\ ↑ TO T2 ↓ SETUP TIME	60		40		30	
A11	TdAS(DS)	AS\ ↑ TO DS\ ↓ DELAY	50		30		25	
A12	TdDS(AS)	DS\ ↑ TO AS\ ↓ DELAY	50		30		25	
A13	TdC(S)	T1 ↑ TO STATUS VALID DELAY		185		125		95
A14	TsS(AS)	STATUS VALID TO AS\ ↑ SETUP TIME	50		30		25	
A15	TdDS(S)	DS\ ↑ TO STATUS NOT VALID	60		40		30	
A16	TdC(DS)	T3 ↓ TO DS\ ↑ DELAY	0	125	0	83	0	62
A17	TsA(AS)	ADDRESS VALID TO AS\ ↑ SETUP TIME	35		35		35	
A18	TsDI(C)	READ DATA TO T3 ↓ SETUP TIME	60		40		30	
A19	TdDS(DI)	DS\ ↑ TO READ DATA NOT VALID	0		0		0	
A20	TsPR(C)	READ PARITY BITS TO T3 ↓ SETUP TIME	32		20		15	
A21	TdDS(PR)	DS\ ↑ TO READ PARITY BITS NOT VALID DELAY	0		0		0	

NOTES

↑ — LOW-TO-HIGH TRANSITION

↓ — HIGH-TO-LOW TRANSITION



#	SYMBOL	PARAMETER	4 MHz MIN	4 MHz MAX	6 MHz MIN	6 MHz MAX	8 MHz MIN	8 MHz MAX
A22	TsDO(DS)	WRITE DATA TO DS\ ↓ SETUP TIME	32		20		15	
A23	TdDS(DO)	DS\ ↑ TO WRITE DATA NOT VALID DELAY	32		20		15	
A24	TsPW(DS)	WRITE PARITY BITS TO DS\ ↓ SETUP TIME	0		0		0	
A25	TdDS(PW)	DS\ ↑ TO WRITE PARITY BITS NOT VALID DELAY	10		10		10	
A26	TsPE(C)	PE\(WRITE) ↓ TO T3 ↓ SETUP TIME	32		20		15	
A27	TdDS(PE)	DS\ ↑ TO PE\ ↑ DELAY	0		0		0	
A28	TwRS	RESET\ LOW WIDTH	1250		830		625	
A29	TwINT1	INT1\ LOW WIDTH	125		83		62	
A30	TdBR-Q(BAO)	BUSREQ\ ↓ TO BAO\ ↓ DELAY (BUS CONTROLLER)	250		166		125	

#	SYMBOL	PARAMETER	MIN (nSEC)	MAX (nSEC)
		ALL TRANSACTIONS		
A1	TdcMC	MCLK DUTY CYCLE TIME	*	*
A2	TdMC(C)	MCLK ↑ TO BCLK ↑ DELAY	−7	7
A3	TcC	BCLK PERIOD	**	
A4	TdcC	BCLK DUTY CYCLE TIME	*	*
A5	TrC	BCLK RISE TIME		10
A6	TfC	BCLK FALL TIME		10
A7	TwAS	AS\ LOW WIDTH	1/3TcC	
A8	TsASf(C)	AS\ ↓ TO T1 ↓ SETUP TIME	10	1/2TcC
A9	TdC(AS)	T1 ↓ TO AS\ ↑ DELAY	20	
A10	TsASr(C)	AS\ ↑ TO T2 ↓ SETUP TIME	1/4TcC	
A11	TdAS(DS)	AS\ ↑ TO DS\ ↓ DELAY	1/5TcC	
A12	TdDS(AS)	DS\ ↑ TO AS\ ↓ DELAY	1/5TcC	
A13	TdC(S)	T1 ↑ TO STATUS VALID		3/4TcC
A14	TsS(AS)	STATUS VALID TO AS\ ↑ SETUP TIME	1/5TcC	
A15	TdDS(S)	DS\ ↑ TO STATUS NOT VALID	1/4TcC	
A16	TdC(DS)	T3 ↓ TO DS\ ↑ DELAY	0	1/2TcC
A17	TsA(AS)	ADDRESS VALID TO AS\ ↑ SETUP TIME	35	
A18	TsDI(C)	READ DATA TO T3 ↓ SETUP TIME	1/4TcC	
A19	TdDS(DI)	DS\ ↑ TO READ DATA NOT VALID	0	
A20	TsPR(C)	READ PARITY BITS TO T3 ↓ SETUP TIME	1/8TcC	
A21	TdDS(PR)	DS\ ↑ TO READ PARITY BITS NOT VALID DELAY	0	
A22	TsDO(DS)	WRITE DATA TO DS\ ↓ SETUP TIME	1/8TcC	
A23	TdDS(DO)	DS\ ↑ TO WRITE DATA NOT VALID DELAY	1/8TcC	
A24	TsPW(DS)	WRITE PARITY BITS TO DS\ ↓ SETUP TIME	0	
A25	TdDS(PW)	DS\ ↑ TO WRITE PARITY BITS NOT VALID DELAY	10	
A26	TsPE(C)	PE\(WRITE) ↓ TO T3 ↓ SETUP TIME	1/8TcC	
A27	TdDS(PE)	DS\ ↑ TO PE\ ↑ DELAY	0	
A28	TwRS	RESET\ LOW WIDTH	5TcC	
A29	TwINT1	INT1\ LOW WIDTH	1/2TcC	
A30	TdBRQ(BAO)	BUSREQ\ ↓ TO BAO\ ↓ DELAY (BUS CONTROLLER)	TcC	

#	SYMBOL	PARAMETER	MIN (nSEC)	MAX (nSEC)
		MEMORY TRANSACTIONS		
M1	TwDSR	DS\(READ) LOW WIDTH	TcC	
M2	TdC(DSR)	T2 ↑ TO DS\(READ) ↓ DELAY	0	3/4TcC
M3	TdA(DSR)	ADDRESS NOT VALID TO DS\(READ) ↓ DELAY	0	
M4	TwDSW	DS\(WRITE) LOW WIDTH	3/5TcC	
M5	TdC(DSW)	T2 ↑ TO DS\(WRITE) ↓ DELAY	0	TcC
M6	TsWT(C)	WAIT\ ↓ TO T3 ↓ SETUP TIME	1/5TcC	
M7	TdC(WT)	T3 ↓ TO WAIT\ ↑ DELAY	25	
M8	TdAS(A)	AS\ ↑ TO ADDRESS NOT ACTIVE DELAY	10	
M9	TsA(C)	ADDRESS VALID TO T2 SETUP TIME	10	
		I/O TRANSACTIONS		
P1	TdAS(A)	AS\ ↑ TO ADDRESS NOT ACTIVE DELAY	1/5TcC	
P2	TdA(DSI)	ADDRESS TO DS\(I/O) ↓ DELAY	0	
P3	TwDSI	DS\(I/O) LOW WIDTH	1.6TcC	
P4	TdC(DSI)	T2 ↓ TO DS\(I/O) ↓ DELAY	0	3/4TcC
P5	TsWT(C)	WAIT\ ↓ TO Tw ↓ SETUP TIME	1/5TcC	
P6	TdC(WT)	Tw ↓ TO WAIT\ ↑ DELAY	25	
		INTERRUPT ACKNOWLEDGE		
I1	TdAS(DSA)	AS\ ↑ TO DS\(ACK) ↓ DELAY	4TcC	
I2	TwDSA	DS\(ACK) LOW WIDTH	1.8TcC	
I3	TdDSA(DI)	DS\(ACK) ↓ TO READ DATA VALID DELAY		1.5TcC
I4	TdDSA(WT)	DS\(ACK) ↓ TO WAIT\ ↓ DELAY		3/8TcC
I5	TsWT(C)	WAIT\ ↓ TO Tw ↓ SETUP TIME	1/5TcC	
I6	TdC(WT)	Tw ↓ TO WAIT\ ↑ DELAY	25	

NOTES

* DUTY CYCLE IS MEASURED BETWEEN 50% OF RISING AND FALLING EDGES OF THE CLOCK AND IS DEFINED TO BE HALF OF THE CLOCK PERIOD + 5 nSEC.

** TcC(4 MHz) = 250 nSEC, TcC(6 MHz) = 166 nSEC, TcC(8 MHz) = 125 nSEC.

↑ LOW-TO-HIGH TRANSITION

↓ HIGH-TO-LOW TRANSITION

ELECTRICAL SPECIFICATIONS

POWER SPECIFICATIONS

DC LOADS per signal line	0.5 mA max per card
AC LOADS per signal line	20 pF max per card
CARDS PER SYSTEM	20 max
LENGTH OF BUS	20 in. max
DRIVERS (3-state)	24-mA LOW-level output current, −1.2-mA HIGH-level output current
DRIVERS (high current)	32-mA LOW-level output current, −1.2-mA HIGH-level output current
DRIVERS (open collector)	40-mA LOW-level output current

All connector pins are rated at 1.5A max per contact, continuous duty, 70°C. The maximum current per card might not be attainable depending on limits imposed by system power supplies. Use of the maximum power on all power pins could result in exceeding the maximum board heat dissipation provided by the standard fans. This limit must be checked on all boards.

The four common power-supply voltages, +5, +12, −5, and −12V, are provided on the backplane as a part of this specification. Other voltages can be provided as required in specific systems on the second connector on ZCM-2 or ZCM-2X boards. Note that currents given are maximum per card and are based upon the number of contacts.

ZCM-1 BOARDS

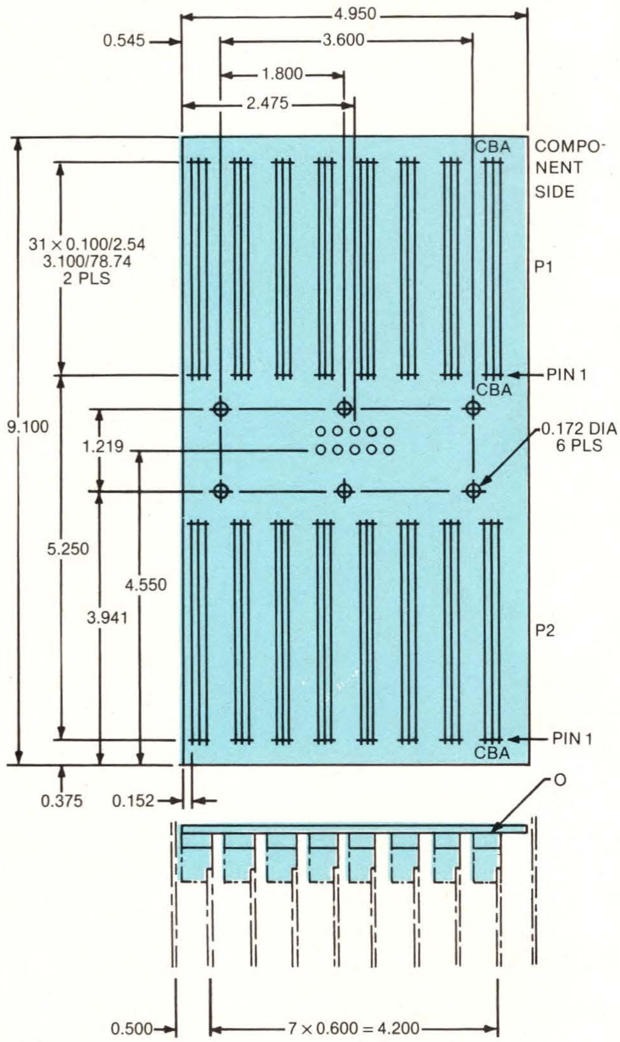
Voltage (V)	Number	Maximum Current per Card (A)
+5	3	4.5
−5	3	4.5
+12	3	4.5
−12	3	4.5
GND	9	Ground, evenly distributed across connectors
	Total 21	

ZCM-2 OR ZCM-2x BOARDS

Voltage (V)	Number	Maximum Current per Card (A)
+5	6	9
−5	6	9
+12	6	9
−12	6	9
GND	18	Ground, evenly distributed across connectors
	Total 42	

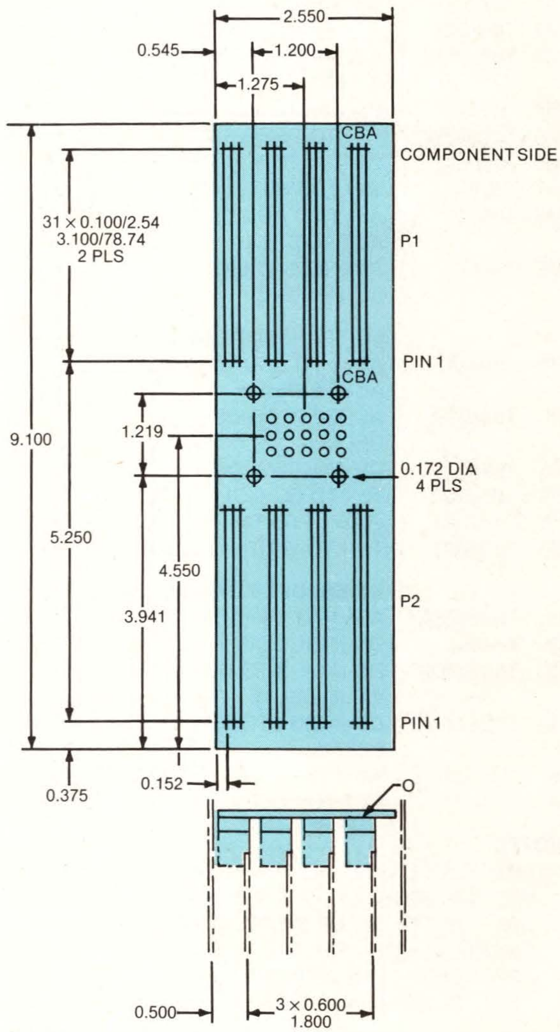
MECHANICAL SPECIFICATIONS

BACKPLANE CONFIGURATION (ZCM2-SCC/8)



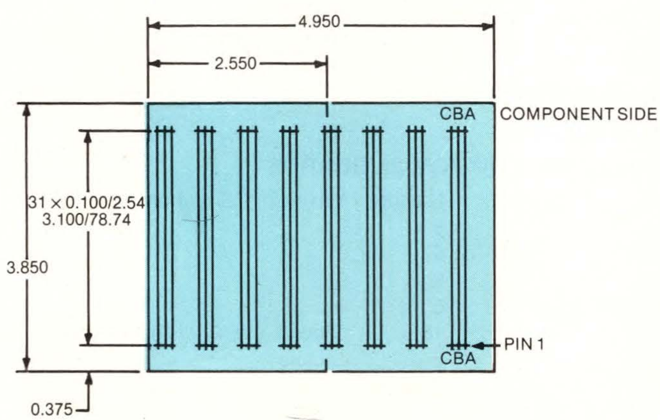
NOTE
O AMP 164303-4 164313-1
PANDUIT 102-096-451 100-096-459
BURNDY NP13B96R-2 NP13B96R-3
AMPHENOL 128-396-0625

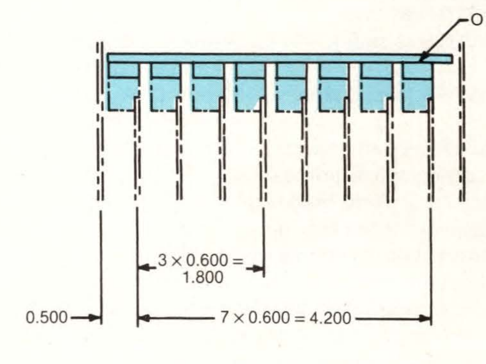
BACKPLANE CONFIGURATION (ZCM2-SCC/4)



NOTE
O AMP 164303-4 164313-1
PANDUIT 102-096-451 100-096-459
BURNDY NP13B96R-2 NP13B96R-3
AMPHENOL 128-396-062S

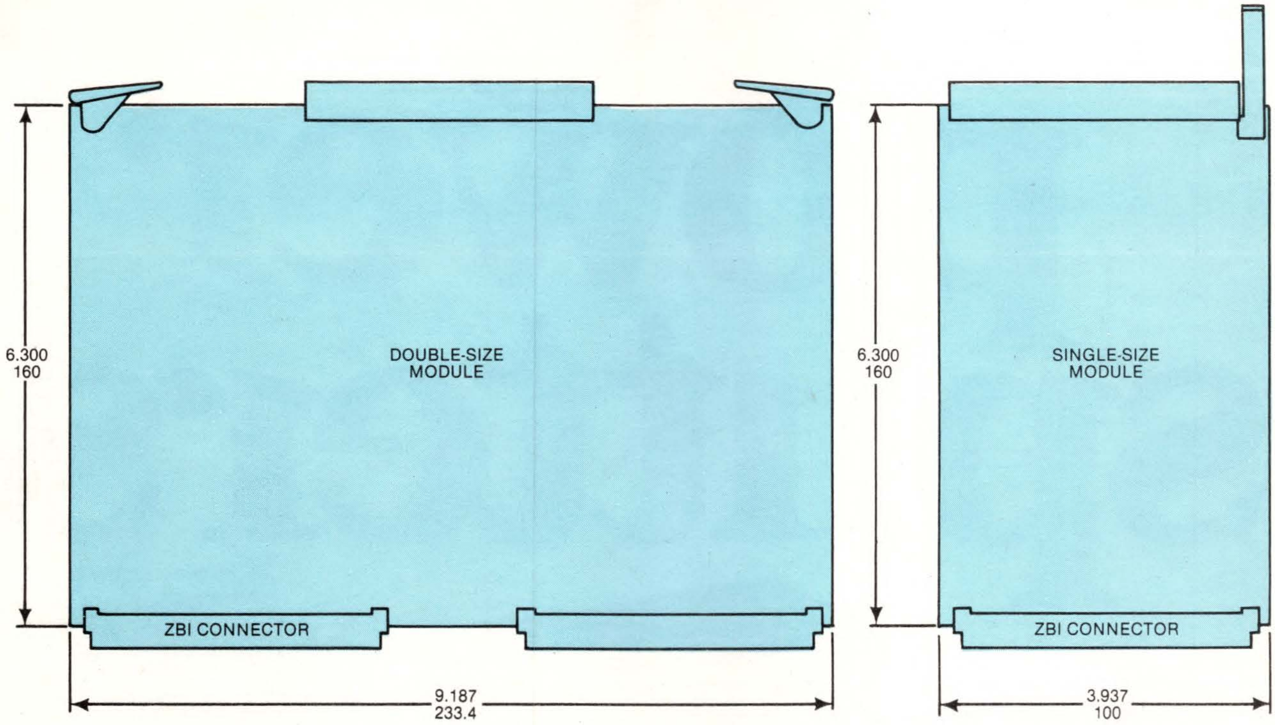
BACKPLANE CONFIGURATION (ZCM1-SCC/4/, /8)





NOTE
O AMP 164303-4 164313-1
PANDUIT 102-096-451 100-096-459
BURNDY NP13B96R-2 NP13B96R-3
AMPHENOL 128-396-062S

CARD SIZES



PIN ASSIGNMENTS

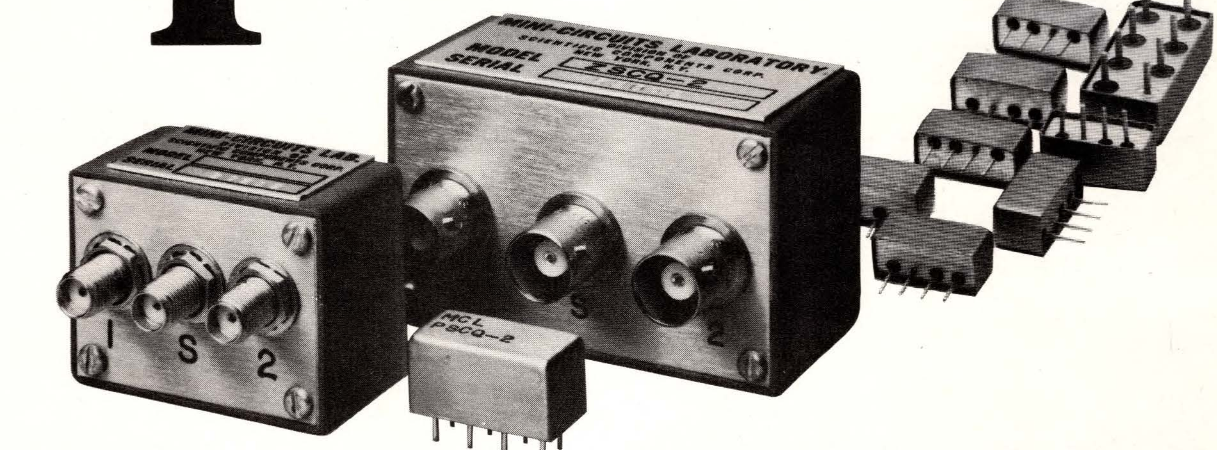
	A	B	C		A	B	C
32	GND	GND	GND	16	* AD28	* AD29	* AD30
31	−12V	−12V	−12V	15	* AD31	* P0	GND
30	+12V	+12V	+12V	14	* P1	* P2	* P3
29	−5V	−5V	−5V	13	* RESERVED	* STOP\	* N/S
28	+5V	+5V	+5V	12	* PE\	* AS\	* DS\
27	* PWRBAD\	* MCLK	* BCLK	11	* S0	* S1	GND
26	* AD0	* AD1	* AD2	10	* S2	* S3	* S4
25	* AD3	* AD4	* AD5	9	* R/W\	* B/W\	* W/LW\
24	* AD6	* AD7	* AD8	8	* INT1\	* INT2\	* INT3\
23	* AD9	* AD10	GND	7	! IEI1	! IEO1	GND
22	* AD11	* AD12	* AD13	6	! IEI2	! IEO2	* RESERVED
21	* AD14	* AD15	* AD16	5	! IEI3	! IEO3	* MMREQ\
20	* AD17	* AD18	* AD19	4	! MMAI\	! MMAO\	GND
19	* AD20	* AD21	GND	3	! BAI\	! BAO\	* BUSREQ\
18	* AD22	* AD23	* AD24	2	! CAI\	! CAO\	* CPUREQ\
17	* AD25	* AD26	* AD27	1	* RESET\	* WAIT\	* CPUAVAIL

NOTES

*THESE LINES ARE INDIVIDUALLY TERMINATED WITH A 330Ω RESISTOR TO +5V AND A 470Ω RESISTOR TO GROUND.

! THE DAISY-CHAIN INPUT SIGNALS, THOSE ON ROW A OF THE CONNECTOR, ARE WIRED ON THE BACKPLANE TO THE DAISY-CHAIN OUTPUT SIGNALS OF THE PREVIOUS CARD SLOT'S CONNECTOR ROW B. EACH PC CARD MUST SHORT DAISY-CHAIN IN PINS TO DAISY-CHAIN OUT PINS FOR ALL OF THOSE DAISY CHAINS IT DOES NOT USE.

90° power splitters



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90° SERIES SPECIFICATIONS

Model No.	Freq. Range MHz	Isolation dB		Insertion Loss dB*		Phase Unbalance Degrees	Amplitude Unbalance dB	Price $	
		Typ.	Min.	Typ.	Max.	Max.	Max.	Each	Qty.
PSCQ-2-1.5	1.4-1.7	29	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-3.4	3.0-3.8	30	25	0.4	0.7	3.0	1.2	16.95	(5-49)
PSCQ-2-6.4	5.8-7.0	30	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-7.5	7.0-8.0	35	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-10.5	9.0-11.0	25	20	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-13	12-14	29	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-14	12-16	30	25	0.3	0.6	3.0	1.8	16.95	(5-49)
PSCQ-2-21.4	20-23	30	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	19.95	(5-49)
PSCQ-2-70	40-70	25	20	0.3	0.7	3.0	1.2	19.95	(5-49)
PSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	19.95	(5-49)
PSCQ-2-120	80-120	25	18	0.3	0.7	3.0	1.5	19.95	(5-49)
PSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	19.95	(5-49)
PSCQ-2-250	150-250	23	18	0.4	0.8	4.0	1.5	19.95	(5-49)
PSCQ-2-400	250-400	22	16	0.4	0.9	4.0	1.5	19.95	(5-49)
PSCQ-2-450	350-450	22	16	0.4	0.9	4.0	1.5	19.95	(5-49)
ZSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	39.95	(4-24)
ZSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	39.95	(4-24)
ZSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	39.95	(4-24)
ZMSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	49.95	(4-24)
ZMSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	49.95	(4-24)
ZMSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	49.95	(4-24)

*Average of coupled outputs less 3 dB   Impedance 50 ohms all models

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CIRCLE NO 85

Design Ideas

Edited by George Huffman

Exerciser tests n-bit DACs for 8 words

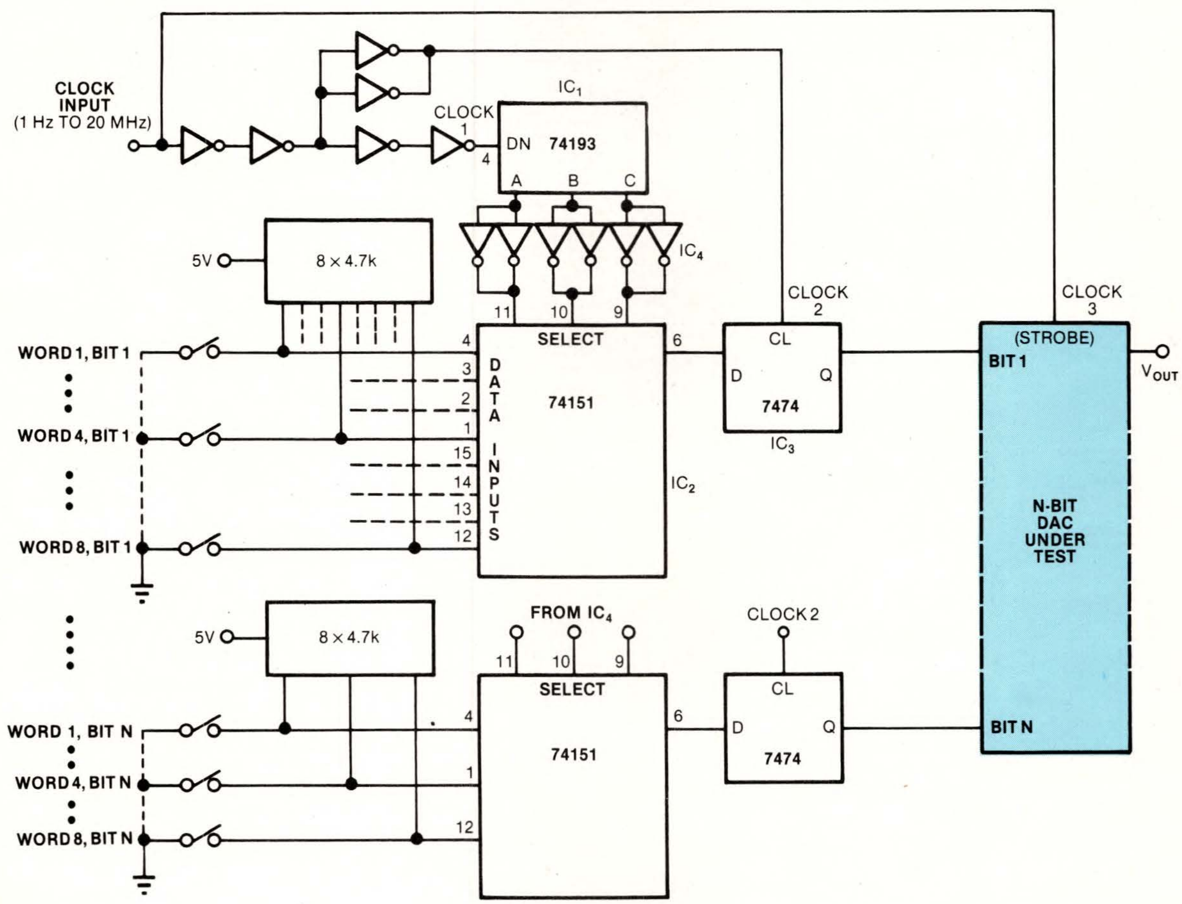
Robert A Pease
National Semiconductor Corp, Santa Clara, CA

Testing a DAC for settling time and glitches ideally calls for stepping it through a sequence of worst-case bit-combination words. For example, a simple but important 4-bit-DAC test can be 0110-0111-1000-1001... You should also have the option of performing these tests over a wide range of clock (strobe) frequencies: You might find that high-speed DACs—such as those used as video-display drivers—exhibit a settle-to-0V time that depends on how long they remain at a high-level output.

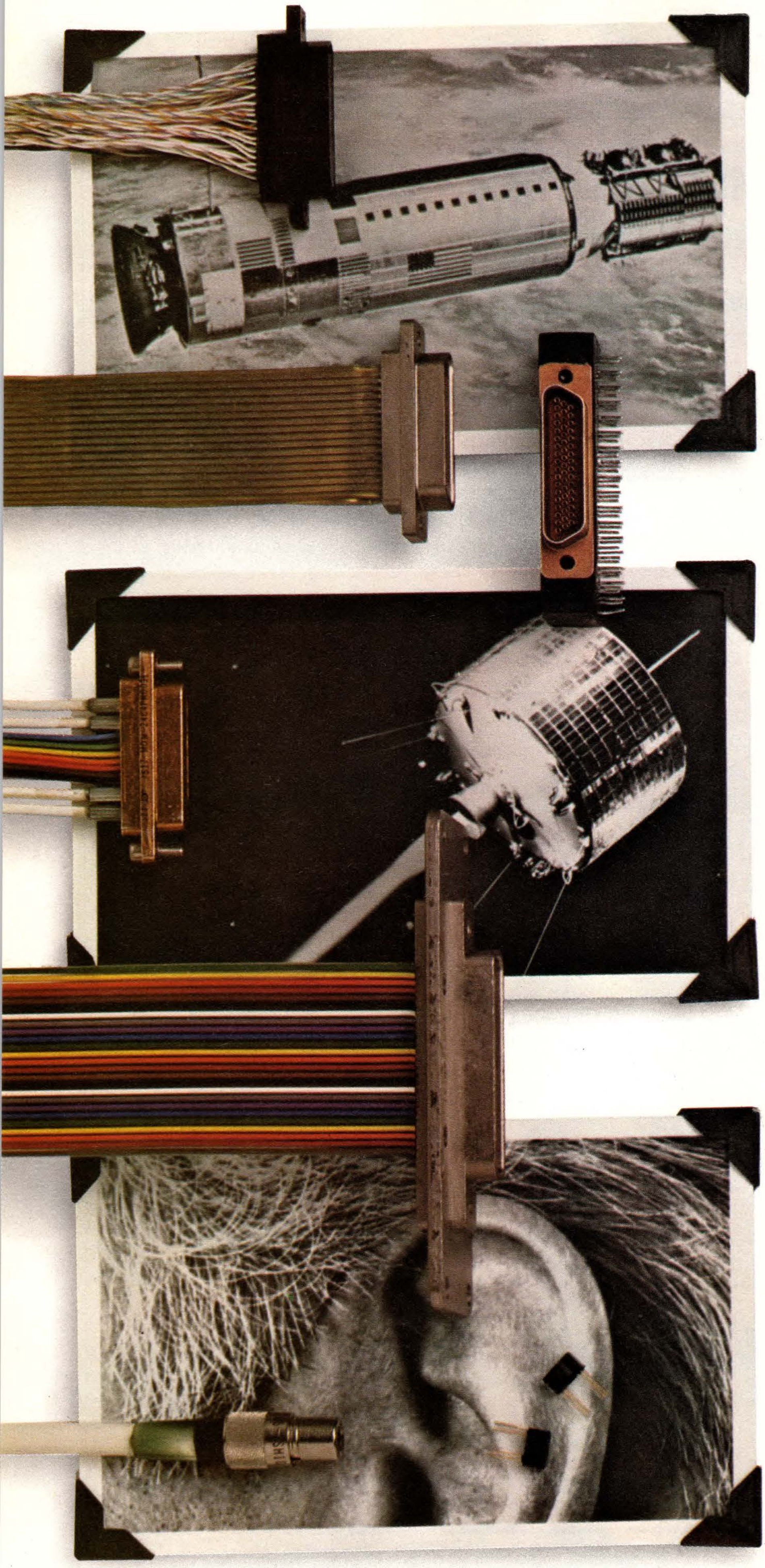
The DAC exerciser shown in the **figure** generates eight consecutive words; you set each word's bit pattern with the appropriate switches as indicated. Thus, to test an 8-bit DAC, you need 64 switches arranged in an 8-word×8-bit matrix. But because these connections are dc, long wire runs or large matrices won't cause any problems.

You can vary the clock's frequency between 1 Hz and 25 MHz; differential skew among all of the DAC input bits typically remains less than 500 psec. Note how some of the inverter ICs serve as clock-delay

Continued on pg 192



Exercising a DAC *requires nothing more than entering the appropriate 8-word×n-bit codes via a switch matrix. Counter IC_1 generates the eight successive addresses that in turn (via the 1-of-8 decoders) parallel-select the switch bank. The selected inputs get latched into the 7474 D flip flops and presented to the DAC under test. (Note that the flip flops' Q outputs are used; the $\overline{Q}$ signal occurs about 2 nsec later and could therefore produce misleading DAC-settling-time indications.)*



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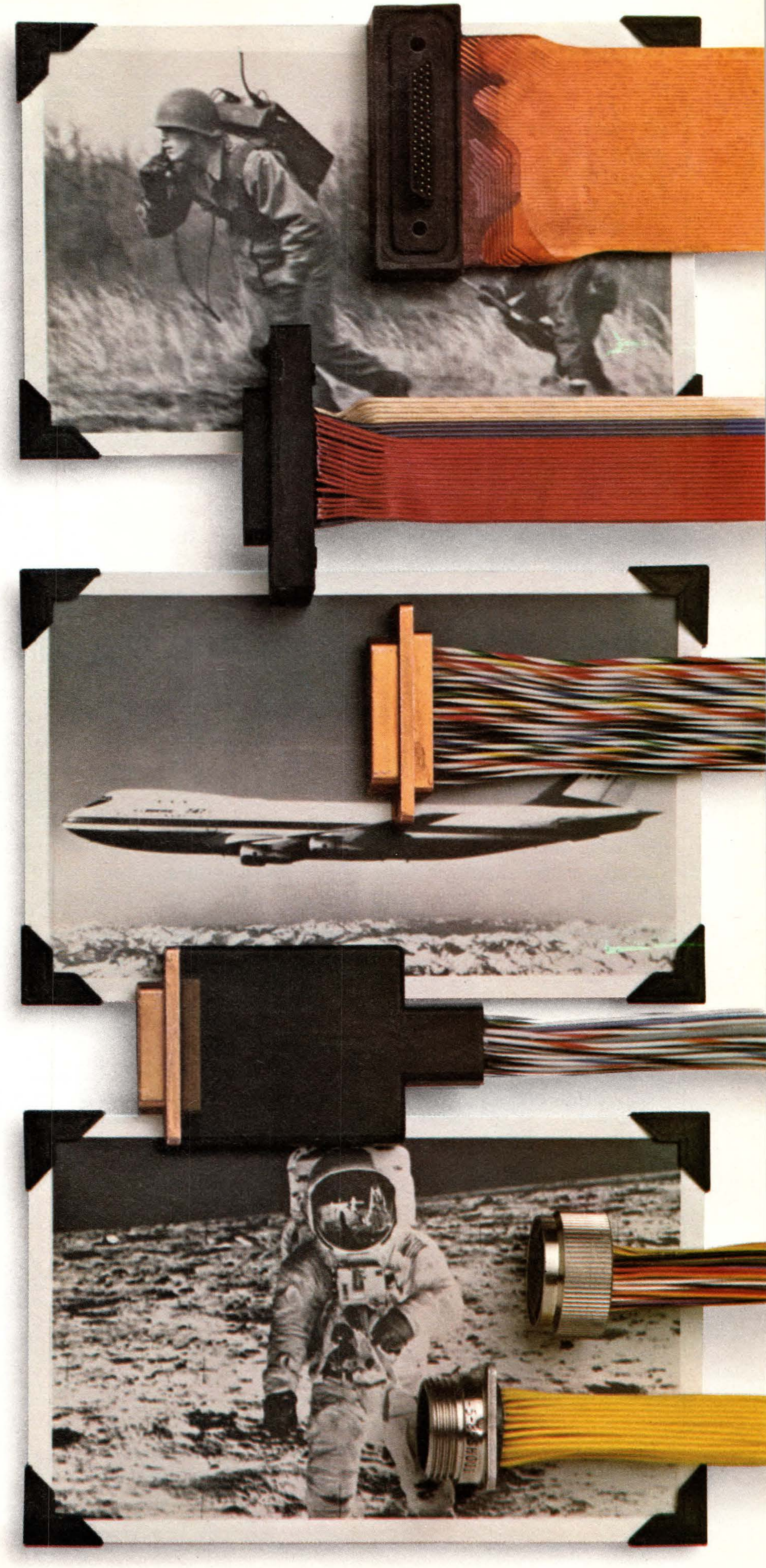


generators, ensuring that whether or not the DAC under test requires a strobe, the incoming data word has settled and been latched by the D flip flops (IC_3, for example) before the time you expect a valid V_{OUT}.

For engineering purposes, the switch-matrix approach is sufficient; it's inexpensive and easily programmed. But for production or incoming-inspection situations requiring a large number of possibly different tests, you can incorporate a modification that puts the entire test sequence under µP control without doing away with the capability of running occasional engineering-type tests. You can, for example, incorporate 3-state latches or dual-input OR gates in the data-input lines to the 74151 1-of-8 decoders.

In the latter case, tie one of the OR gates' inputs to the appropriate switch and the other input to the µP's output bus. Thus, to achieve a switch-controlled input, the µP's inputs must be all ZEROs, and when the switch's outputs are all ZEROs, the µP takes over. (Be careful with this scheme, though; you might have to include AND gates in the design to ensure that the switch settings aren't contending with the µP.)

Using an OR gate, 3-state latch or similar component, you can program the test-data inputs via computer at the relatively slow rate of 100 or so changes per second and still exercise a DAC at 200 bits/µsec or more. **EDN**

To Vote For This Design, Circle No 450

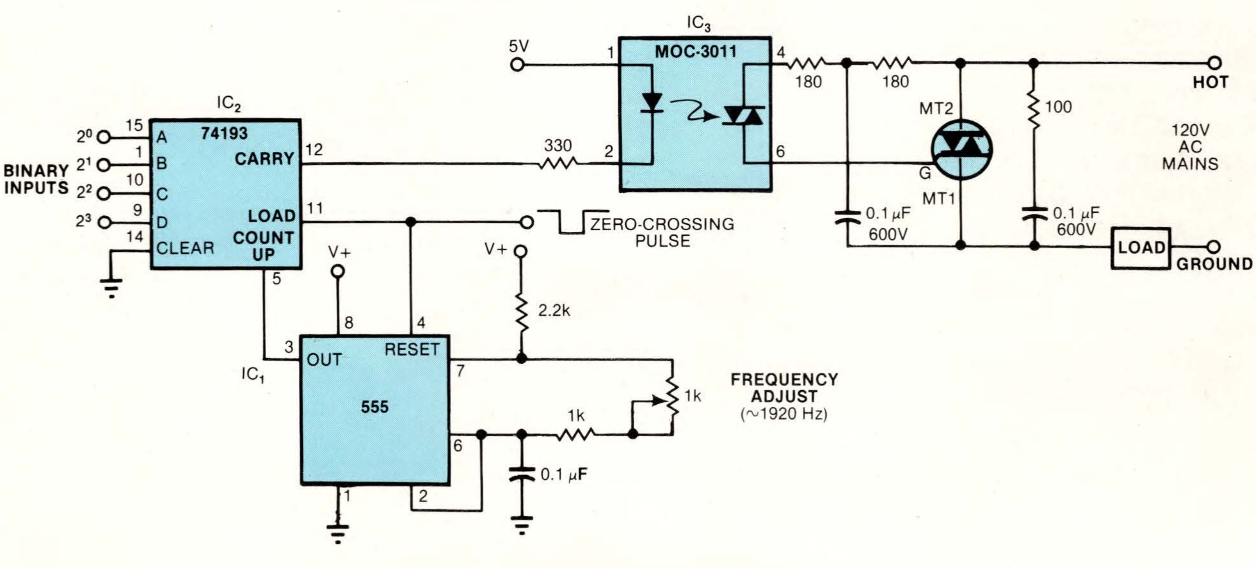
Three ICs control triacs digitally

Julian R Bryttan
Amtrak-CSD, Washington, DC

By using the design shown in the **figure,** you can directly control a triac's firing phase angle with a 4-bit data input. Thus, with either a µP/µC or thumbwheel set you can determine a lamp's intensity or a motor's speed. And if your application requires even finer control, you can easily expand this design's basic concept.

Configure IC_1 as a synchronizable astable oscillator running at approximately 1920 Hz. The oscillator's output drives IC_2's Count Up input. This presettable counter generates a Carry output when

Continued on pg 196



Triac phase-angle firing *occurs when the counter's preloaded binary input value is overflowed by the oscillator's signal. At this time, the Carry output drops LOW, turning on the optocoupler's LED and thus the triac. The next zero crossing resets the oscillator and reloads the counter in preparation for the following cycle.*

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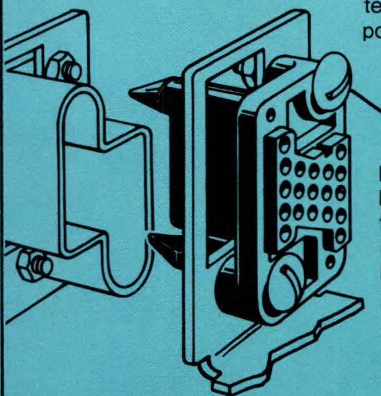
AMP Facts

Power Distribution module eliminates tedious point-to-point wiring.



Drawer connector has .090" radial float and integral alignment for blind mating applications.

For more information, call the AMP Metrimate Desk at (717) 780-8400.

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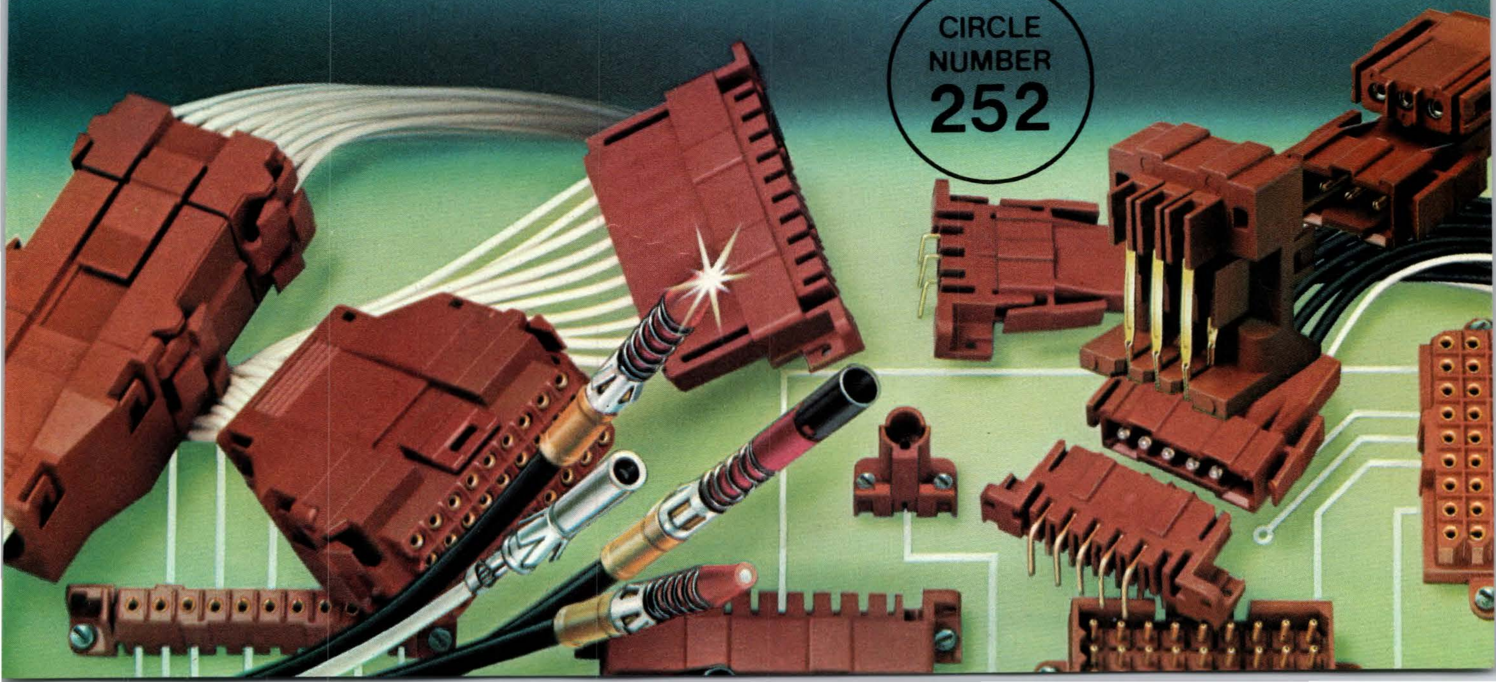
CIRCLE NUMBER 252



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3636-1	2K x 8	65ns
3636	2K x 8	80ns
3628A-1	1K x 8	50ns
3628A-3	1K x 8	70ns
3628A-4	1K x 8	90ns
M3636 (Military)	2K x 8	80ns

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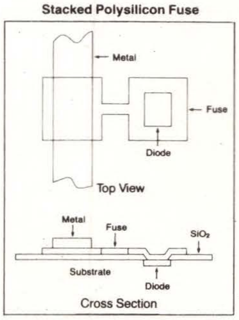

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CIRCLE NO 91

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it overflows; that pulse in turn fires the triac via optocoupler IC_3.

To control the triac, enter the appropriate binary code into the counter's Load inputs—all ZEROs correspond to completely off. A zero-crossing pulse (see *Ed Note*) resets the oscillator and concurrently loads the data into the counter.

The counter starts counting up until it overflows. This action forces the Carry output LOW, turns on the optocoupler's LED and fires the triac. The next zero-crossing pulse resets the circuits, and (assuming you haven't changed the input data) the triac refires during the subsequent cycle at exactly the same phase angle.

Set the oscillator's frequency to keep the triac barely off with an all-ZEROs data input. (In practice, you might want to prolong an incandescent load's life by providing it with a keep-alive or glow voltage. In that case, adjust the oscillator's frequency to the point where the counter overflows just before the end of a mains cycle.)

Note that you can easily expand this design's control resolution by cascading counters and employing additional input bits. But don't forget to double the oscillator's operating frequency for each binary level you add.

(Ed Note: Your particular application will determine what you employ as a zero-crossing detector/pulse generator. Some designs provide an output pulse only once per cycle (ie, when the mains voltage is going positive or negative, but not both). In addition to this consideration, keep in mind that the zero-crossing detector's stability is also important, especially if you expand the triac controller's resolution. A well-designed zero-crossing detector was described in "60-Hz synchronizer offers stability, safety," which appeared in this department in the May 27 issue.) EDN

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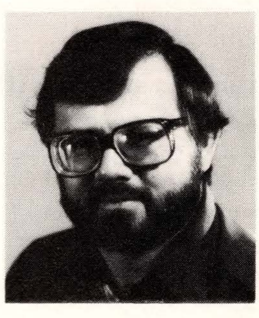
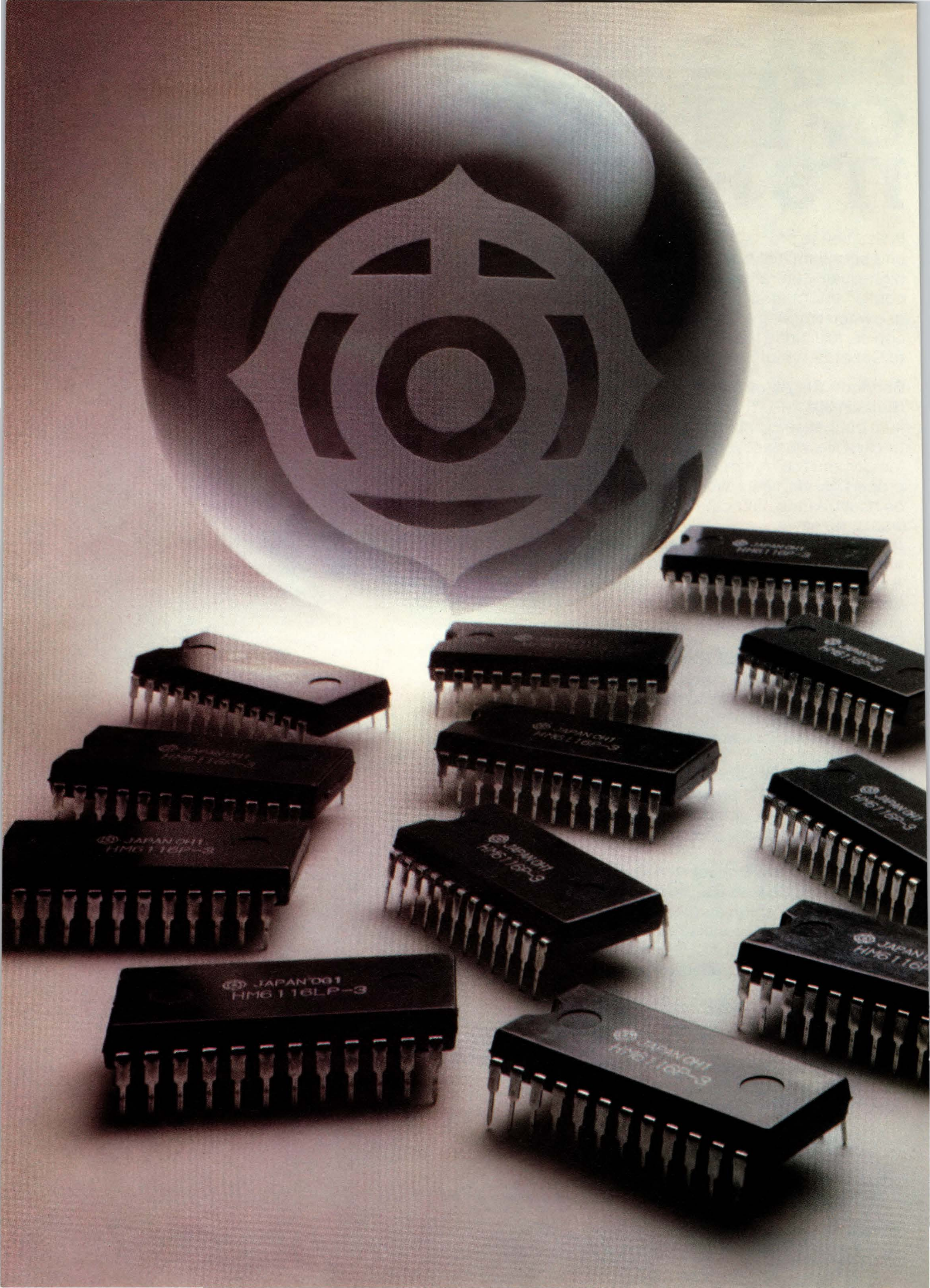


Larry McDonald winner of the October 5, 1980 US Savings Bond Award. His winning design is "Diode-connected FET protects op amps." Mr McDonald is with Burr-Brown Research Corp, Tucson, AZ.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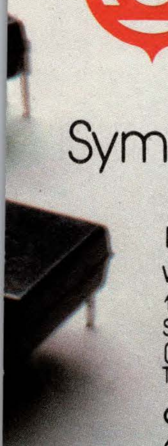

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μC Design Techniques

EDN Software Note #71

Check system RAM in real time

John J O'Flaherty
Radio Telefis Eireann, Dublin, Ireland

In critical real-time μC applications such as process control and monitoring, system-RAM integrity is vital. Faulty RAM bits can cause false alarms, confusion or even dangerous executive action. The method described here allows the real-time software to continuously monitor every bit of system RAM without affecting the RAM's contents.

A simple routine (**figure**), if included in the system program's main loop, tests each RAM word. This particular program suits use with a TMS9900 μP. The test is based on two observations. First, the one's complement of a binary number toggles every bit of that number to its complement—inverts it. Other functions, such as two's complement, don't guarantee the exercise of every bit. Second, the sum of a binary number and its one's complement is always an all-HIGH binary number (eg, FF or FFFF). No other pair of equal-length binary numbers produces this result without a carry bit.

Thus, if a program inverts the RAM's contents, then sums that value wth the original value, the result is all Fs if the bits are good. To that end, this test looks at each RAM word individually and performs six functions:

- Move the contents to a scratch register
- Invert the word to form its one's complement
- Add the inverted value to the original value
- Check to see that the scratch register contains all ZEROs
- Invert the RAM word again to restore its contents to their original value. EDN

```
                *
                *
                *              ******************
                *              * RAMCHK ROUTINE *
                *              ******************
                *
                ****** CHECK SYSTEM RAM WITHOUT *******
                ******  AFFECTING ITS CONTENTS  *******
                *                                     *
                *METHOD: If RAM loc.OK then           *
                *        [val+INV(val)] = >FFFF.      *
                *        Scratch Reg.       = R0      *
                *        Counter/Status Reg. = R1     *
                *          Avoid these Regs.          *
                *          Use checks them.           *
                *        Normal RETURN through R11    *
                *ON RETURN: RAM Status in R1          *
                *           R1=0 => All RAM OK        *
                *           R1<>0=> R1=BAD RAM loc.   *
                *              & bad bits at 0<->1    *
                *                transitions in R0.   *
                *REGS.USED: R0,R1,R11                 *
                *CONSTANTS: RAM1 - First RAM location.*
                *           RAM2 - Last RAM location. *
                ***************************************
                *
0482 0201   RAMCHK LI R1,RAM1      First RAM loc.
0484 1000
            ****  Avoid R0 & R1 own locations. ****
0486 02A0   RL1    STWP R0         Put R0=loc.of R0
0488 8040          C R0,R1         Pting at Scratch?
048A 1309          JEQ RL2         If so skip it.
048C 05C0          INCT R0         Put R0=loc.of R1
048E 8040          C R0,R1         Pting at Counter?
0490 1306          JEQ RL2         If so skip it.
            ****   Check the RAM location.     ****
0492 C011          MOV *R1,R0      Loc.val.->Scratch
0494 0551          INV *R1         Loc.val's 1's Cmp
0496 A011          A *R1,R0        Sum=loc.val+inv.
0498 0540          INV R0          1's Comp.of Sum.
049A 1606          JNE RL3         Sum=0 => OK
049C 0551          INV *R1         Orig.loc.val.back
            ****     Next RAM location.        ****
049E 05C1   RL2    INCT R1         Next RAM word.
04A0 0281          CI R1,RAM2      All RAM done?
04A2 13FE
04A4 12F0          JLE RL1         If not, do next.
            ****   End of RAM so Return.       ****
04A6 04C1          CLR R1          RAM OK Status.
04A8 045B   RL3    RT              Ret.w.Stat.in R1
            *
            *
```

Test RAM bits continuously *by inserting this TMS9900-μP program into the main loop of your system software.*

BASIC subroutine selects resistances

Albert C Brunelli
White Mountain Electronics, Berlin, NH

When you write a program to aid in circuit design, it's useful to have a routine to convert all calculated resistance values to their nearest standard value. You can then determine the circuit's response with the values actually used in the circuit.

The BASIC program shown in **Fig 1** determines the nearest 5% standard value to the calculated value that you provide as an input. The procedure resembles the successive-approximation techniques used in A/D conversion.

Lines 140 through 200 create an ordered list of standard-value mantissas that the routine begins using at line 1000. Choosing the lowest possible values for the array maintains decimal-point shifting always to the left. (Storing integers in the array might save memory, but the subroutine would then have to be longer and more complex.)

Line 1000 sets the Out of Range flag to ZERO. If you later enter a value of less than 0.1Ω or more than 10 MΩ, lines 1020 and 1030 set the flag to ONE.

Line 1010 sets the decimal-point-shift counter to ZERO, and lines 1060 through 1090 shift the decimal point of the input value until the value falls within the table's range. The variable K stores the number of shifts used.

The binary search, beginning at line 1100, examines the value in the middle of the table. If this value equals the input value, the search stops. If the input value is greater than the table value, the routine ignores the table's bottom half and picks a new center value out of the top half. And if the input value is smaller than the table entry, the top half of the table gets ignored.

At some point, unless the input value *is* a standard resistance value, you run out of table without finding a match. Line 1170 then determines whether your input value is closer to the last value of B or E.

The program shown in **Fig 2** illustrates the use of this routine in designing an astable multivibrator

```
10 '
20 '     Subroutine to determine the nearest standard 5% resistor
30 '     value when given R from CAD program.
40 '
50 '     Program created for EDN          2/27/81
60 '             Updated                  3/3/81
70 '
80 '     Albert Brunelli
90 '     White Mountain Electronics
100 '
110 '    Writen in Microsoft BASIC VER 5.1
120 '
130 ' CREATE ARRAY FOR SELECTION
140 DIM A(25)
150 '                       STANDARD VALUE TABLE
160 DATA .1, .11, .12, .13, .15, .16, .18, .2, .22, .24, .27, .3, .33
170 DATA .36, .39, .43, .47, .51, .56, .62, .68, .75, .82, .91, 1
180 FOR I=1 TO 25
190      READ A(I)
200 NEXT I
210 '            SIMULATE DETERMINATION OF R
220 INPUT"Test value of R ";R
230 GOSUB 1000' USE SUBROUTINE TO DETERMINE NEAREST STANDARD VALUE
240 IF F<>1 THEN 270
250 PRINT"RESISTOR INPUT OUT OF RANGE. TRY AGAIN."
260 GOTO 220
270 PRINT"NEAREST STANDARD VALUE IS";R1
280 PRINT
290 INPUT"Shall we try another ";Y$
300 IF RIGHT$(Y$,1)="Y" THEN 220
310 END
320 ' SUBROUTINE BEGINS WITH FILTER FOR VALUES TOO BIG OR TOO SMALL
1000 F=0          'OUT OF RANGE FLAG
1010 K=0          'EXPONENT COUNTER
1020 IF R<.1 THEN F=1:RETURN    'RESISTOR TOO SMALL
1030 IF R>1E+07 THEN F=1:RETURN 'RESISTOR TOO LARGE
1040 R1=R
1050 '            GET VALUE WITHIN RANGE OF TABLE
1060 IF R1<=1 THEN 1100
1070 R1=R1/10     'SHIFT DECIMAL PLACE
1080 K=K+1        'COUNT THE SHIFTS
1090 GOTO 1060    'SEE IF IN RANGE YET
1100 B=1          'SET POINTER TO BEGINNING OF ARRAY
1110 E=25         'SET POINTER TO END OF ARRAY
1120 M=INT((B+E)/2)      'SET POINTER TOO MIDDLE OF USEFUL AREA
1130 IF M=B THEN 1170    'VALUE ENTERED WAS NOT STANDARD
1140 IF R1=A(M) THEN 1190        'VALUE ENTERED FOUND IN ARRAY
1150 IF R1<A(M) THEN E=M:GOTO 1120      'NEAREST VALUE BELOW POINTER M
1160 IF R1>A(M) THEN B=M:GOTO 1120      'NEAREST VALUE ABOVE POINTER M
1170 IF (R1-A(B))<(A(E)-R1) THEN R1=A(B) ELSE R1=A(E)
1180          'PICK NEAREST ONE. IF EQUIDISTANT, ROUND UP.
1190 R1=R1*10↑K          'RESTORE PROPER DECIMAL POINT
1200 IF R1>10 THEN R1=INT(R1+.5)         '10↑K GIVES OCCASIONAL ERRORS BECAUSE
1210                                     'BASIC USES BINARY ARITHMETIC
1220 RETURN
```

Fig 1—Use standard resistor values *in your design equations—send each calculated value to this routine to find the standard value nearest it.*

```
10 '
20 '     Design program for 555 astable multivibrator
30 '     Notation from National Semiconductor Linear Data Book, 1980
40 '
50 '     Program created for EDN          3/1/81
60 '             Updated                  3/3/81
70 '
80 '     Albert Brunelli
90 '     White Mountain Electronics
100 '
110 '    Writen in Microsoft BASIC VER 5.1
120 '
130 ' CREATE ARRAY FOR SELECTION
140 DIM A(25)
150 '                    STANDARD VALUE TABLE
160 DATA .1, .11, .12, .13, .15, .16, .18, .2, .22, .24, .27, .3, .33
170 DATA .36, .39, .43, .47, .51, .56, .62, .68, .75, .82, .91, 1
180 FOR I=1 TO 25
190     READ A(I)
200 NEXT I
210 PRINT CHR$(12)                'Clear screen
220 PRINT"       This program will calculate the two resistors and capacitor"
230 PRINT"needed to make a 555 astable multivibrator"
240 PRINT:PRINT"        Please type in the required duty cycle of the voltage"
250 PRINT"at pin 3. The duty cycle must be greater than 50% and less than 100%"
260 PRINT
270 INPUT"Duty cycle as a % ";D
280 IF D>0 THEN 310
290 PRINT"**** DUTY CYCLE OUT OF RANGE. TRY AGAIN. ****"
300 GOTO 240
310 IF D<1 THEN D=D*100           'ENTERED AS DECIMAL FRACTION
320 IF D<=50 THEN 290             'TOO SMALL
330 IF D>=100 THEN 290            'TOO LARGE
340 D=D/100                       'CREATE DECIMAL FRACTION
350 PRINT
360 PRINT"       Please type in the required frequency of the astable"
370 PRINT"The frequency must be greater than 0.1 Hz and less than 100 KHz."
380 PRINT:INPUT"Oscillating frequency ";F
390 IF F>.1 THEN 420
400 PRINT"*** FREQUENCY OUT OF RANGE. TRY AGAIN. ***"
410 GOTO 350
420 IF F<10 THEN C=.00001:GOTO 460
430 IF F<1000 THEN C=.0000001 :GOTO 460
440 IF F<100000! THEN C=1E-08 :GOTO 460
450 GOTO 400                      'FREQUENCY TOO HIGH
460 K1=LOG(2):K2=1/(K1*F*C)
470 RB=K2*(1-D)
480 RA=K2-2*RB
490 R=RB:GOSUB 1000:RB=R1
500 R=RA:GOSUB 1000:RA=R1
510 PRINT
520 PRINT"RA=";RA,"RB=";RB,"C=";C*1E+06;" microFarads"
530 PRINT"With the values shown above:"
540 PRINT"Frequency=",1/(K1*(RA+2*RB)*C)
550 PRINT"Duty cycle=",100*(RA+RB)/(RA+2*RB);" %"
560 PRINT:GOTO 240
570 '
580 '             SUBROUTINE BEGINS AT LINE 1000
590 '
1000 F=0          'OUT OF RANGE FLAG
1010 K=0          'EXPONENT COUNTER
1020 IF R<.1 THEN F=1:RETURN     'RESISTOR TOO SMALL
1030 IF R>1E+07 THEN F=1:RETURN 'RESISTOR TOO LARGE
1040 R1=R
1050 '            GET VALUE WITHIN RANGE OF TABLE
1060 IF R1<=1 THEN 1100
1070 R1=R1/10     'SHIFT DECIMAL PLACE
1080 K=K+1        'COUNT THE SHIFTS
1090 GOTO 1060    'SEE IF IN RANGE YET
1100 B=1          'SET POINTER TO BEGINNING OF ARRAY
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1120 M=INT((B+E)/2)      'SET POINTER TOO MIDDLE OF USEFUL AREA
1130 IF M=B THEN 1170    'VALUE ENTERED WAS NOT STANDARD
1140 IF R1=A(M) THEN 1190         'VALUE ENTERED FOUND IN ARRAY
1150 IF R1<A(M) THEN E=M:GOTO 1120      'NEAREST VALUE BELOW POINTER M
1160 IF R1>A(M) THEN B=M:GOTO 1120      'NEAREST VALUE ABOVE POINTER M
1170 IF (R1-A(B))<(A(E)-R1) THEN R1=A(B) ELSE R1=A(E)
1180              'PICK NEAREST ONE. IF EQUIDISTANT, ROUND UP.
1190 R1=R1*10↑K          'RESTORE PROPER DECIMAL POINT
1200 IF R1>10 THEN R1=INT(R1+.5)       '10↑K GIVES OCCASIONAL ERROR BECAUSE
1210                                   'BASIC USES BINARY ARITHMETIC
1220 RETURN
```
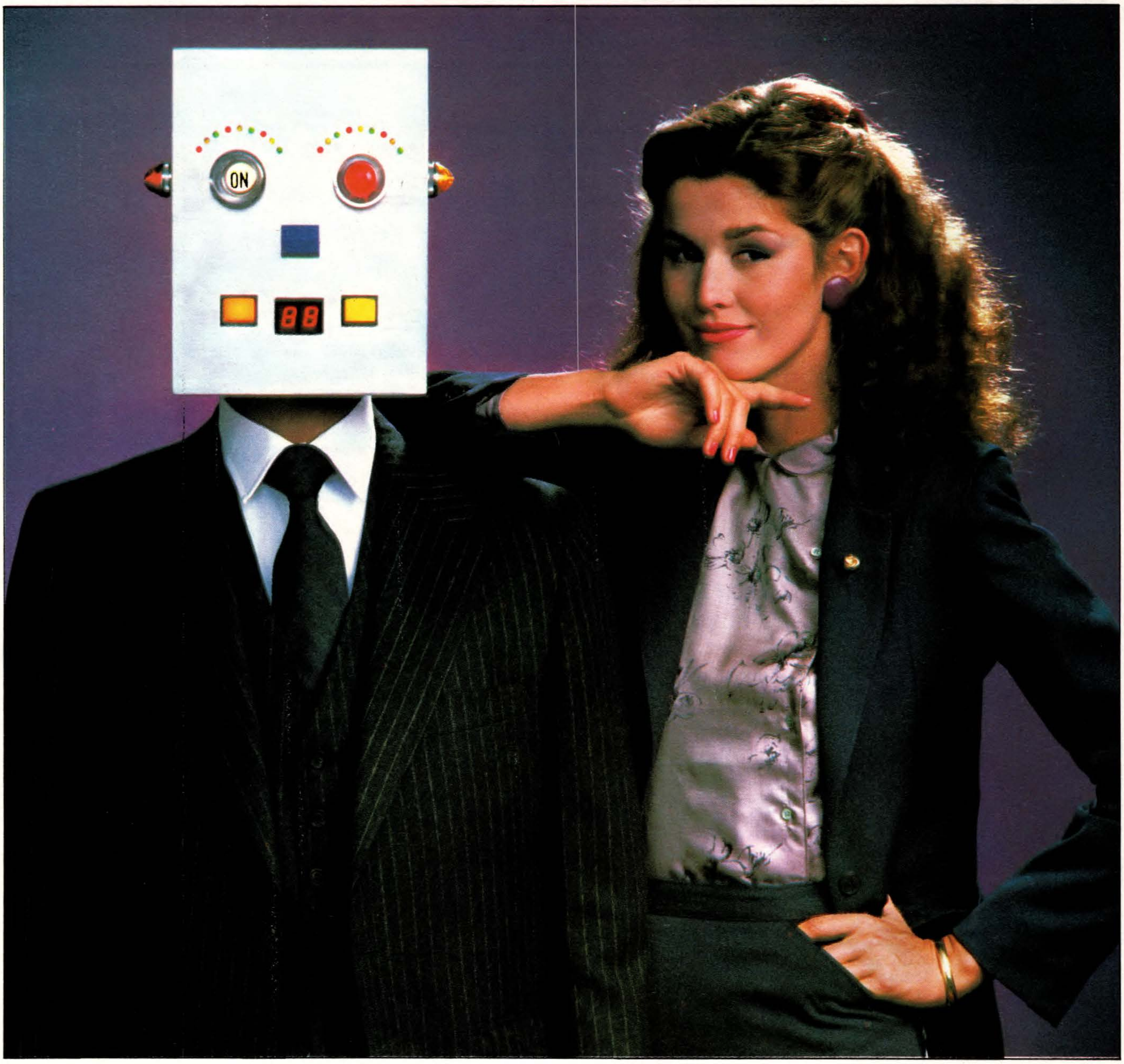

Fig 2—Designing an astable multivibrator *calls for sending the resistor values to the standardization subroutine before calculating frequency and duty cycle.*

TOPS THE BEST-DRESSED LIST.



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CIRCLE NO 99

with a 555 timer. The capacitor value gets chosen first on the assumption that it will provide reasonable resistor values in the final design. Solving two equations then produces values for R_A and R_B. The program sends these values to the subroutine to obtain the nearest standard values. Substituting the standard values into the design equation then provides the frequency and duty-cycle information. Finally, the program displays the results. **EDN**

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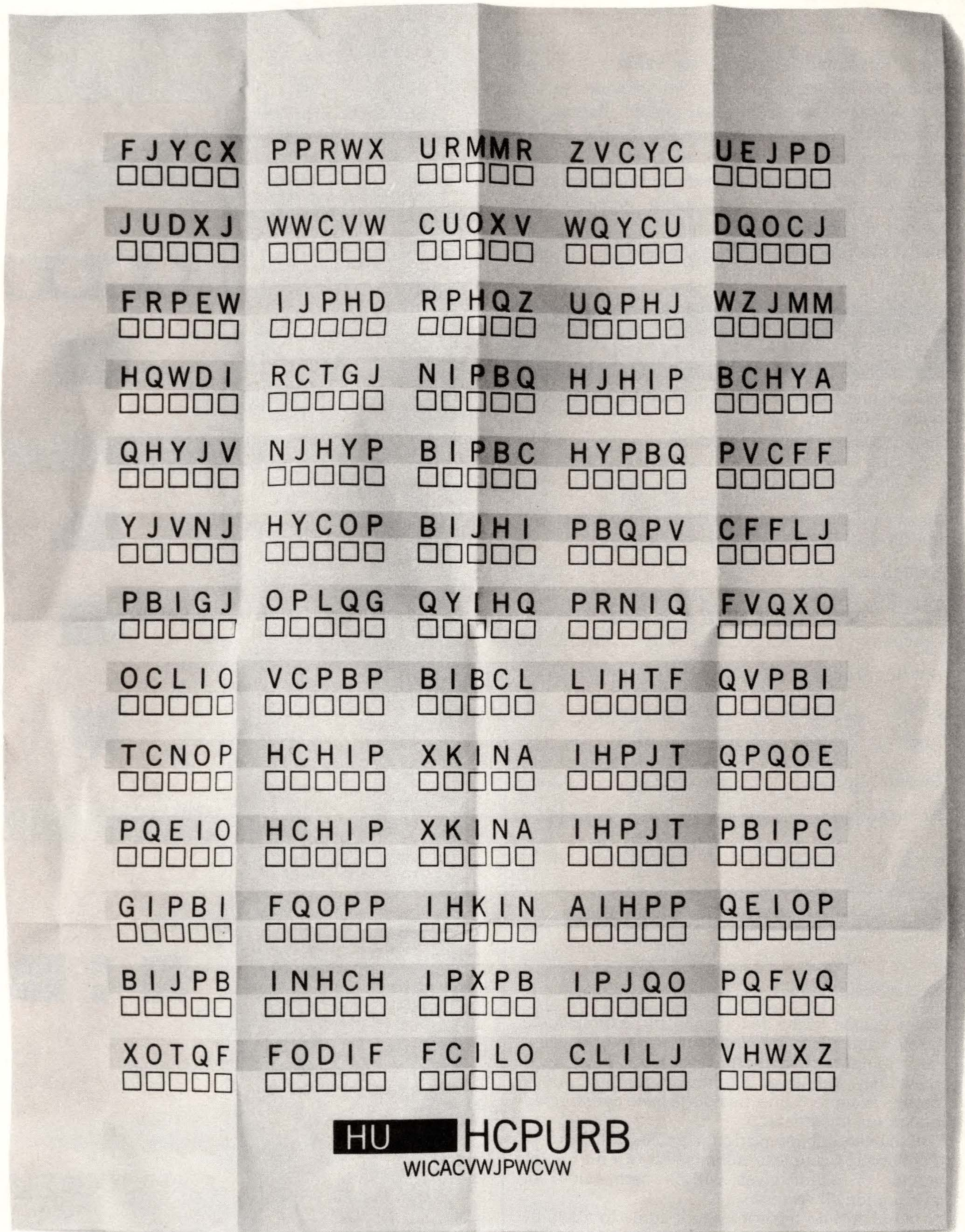

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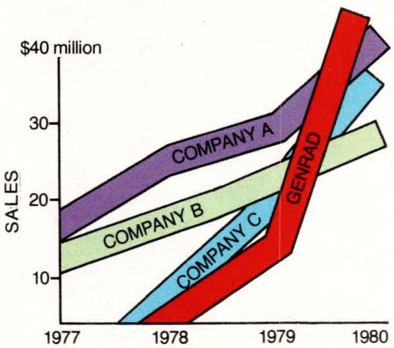

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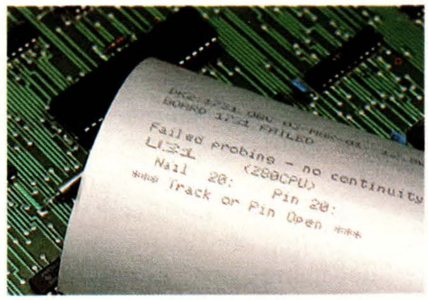

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*Source: Dataquest, Inc. 1981

CIRCLE NO 100

Lightweight 1200-baud terminal serves nontechnical users

Model 2300 interactive portable terminal, a high-speed device designed for cost-efficient interactive access to host computers from remote telephone locations, employs μP control to simplify its use by nontechnical personnel. It weighs 18½ lbs (including carrying case) and incorporates a high-speed (160 cps) bidirectional thermal printer that provides 120-cps throughput at 1200 baud.

The thin-film-head printer provides fully formed 5×9 dot-matrix characters with true ascenders and descenders and true overscore and underscore. It's key or code selectable for 80- or 132-column printing on 8.75-in.-wide thermal paper. A plotting option permits 512- or 1024-dots/line resolution.

Battery backup, multiple communications modes and portability *are the prime features of Model 2300 interactive terminal. Weighing 18.5 lbs, it incorporates an acoustic modem with switch-selectable data rates of 110 to 1200 baud and a 160-cps thermal printer.*

Nonvolatile memory

The unit's typewriter-style keyboard generates 96 printable characters with a full 128 ASCII character set and has six software-definable function keys for special applications. It works in tandem with the terminal's 2k bytes of nonvolatile memory (expandable to 4k), which, equipped with battery backup, permits field use and maintenance of key data without power.

In addition to the main RAM, memory space is available for 8k bytes of user-defined ROMable code for special applications.

Multiple data rates

To enhance the terminal's versatility and portability, a built-in switch-selectable 300/1200-baud acoustic coupler is provided. This Bell 103- and Vadic 3400-compatible unit can handle data rates from 110 to 1200 baud in full- or half-duplex originate-only modes. For hardwired communications employing the RS-232 interface, eight selectable speeds are available, ranging from 110 to 9600 baud. Typically, data configuration is 11 bits/character at 110 baud and 10 bits/character for other rates.

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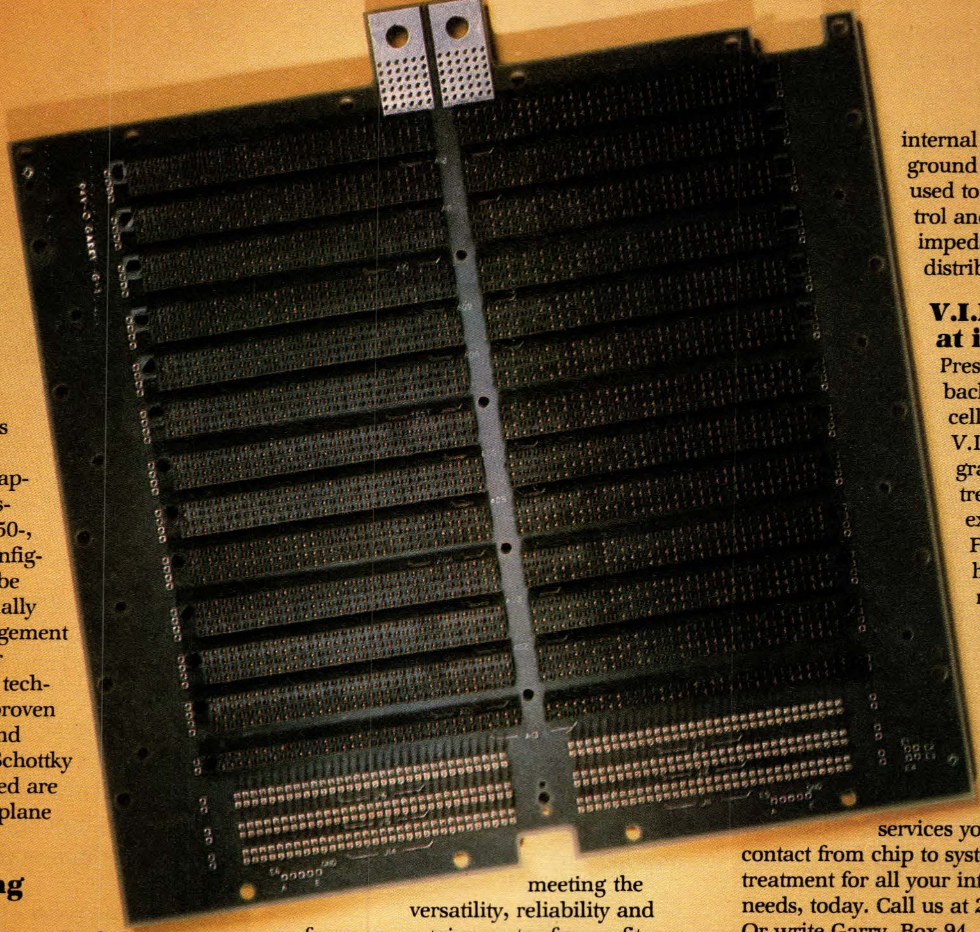

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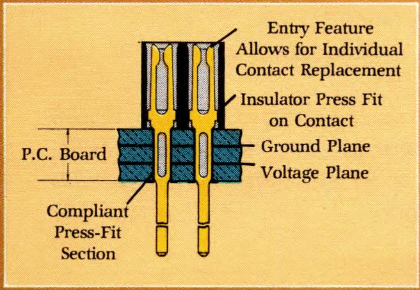
When you choose Garry backplanes built to MIL-C-28859A specifications, you know exactly what you'll get. The reliability and individual replacement versatility of gold-plated, press-fit compliant contacts designed to mate with hi-rel NAFI-type connectors. With all the performance criteria built into the MIL-C-28859A standard.

Technology is the answer

Up-to-date technology is the answer to meeting the versatility, reliability and performance requirements of press-fit, multi-layer backplane applications. Here's a sample of the technology Garry offers for your immediate use:



Press-Fit Compliant Contacts—Garry's compliant contact design provides broad contact area and constant contact tension for reliable electrical and mechanical press-fit performance. Beryllium copper (per QQ-C-533) construction, alloy 172 spring temper, gold plated per MIL-G-45204.

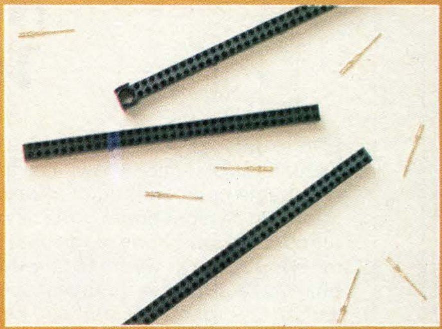
Snap-on Insulator Housings—Polyester material per MIL-M-24519 is molded into modular, snap-on housings with unique entry receptacles that allow for individual contact replacement. Bent or broken contacts can be replaced quickly and easily, even in the field.

Multi-layer Construction—Epoxy glass base laminate is custom manufactured into configurations from 2 to 10 layers, in accordance with MIL-P-55110. Multi-layer construction, manufactured with internal voltage and ground planes, can be used to provide the control and benefits of low impedance and high distributed capacitance.

V.I.P. treatment at its best

Press-fit, multi-layer backplanes are an excellent example of the V.I.P. (Vertical Integration Packaging) treatment you can expect from Garry. From individual hi-rel contacts, to molded sockets and headers, custom boards, multi-layer backplanes and automatic wire-wrapping*, Garry provides all the interconnection products and services you need to make contact from chip to system I/O. Get V.I.P. treatment for all your interconnection needs, today. Call us at 201-846-5280. Or write Garry, Box 94, North Brunswick, NJ 08902.

*Wire-Wrap is a Gardner-Denver trademark.



Garry

V.I.P. VERTICAL INTEGRATION PACKAGING

A Division of Brand-Rex Company

CIRCLE NO 101

Letter-quality dot-matrix printer generates raster graphics

For systems requiring rapid throughput for data processing and near-letter-quality printing for documentation, Model M-100 dot-matrix printer features 140-cps bidirectional-logic-seeking print speed. Its throughput specs at 56 lpm for 132 characters/line, 96 lpm for 72 characters/line and 145 lpm for 40 characters/line; paper slew rate equals 10 ips.

Printing 140 cps, *Model M-100 dot-matrix printer provides near-letter-quality output.*

True descenders

The printer creates characters in a 9×9 matrix by employing a 14-wire printhead assembly with its wires offset. The result? Near-letter-quality character representations: The head design permits true lowercase descenders as well as superscripts and subscripts.

Plotting option

A \$250 (200) plotting option takes advantage of the print wires' 0.16-in. dot diameter, producing a plotting dot density of 70 dots horizontal and 84 dots vertical per plot cell. It employs a raster-style technique that allows 1320 dots max per raster.

The 60-lb, 8×26.6×23.4-in. printer employs a full 128-character set (96 ASCII plus 32 commonly used international characters). Its full-sized carriage handles paper widths from 3 to 16 in. Paper can load from the front or bottom; rear loading is optional.

You can easily produce an original plus five copies. As in the manufacturer's other printers, a continuous-loop fabric ribbon cartridge is used.

Parallel interface standard

The standard configuration comes with an 8-bit parallel interface; RS-232C, current-loop and Centronics-compatible interfaces are optional, as is bar-code-generation capability. The printer requires 250W in operating mode, 125W in standby. Voltage requirements spec at 115V at 60 Hz or 110 to 240V at 50/60 Hz.

\$2200 (200). Delivery, 90 days ARO.

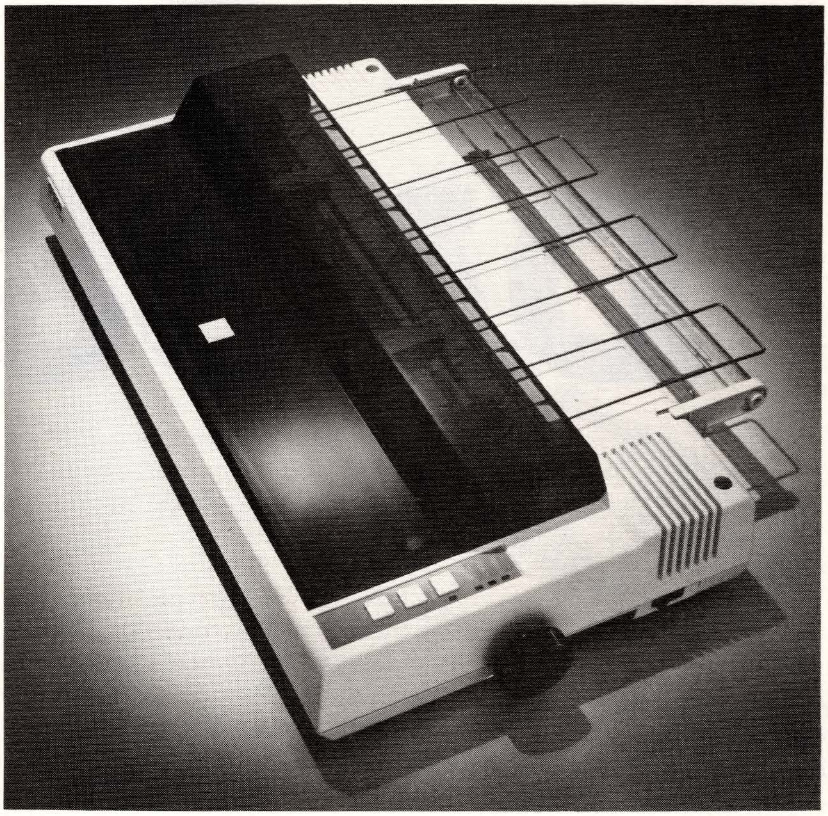
Dataproducts Corp, 6200 Canoga Ave, Woodland Hills, CA 91365. Phone (213) 887-8000. **Circle No 467**

High-resolution dot-matrix printer provides full-sized carriage

Another in the growing ranks of letter-quality dot-matrix printers, Model MX-100 features a full-sized carriage, permitting the use of paper as wide as 15½ in. and a print format of 136 columns.

The bidirectional 80-cps printer serves both data-processing and correspondence requirements, thanks to its selectable 9×9 or 9×18 (double width) character matrices. Additionally, you can emphasize characters with an 18×9 matrix or double emphasize them with an 18×18 matrix. (These emphasized modes also implement a double strike to provide additional highlighting.)

As an added feature, you can create several print sizes, including normal (10 cpi for 136 characters/line), normal expanded (5 cpi, 68 characters/line), compressed (16.5 cpi, 233 characters/line) and compressed expanded (8.25 cpi, 116 characters/line).



A full-sized carriage, *letter-quality printing and a $565 (1000) price tag are the prime features of the MX-100 dot-matrix printer.*

Graphics built in

Working in concert with the unit's basic text-printing features is a built-in graphics function—a unidirectional bit-range configuration that provides horizontal dot density of 60 dots/in. in Standard mode and 120 dots/in. in Double Density mode.

Like the manufacturer's MX-70 and MK-80 dot-matrix printers, the MX-100 employs a "throwaway" head assembly that costs less than $40 and exhibits a typical life expectancy of five million lines. It provides programmable line-feed length (1 to 85/72), programmable form-feed (to 127 lines), horizontal tab (to 12 positions), vertical tab (to eight positions) and programmable skip over perf for length and interval spacing.

The 21-lb, 5.2×23.3×12.5-in. printer requires 115V at 60 Hz and 1A. $565 (1000).

Epson America Inc, 23844 Hawthorne Blvd, Torrance, CA 90505. Phone (213) 378-2220.

Circle No 468

Your speed machines are here.
High speed, high performance Static RAMs.

For high speed mainframe, mini and micro memory applications, you can't beat the speed machines from Synertek.

There's a whole range of speeds available to meet your system needs. The SY2147 and SY2148 down to 55nsec. And the SY2149H down to 45nsec. For systems where speed is even more critical to performance, the SY2149H offers an enhanced Chip Select access time down to 20nsec.

The latest proven process technology—advanced high performance scaled N-channel MOS—is what makes these machines perform.

High Performance Selection Guide

Organization	Part Number	Speed	Operating Current (Max.)	Standby Current (Max.)
4Kx1	SY2147-3	55nsec	180mA	30mA
	SY2147L	70nsec	140mA	10mA
	SY2147	70nsec	160mA	20mA
	SY2147-6	85nsec	160mA	20mA
1Kx4	SY2148-3	55nsec	140mA	30mA
	SY2148	70nsec	140mA	30mA
	SY2148-6	85nsec	140mA	30mA
1Kx4	SY2149H-2	45nsec	150mA	*
	SY2149H-3	55nsec	150mA	*
	SY2149HL-3	55nsec	125mA	*
	SY2149H	70nsec	150mA	*
	SY2149HL	70nsec	125mA	*

*Not Applicable

To exactly meet your system requirements, Synertek's speed machines not only deliver the performance you need, they deliver flexible organization, too. The SY2148 and SY2149H are organized 1Kx4 with common data I/O. For deeper high speed memory applications, there's the SY2147—organized 4Kx1 with separate data I/O.

You also get a choice of Automatic Power Down, available in both the SY2147 and SY2148. That can mean system level power savings of up to 80 percent.

Standard features include total TTL compatibility on all inputs and outputs, single +5V power supply, and three-state outputs. All use fully static circuitry. So you get identical cycle and access times with no clocks or strobes required.

Put yourself in the winner's circle. With the speed machines from Synertek. Contact your nearest Synertek distributor or representative. or call Memory Product Marketing direct at (408) 988-5611.

Synertek is a major MOS supplier of high volume parts with advanced technologies and techniques behind everything we make. Static RAMs. ROMs. Custom circuits. Single-chip Microcomputers. Systems. 6500 Microprocessors and Peripherals.

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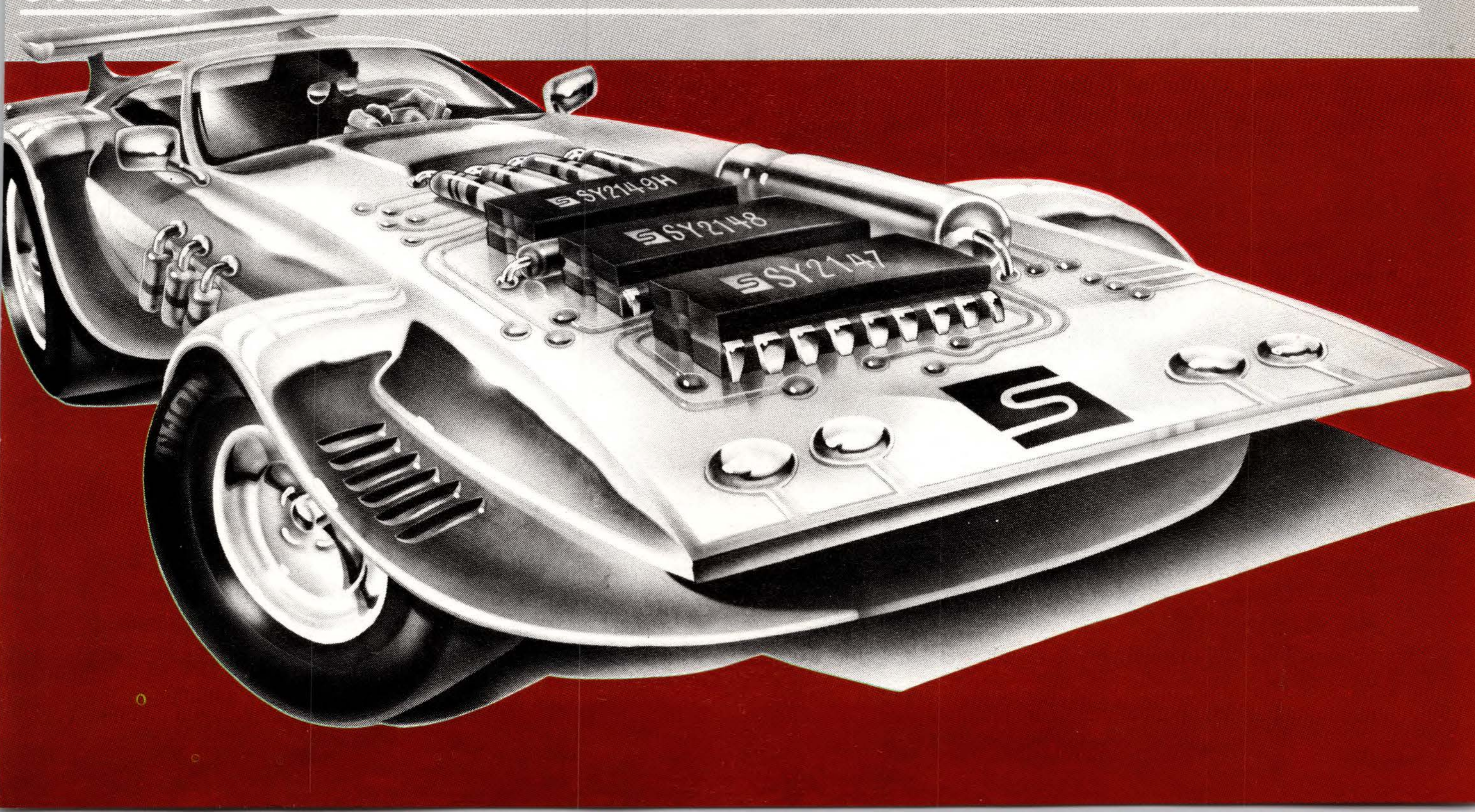
SY2147 55nsec

SY2148 55nsec

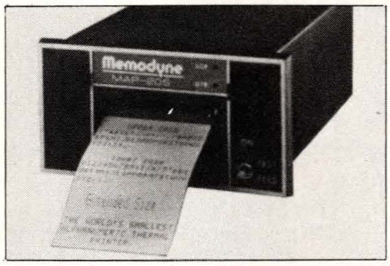
SY2149H 45nsec



Compact 20-column thermal printer packs multiple features in 95 in.^{3}

If your system packaging requirements restrict printer size and location, consider Model MAP-20S. This 20-column alphanumeric thermal printer occupies just 95 in.^{3} and weighs less than 4.2 lbs. But its small size doesn't shortchange you: It comes complete with μP-controlled timing, character-generation, printhead-drive and stepping-motor circuits, a UART and an ac power supply.

Fitting into a 4.5×2.78-in. panel area, the printer outputs the 96-character ASCII set of upper- and lower-case letters, numerals and punctuation. For normal-size characters, it runs at 115 lpm (240 lpm max).



Accepting 75- to 9600-baud inputs, *the compact and lightweight Model MAP-20S alphanumeric thermal printer outputs 96 upper- and lower-case ASCII characters over 20 columns at 115 lpm typ.*

The unit's internal logic allows a wide variety of user-programmable features—either data coded or pin selected—such as print direction, buffer mode, character size, form forward, vertical and horizontal tab, backspace, carriage return and line feed. Other features include end-of-paper sensing, internal self testing and optoisolation to guard against common-mode noise and ground-loop problems.

Accommodating 75- to 9600-baud serial input data rates, the printer provides both 20-mA current-loop and RS-232C interfaces. $725.

Memodyne Corp, 220 Reservoir St, Needham Heights, MA 02194. Phone (617) 444-7000.

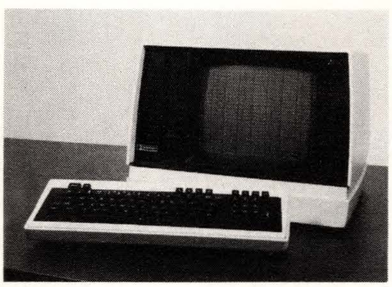
Circle No 469

DEC-compatible 15-in. CRT terminal provides a host of options

Model BT-100+ video display terminal employs a Z80 μP and is designed for operator convenience, providing such features as a detachable keyboard with clustered numeric keypad, a 15-in. nonglare screen with either P4 or P31 phosphor, audible key clicks (user selectable to signify either on or off) and seven LEDs for diagnostic aids and operator information.

Additionally, it employs an automatic monitor saver that shuts the display off after approximately 16 min of nonuse; a depression of any key or receipt of a character from the host computer then restores all data on the screen without change.

The 15-in.-diagonal screen displays a user-selectable 80×24 or 132×24 format. Other features include bidirectional smooth scrolling, split-screen capability, Setup mode, fixed and floating tabs, and composite video for auxiliary monitors.



With a 15-in.-diagonal screen, *Model BT-100+ video display terminal employs a Z80A μP and furnishes a detachable keyboard and selectable display formats of 80×24 or 132×24.*

True lower case

The terminal displays 96 ASCII plus 32 line-drawing and graphics characters in a 7×9 dot-matrix cell, with 2-dot descenders providing true lower-case characters and underlining. You can select reverse video and two intensity levels on a character-by-character basis.

Weighing 60 lbs and measuring 19.5×28×16 in., the terminal includes a serial asynchronous RS-232/current-loop interface that operates in full-duplex mode and supports data rates ranging from 50 to 19.2k baud. $1495 (500).

Braegen Corp, 3340 E La Palma Ave, Anaheim, CA 92806. Phone (714) 632-9600.

Circle No 470

Five goes into twenty-one perfectly. Synertek's 1791 Floppy Disk Controller.

We've made it simple for you. Synertek's 1791 Floppy Disk Controller. With a single +5V power supply.

By eliminating the −5V and +12V power supplies, we've not only simplified system design, we've reduced energy consumption as well.

That's the way we design all of our microprocessor and microprocessor peripherals. To make your job easier. To fit in with your needs. And lower your costs.

The single +5V supply heads a list of solid features we've designed into our SY1791 and SY6591. Like IBM 3740 and System 34 compatibility. Double-buffered data transfers. Single (FM) or double-density (MFM) recording formats. Plug compatibility with the WD1791-02. Accommodates both 5-inch and 8-inch floppies. And solid performance over the entire 0°C to 70°C range.

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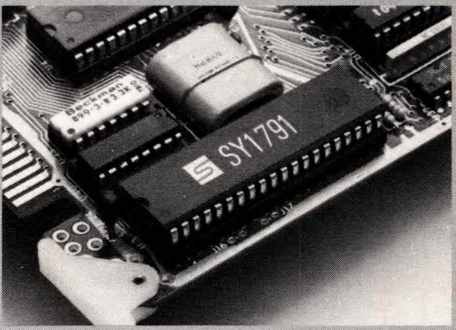

- SY1791-02 Inverted Data Bus
- SY1793-02 Non-inverted Data Bus
- SY6591 6500/6800 Bus compatible

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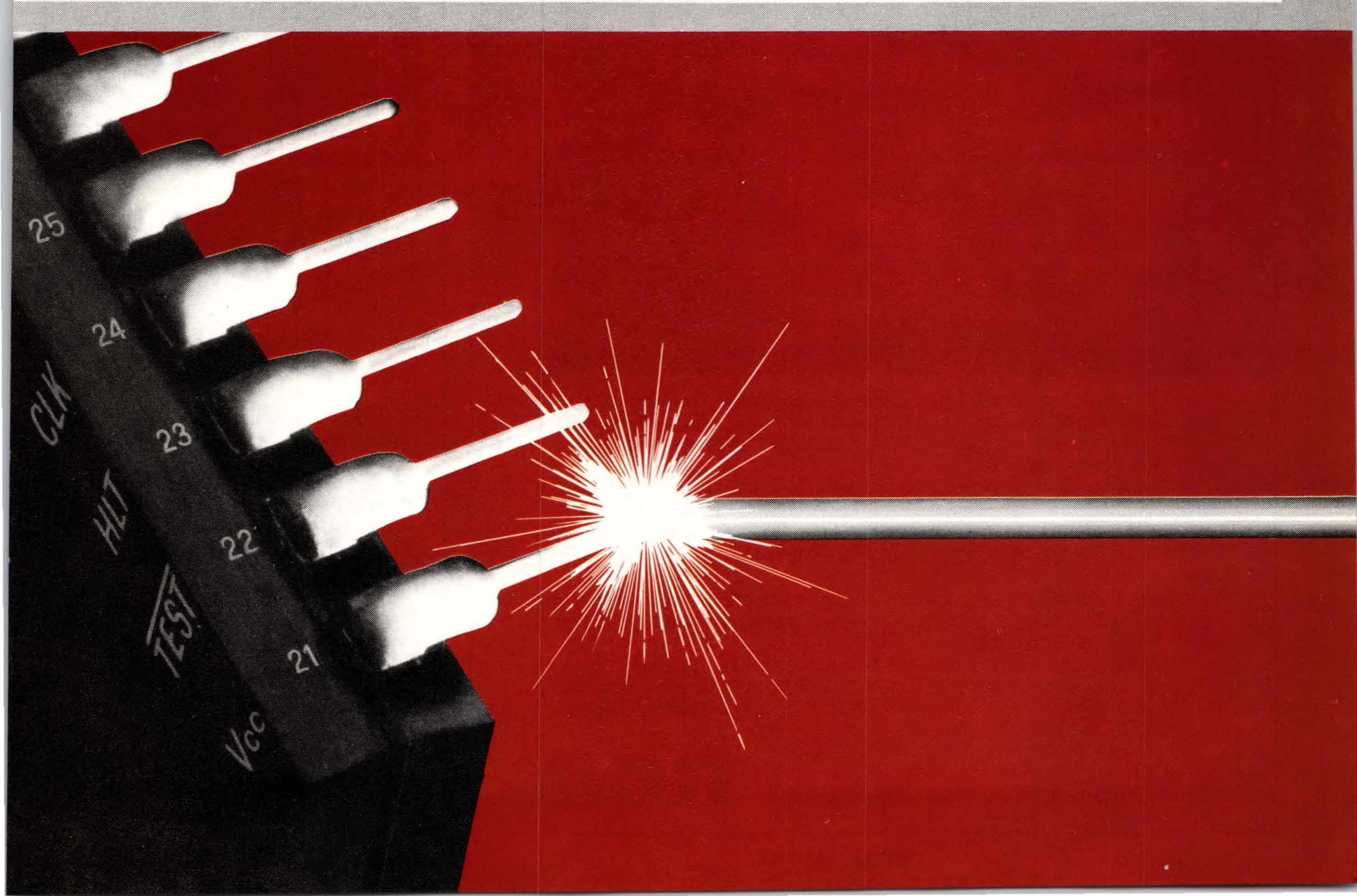
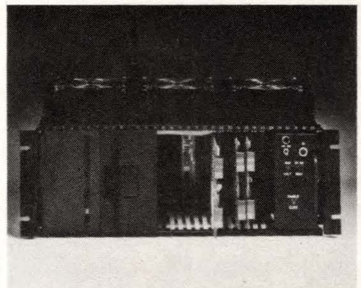
SY1791/93/6591 Single +5V Supply



New Products

COMPUTERS & PERIPHERALS



MICROCOMPUTER SYSTEM. The rack-mounting WCF-1 features an LSI-11/2 μP with 64k bytes of RAM or an LSI-11/23 with 256k of RAM, I/O interfaces with four RS-232 ports, controller, DMA capability, 5¼-in. Winchester disk drive and 5¼-in. floppy-disk drive, all with their respective power supplies. It provides a Q-bus prewired backplane and front-panel controls and indicator. Accommodating 12 dual-height cards, the system occupies 8¾ in. of a 19-in. rack and is expandable to accept additional floppies, Winchester drives or system cards by stacking individual system units. $8500 with LSI-11/2; $13,500 with LSI-11/23. Delivery, 60 days ARO. **North Atlantic Industries Inc,** 60 Plant Ave, Hauppauge, NY 11787. Phone (516) 582-6500.
Circle No 210

CROSS COMPILER. PasPort 8086 PASCAL cross compiler permits development and testing of 8086-μP software on PDP-11 minicomputers. Compatible with the 1980 International Standards Organization proposal for PASCAL, it operates with PDP-11s running under UNIX or RSX-11M operating systems. $15,000. **Intermetrics Inc,** 733 Concord Ave, Cambridge, MA 02138. Phone (617) 661-1840. TWX 710-320-7523. **Circle No 211**

HMOS technology from Synertek Custom. It's about time.

Whatever your needs in custom, ;ynertek is committed to meet them. Vith the latest technologies—HMOS ınd HCMOS—in addition to industry ;tandard NMOS silicon gate. So that ·ou don't have to compromise. Not ›n speed. Not on system size. Not on ;ost. Because your custom circuit ;hould be a masterpiece in every ;ense of the word.

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We offer you, the custom user, ıdvanced technologies that result n substantial benefits. Such as higher ;peeds—18 to 20 MHz, or greater vith HMOS. Plus faster microprocessor ;peeds. Faster control functions. And more complex functions on a minimized chip size, resulting in reduced part count and enhanced system efficiency. By offering you more capability in silicon, you get more from Synertek.

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HMOS. HCMOS. Or standard NMOS technology. A process for every masterpiece. A program for every need. It's about time someone did it. From the artisans of technology, Synertek Custom. Contact Custom Product Marketing at (408) 988-5600.

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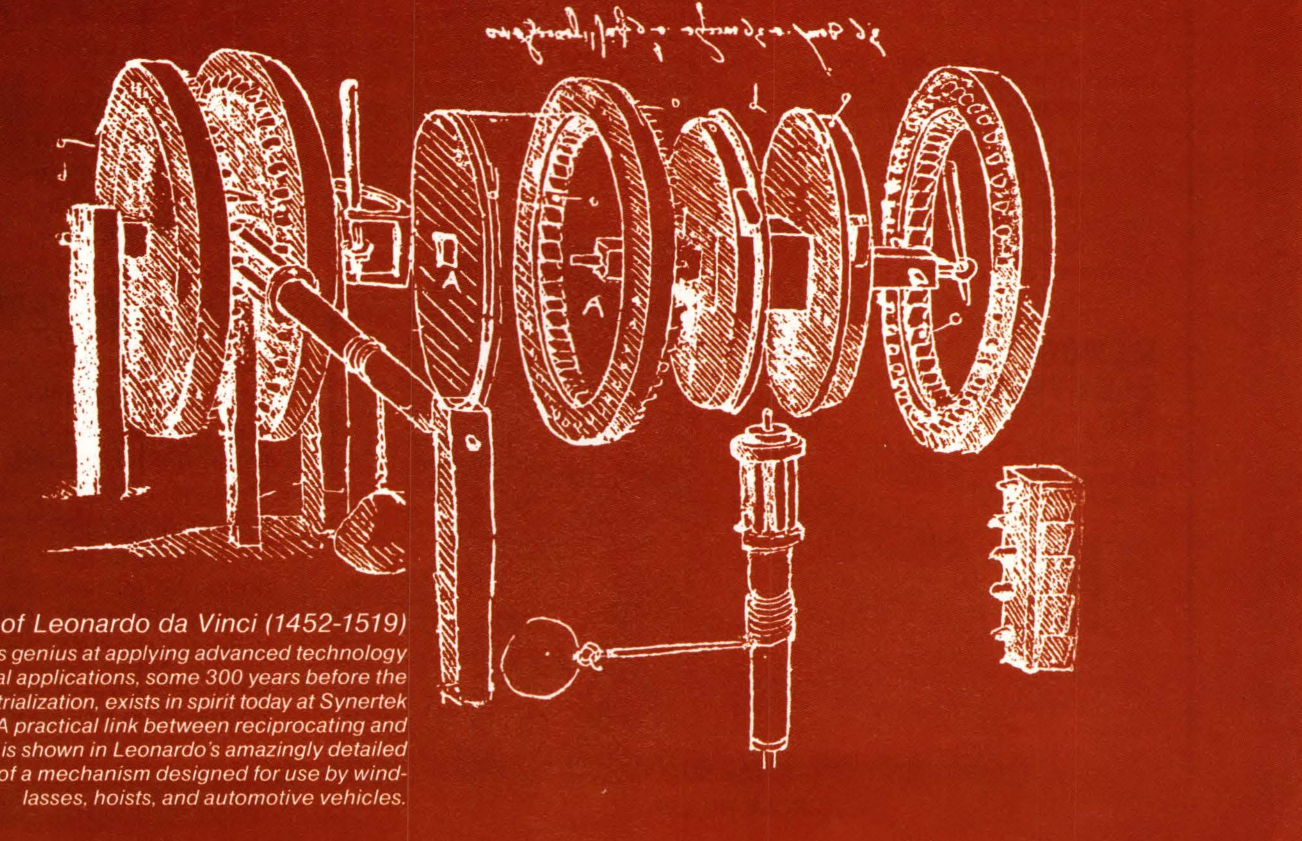
Artisans of Technology



A creation of Leonardo da Vinci (1452-1519)

Leonardo's genius at applying advanced technology to practical applications, some 300 years before the Age of Industrialization, exists in spirit today at Synertek Custom. A practical link between reciprocating and rotary motion is shown in Leonardo's amazingly detailed drawing of a mechanism designed for use by windlasses, hoists, and automotive vehicles.

New Products

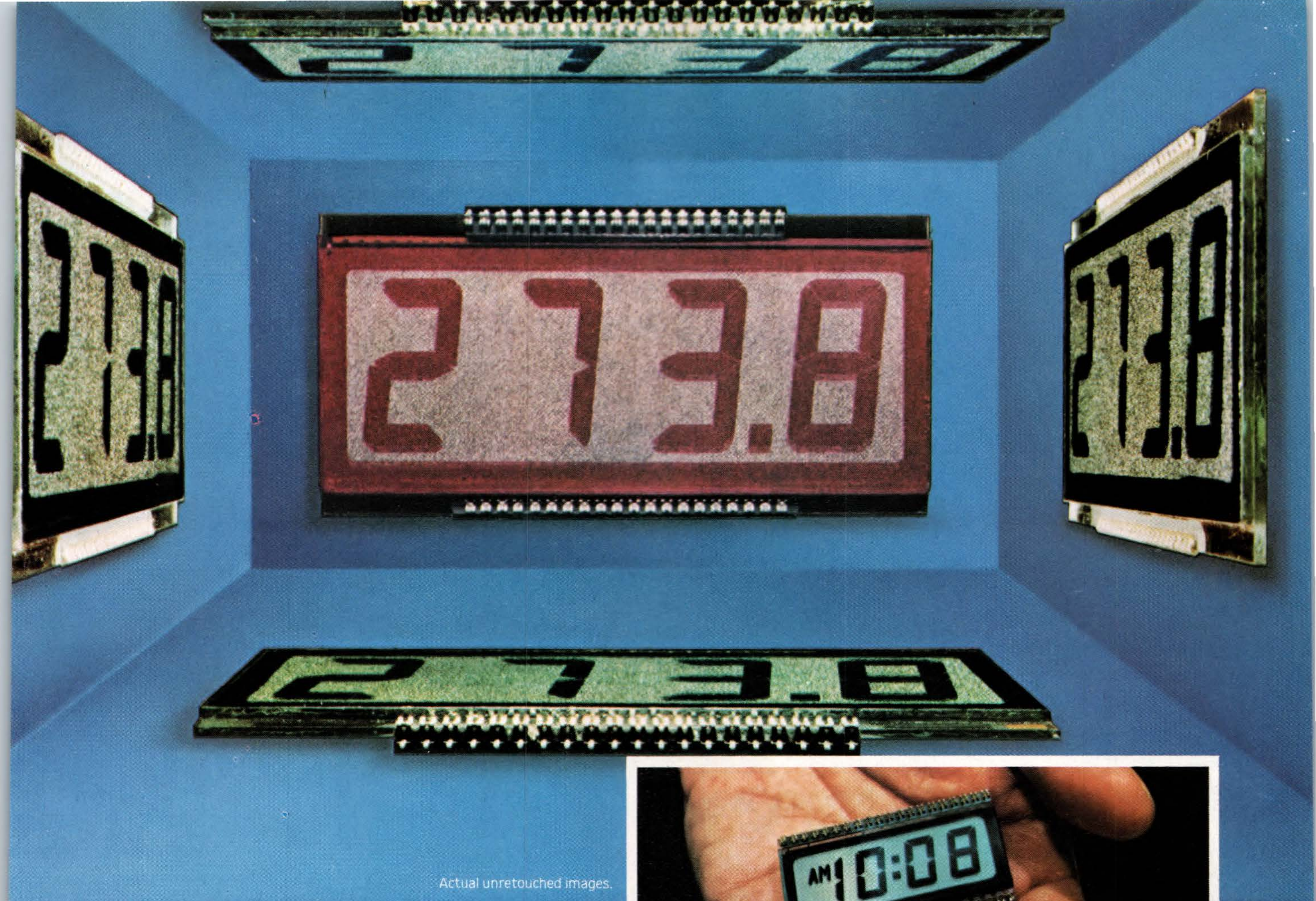
COMPUTERS & PERIPHERALS

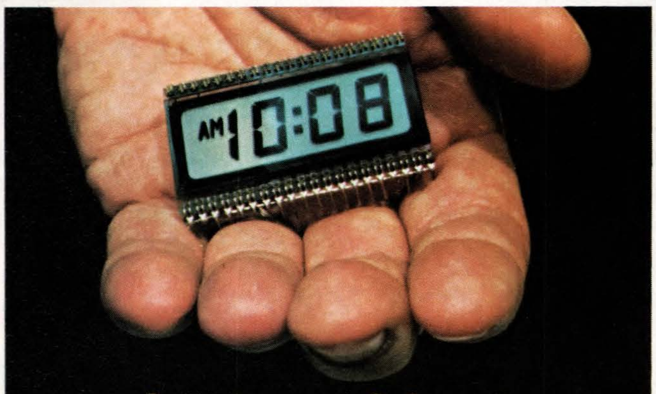
COLOR TERMINAL. For business-graphics applications, the high-resolution ColorScan 10 provides eight colors for foreground and background information and a graphics character set. A nonglare 12-in. screen presents 80- or 132-column×24-line displays. Also featured are a detachable typewriter-style keyboard with separate numeric pad; split-screen, regional- and smooth-scrolling capabilities; and double-high/wide characters. $3795. Delivery, 120 days ARO. **Datamedia Corp,** 7401 Central Hwy, Pennsauken, NJ 08109. Phone (609) 665-5400.

Circle No 212

DESKTOP PRINTER. Model SP110 features bidirectional 136-character/line dot-matrix printing at 90 cps, character-mode operation, 7×9 matrix with descenders and underlining and condensed and expanded fonts. Foreign-language character sets and programmable horizontal and vertical tabbing are also available. Utilizing the 96-character ASCII set and APL, the unit accepts both friction and pin-feed forms and can print with horizontal pitches of 10, 12½ and 16⅔ cpi. $900 (500). **Burroughs OEM Marketing,** Burroughs Pl, Detroit, MI 48232. Phone (313) 972-8031.

Circle No 213





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CIRCLE NO 105

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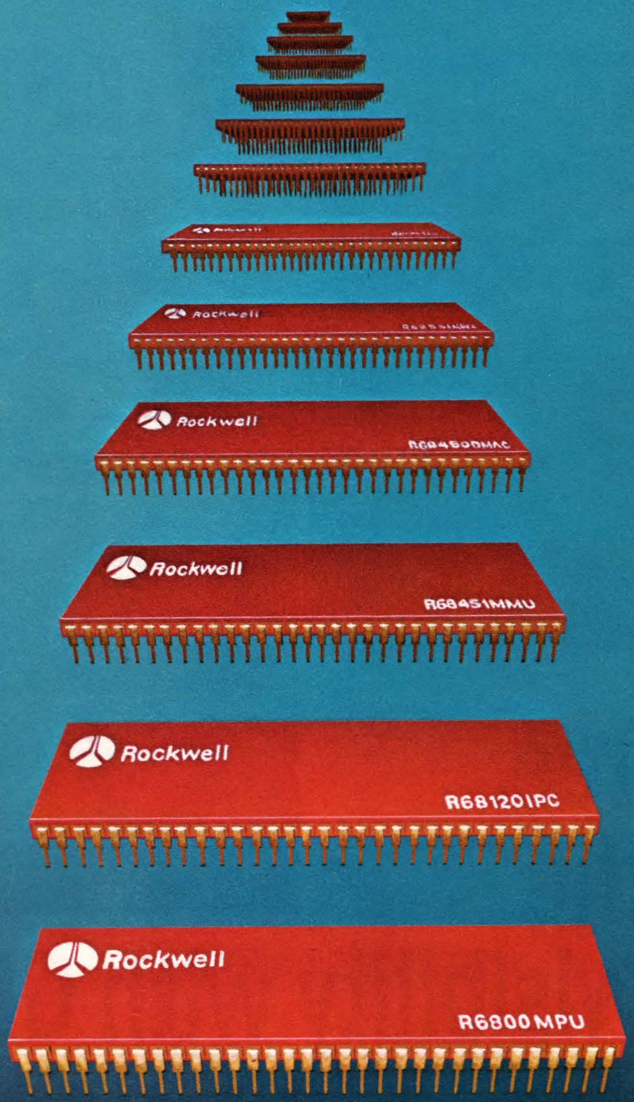

Choose Rockwell's family of 16-bit micros. You'll get the best in performance and versatility of the three popular 16s.

The Rockwell 16s are the number crunching champs. The R68000 is your best choice for computational performance.

And its versatility makes the R68000 the best choice for more applications than any other 16s.

Business computers. Intelligent peripherals. Communications. Process controls. Only the R68000 gives you powerful mass memory handling and architectural features designed to fit the broadest range of 16-bit needs.

Software development is a snap, compared to other 16s. There's powerful 16-megabyte addressing without the need for segmentation. It handles bytes and BCD nibbles. Has extended memory addressing.

The R68000 MPU is available now. The powerful 8-bit R6500 peripheral fam including a one-chip R650(specifically designed to b slave to the 16-bit master, e tends your system develc ment reach. And a host of 16- peripherals are on their w

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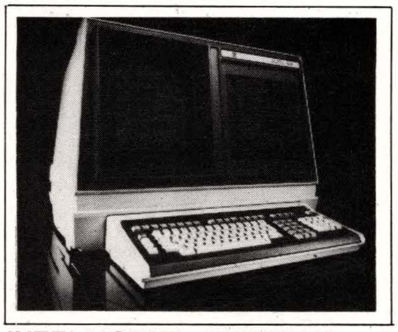
New Products

COMPUTERS & PERIPHERALS



INTELLIGENT TERMINAL. A 16-bit intelligent unit for word-processing and office-automation applications, the DataVue Model 1000 features an 8086 μC, CP/M 86 operating system, full-page 66×80-character video display, 64k bytes of RAM, 8k bytes of PROM and three RS-232C ports. Two double-sided, double-density floppy-disk drives with 1.2M bytes of storage are included. Any combination of 128 upper- and lower-case ASCII characters can be displayed in high or low intensity with blinking, reverse, blank and underline capability. The detachable keyboard provides a full alphanumeric set of 107 keys with n-key rollover and eight user-programmable function keys. $8654 (25) including word-processing applications software. **Piiceon Inc,** 2350 Bering Dr, San Jose, CA 95131. Phone (408) 946-8030.

Circle No 214

GRAPHICS GENERATOR. A 512×480-resolution intelligent stand-alone unit, Model RG-B1 accepts high-level display opcodes from a host computer to generate circles, ASCII characters (bold font and variable size), point-to-point drawings and rectangular fills on a standard 525-line TV monitor. Display opcodes are downloaded from the host to the RG-B1 and stored in its 2k RAM buffer; after loading, they are processed by the unit's 8085 processor to create graphics shapes, which are stored in its refresh memory. Data can be uploaded to or downloaded from the host computer in either binary or Intel hex format. A software monitor is provided for use at a keyboard when the unit is in Manual mode. $1450. **Raster Graphics,** Box 23334, Tigard, OR 97223. Phone (503) 620-2241.

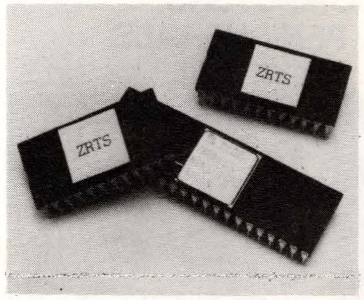
Circle No 215

DESKTOP COMPUTER. Model XP/3 sports a 5M-byte micro-Winchester hard-disk drive (170-msec average access time) plus a 900k-byte double-sided GCR mini-floppy drive for I/O and backup. It also provides a Z80 μP, 64k of RAM and a 1920-character 12-in.-diagonal CRT with antiglare amber screen, 10- to 9600-baud serial-communications channel and Centronics-compatible parallel printer interface. Options include two additional 5M-byte micro-Winchesters and a selection of dot-matrix and daisy-wheel printers. The system is supported by CP/M, with Microsoft BASIC (interpreter and compiler), FORTRAN and COBOL also available. A wide variety of business software packages are available. From $7200. **Commercial Computer Inc,** 7884 12th Ave South, Minneapolis, MN 55420. Phone (612) 854 2309.

Circle No 216

COMPUTERS & PERIPHERALS

SOFTWARE. ZRTS 8000 modular multitasking software permits customized operating systems for Z8001 (segmented) and Z8002 (nonsegmented) 16-bit CPUs. It consists of a real-time, multitasking executive program (the kernel) and a language processor (the system configurator). The kernel manages all major real-time functions, including task synchronization, priority scheduling, real-time clock control and interrupt handling; it requires 4k bytes of memory (in



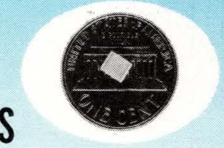
PROM or RAM) and executes on Z8001 and Z8002 development modules or on any Z8000-based target system with a real-time clock. The System Configurator supports a variety of target configurations via ZRTs configuration language. $3500 on diskette, including unlimited duplication rights. **Zilog Inc,** 10340 Bubb Rd, Cupertino, CA 95014. Phone (408) 446-4666.

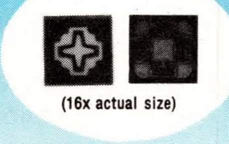
Circle No 217

DISK DRIVES. 8-in. Winchester-type units, drives in the D2200 Series feature 42.5M-bytes max storage, 30-msec access time and interface/format compatibility with SMD controllers. Model D2220 provides 25.5M-bytes capacity; Model D2230, 42.5M bytes. MTBF specs at >10,000 hrs; MTTR, <½hr. Two of the 5½×8½×16½-in. drives mount in one 19-in. rack. Model D2220, $2365; Model D2230, $2590 (100). Delivery, 60 days ARO. **NEC Information Systems Inc,** 5 Militia Dr, Lexington, MA 02173. Phone (617) 862-3120.

Circle No 218

CIRCLE NO 108





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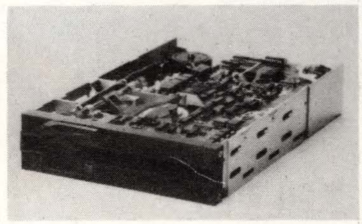
New Products

COMPUTERS & PERIPHERALS



FLOPPY-DISK DRIVES. Half the height of comparable drives, the 2.3-in.-high Thinline utilizes a dc brushless spindle motor, can be operated by interface-control signals and incorporates a double-sided head. Head positioning occurs through a band-driven carriage; track-to-track access time equals 3 msec, and the units record at 48 tpi (96 tpi with suitable media). Model TM 848-1 stores 0.6M bytes (double density, IBM formatted) on one side of a disk. Model TM 848-2 stores 1.2M bytes, utilizing both sides. $375 for double-sided unit. Delivery, 90 days ARO. **Tandon Corp,** 20320 Prairie St, Chatsworth, CA 91311. Phone (213) 993-6644. **Circle No 219**

LINE DRIVER. A multidrop synchronous multipoint unit, SLD-1 provides data transmission over unloaded twisted pairs at rates to 19.2k bps. Standard features include internal crystal-controlled oscillator; CMOS circuitry; scrambler; complete diagnostics, including status indicators displaying all operating conditions; and line and digital loopbacks. The rack-mounting version accommodates as many as 16 line drivers in one unit. Transmission rates are switch selectable from 1200 to 19.2k baud. $365. Delivery, 45 days ARO. **Tri-Communications Industries Inc,** 20 Fitch St, East Norwalk, CT 06885. Phone (203) 866-1154. **Circle No 220**

Maglatch TO-5. The world's smallest relay with indestructible memory.

Our little magnetic latching TO-5 relay simply never forgets. Once it's set with a short pulse of coil voltage, Teledyne's Maglatch TO-5 will retain its state until reset. Even if system power fails or is shut off.

Because holding power is not required, the Maglatch TO-5 uses less energy than any other relay you can buy. This makes it ideal for any situation where power drain is critical. And its tiny footprint makes it ideal for high density printed circuit boards.

For RF switching applications, the Maglatch's low intercontact capacitance and contact circuit losses provide high isolation and low insertion loss up through UHF.

The Maglatch TO-5 is available in SPDT and DPDT styles. And it comes in commercial/industrial versions as well as military versions qualified to "L," "M," and "P" levels of MIL-R-39016.

Teledyne is an industry leader. We have been for over twenty years. We've used our technical and manufacturing know-how to create the world's best subminiature electromechanical and solid state relays.

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Program out a Integrated

Signetics' new IFL Series 20 maximizes design flexibility, lowers power dissipation, and cuts parts count.

Integrated Fuse Logic is Signetics' answer to TTL logic replacement. With our versatile IFL family, you can turn almost any logic design into hardware with just a handful of programmable parts. You'll save design time, reduce inventory, and improve system performance in the process.

Our new IFL Series 20 packs superior performance into 20-pin, PAL®-compatible DIPs. Besides offering I/O structures and AND arrays that are fully programmable, the IFL Series 20 gives you unique features that maximize both design flexibility and cost effectiveness with only three standard architectures: FPGA, FPLA, and FPLS.

® PAL is a registered trademark of Monolithic Memories Inc.

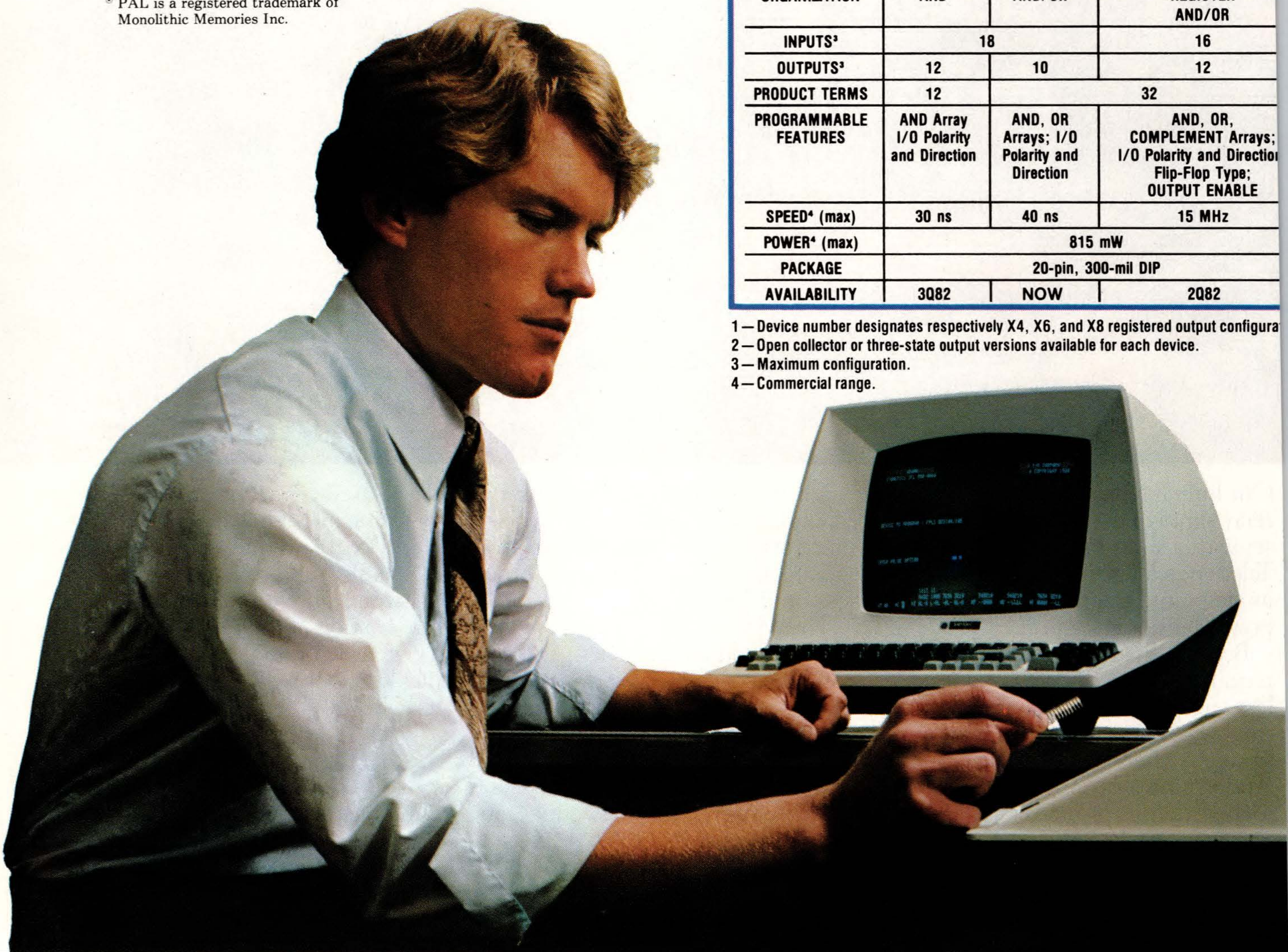
For starters, each IFL Series 20 device uses 81 milliwatts, maximum. That's 30% less power at th same speed than comparable field programmab elements. Lower power means greater reliability.

And thanks to open collector output options, IF Series 20 lets you synthesize functions with great complexity and faster switching speeds.

Series 20 

	FPGA	FPLA	FPLS[1]
DEVICE[2]	82S150/151	82S152/153	82S154/155 82S156/157 82S158/159
ORGANIZATION	AND	AND/OR	REGISTER AND/OR
INPUTS[3]	18		16
OUTPUTS[3]	12	10	12
PRODUCT TERMS	12	32	
PROGRAMMABLE FEATURES	AND Array I/O Polarity and Direction	AND, OR Arrays; I/O Polarity and Direction	AND, OR, COMPLEMENT Arrays; I/O Polarity and Directio Flip-Flop Type; OUTPUT ENABLE
SPEED[4] (max)	30 ns	40 ns	15 MHz
POWER[4] (max)	815 mW		
PACKAGE	20-pin, 300-mil DIP		
AVAILABILITY	3Q82	NOW	2Q82

1 — Device number designates respectively X4, X6, and X8 registered output configura
2 — Open collector or three-state output versions available for each device.
3 — Maximum configuration.
4 — Commercial range.



lot of TTL with Fuse Logic.

You also get programmable output polarities to iminate the need for external parts. Because each 'L device lets you program both active high and :tive low outputs.

With the IFL Series 20 logic array (FPLA) and gic sequencer (FPLS), you'll achieve higher speeds id greater logic density via programmable "OR"

Series 28 

FPGA	FPLA	FPRP	FPLS
2S102/103	82S100/101	82S106/107	82S104/105
AND	AND/OR		REGISTER AND/OR
16			
9	8		
9	48		
AND Array /O Polarity	AND, OR Arrays; I/O Polarity	AND, OR Arrays; INPUT Polarity	AND, OR, COMPLEMENT Arrays; INPUT Polarity
35 ns	50 ns	70 ns	11 MHz
895 mW			945 mW
28-pin, 600-mil DIP			
NOW			

rrays. These allow you to "edit" logic functions even fter delivery of systems to the field by just eprogramming spare gates.

Moreover, the Series 20 FPLS allows you to:

• Save I/O pins and minimize AND gates with on-:hip complement array.

• Optimize AND gate allocation in counting, shift-ng, and data buffering applications with program-nable J/K, D, or T flip-flop options.

• Save AND gates and free package pins for con-:rol functions with bi-directional flip-flops that can iandle I/O bus data, or convert to direct input mode.

• Use synchronous clocking together with asyn-:hronous flip-flop preset and clear for clock override or initialize functions.

• Gain additional programming capabilities—including Boolean equation entry with standard programmers.

Programming the IFL family is simple. Many standard PROM programmers selectively open fusible links on our IFL parts. Intact fuses couple all logic blocks for the desired function.

IFL Series 20 now complements our field-proven IFL Series 28, specially designed for high-end applications demanding greater I/O capability.

Find out how you can program flexibility into your next logic design with IFL Series 20, Series 28—or a *combination of both.* Write us today. Or contact your nearby Signetics sales office or authorized distributor.

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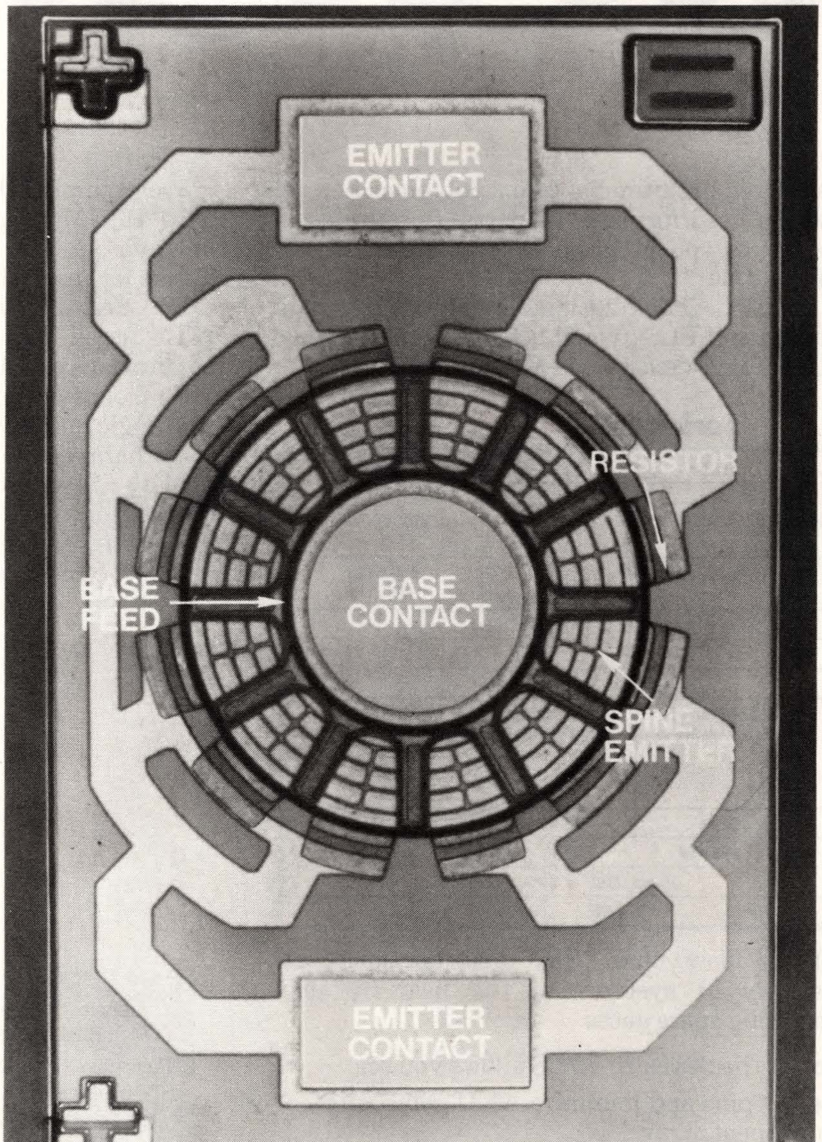
UHF transistor's innovative chip design yields high performance at low cost

Specifically designed for use as a low-power (0.5W) driver and as the output stages in mobile and MATV/CATV designs, the MRF559 RF transistor is fully characterized from 400 to 950 MHz. In addition, complete S parameters are spec'd for several I_C/V_{CE} combinations spanning 250 MHz to 1.5 GHz.

Low-voltage operation is the keystone of this device's performance versatility. At V_{CC}=12.5V dc, f_{OUT}=870 MHz and P_{OUT}=0.5W, power gain specs at 9.5 dB typ and collector efficiency equals 65% typ. Dropping V_{CC} to 7.5V dc (without changing f_{OUT} and P_{OUT}) reduces typical power gain to 6.5 dB but raises the collector's efficiency to 70% typ.

The 512-MHz specs are impressive, too. Holding to the 7.5V dc/0.5W levels, the device's typical power gain and collector efficiency spec at 10 dB and 65%, respectively.

Much of this RF transistor's performance results from the chip's geometry. Its unusual radially placed overlay architecture combines a distributed metal feed structure with emitter-ballasting resistors to assure equal operating currents throughout the junction.



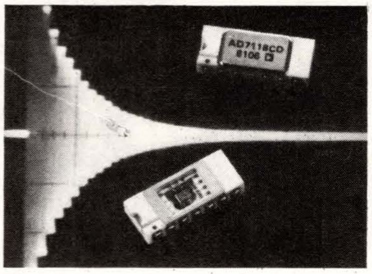
A radial chip geometry *allows the MRF559 RF transistor to achieve high performance and reliability at low cost. When operating at 7.5V dc and 870 MHz, it can deliver 0.5W output power with power gain of 6.5 dB and collector efficiency of 70%.*

In a 4-radial-leaded, 0.2-in.-diameter plastic package, the MRF559 costs $1.80 (100).

***Motorola Semiconductor Products Inc, Box 20912, Phoenix, AZ 85036. Phone (602) 244-6394.* Circle No 463**

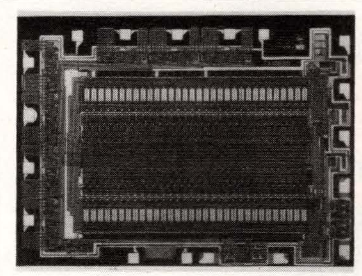
New Products

ICs & SEMI-CONDUCTORS

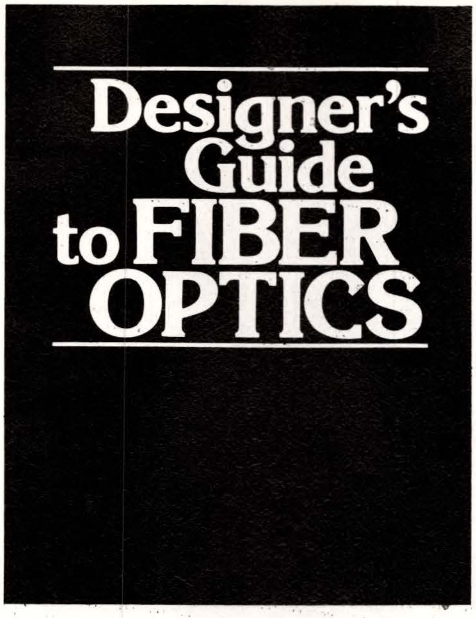


CMOS DAC. The monolithic LogDac AD7118 provides 0 to 85.5-dB attenuation in 1.5-dB steps under control of a 6-bit digital input code, plus guaranteed monotonic performance. Typical total harmonic distortion equals −85 dB; intermodulation distortion, −79 dB. Drawing as little as 2.5 mW from a 5 to 15V power supply, the part features an antilogarithmic transfer function and feedthrough at 1 kHz guaranteed at −86 dB max for L, C and U grades and −80 dB max for grades K, B and T. Operating frequency ranges from dc to 250 kHz typ with output noise limited to 70 nV/$\sqrt{\text{Hz}}$ max when used with a low-noise output amplifier. From $7.95 in plastic; $10 (100) in ceramic. **Analog Devices Semiconductor,** 804 Woburn St, Wilmington, MA 01887. Phone (617) 329-4700. **Circle No 224**

FLASH A/D CONVERTER. A CMOS video-speed unit, Model CA3300 furnishes sampling rates to 15 MHz (66-nsec conversion time) with power consumption <200 mW. Operating from a 3 to 12V dc supply, it produces a 6-bit latched 3-state output with an overflow bit and



two Chip Enables at an accuracy within ±0.5 LSB. For a 5V supply at a clock-generated sampling frequency of 11 MHz, power dissipation specs at ≤50 mW. Connecting two units in series produces a 7-bit high-speed converter. Operating two devices in parallel increases the sampling rate from 15 to 30 MHz. $38 for packaged units; $22 (1000) for chips. **RCA Solid State Div,** Box 3200, Somerville, NJ 08876. Phone (201) 685-6423. **Circle No 225**



A Designer's Guide to FIBER OPTICS

This comprehensive, authoritative guide covers all aspects of fiber-optic systems. Totalling 60 pages, it provides full understanding of the components, their key parameters and how they relate to fiber-optic system design.

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- **Part 2** — Matching sources and detectors to the fibers
- **Part 3** — System-design considerations
- **Part 4** — Building a fiber-optic system
- **Part 5** — What's available today: Fibers, connectors, sources and detectors

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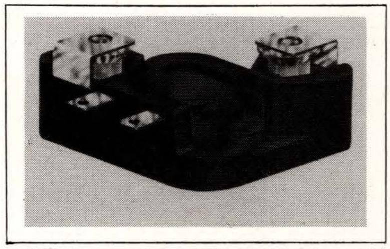
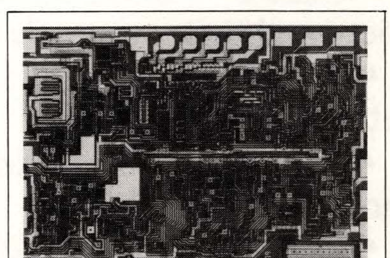
New Products

ICs & SEMI-CONDUCTORS



POWER TRANSISTORS. MJ 10050, -10100 and -10200 npn Darlingtons operate at collector currents of 50, 100 and 200A, have V_{CEO} ratings of 850, 450 and 250V, respectively, and can dissipate 500W. For 6-step ac-motor-speed/torque-control and low-frequency-inverter applications, they come in a "user-designed package" that features single-sided mounting with isolated mounting holes, busable terminals (¼-in. bolt with captured nut), separate drive terminals (¼-in. fast-on terminals), extra-large heat-sink contact area and a hybrid freewheeling diode. Operating from 120, 220 and 440V lines, the units have key parameters specified at elevated temperatures. $30.60 (100). **Motorola Semiconductor Products Inc,** Box 20912, Phoenix, AZ 85036. Phone (602) 244-4911.

Circle No 226



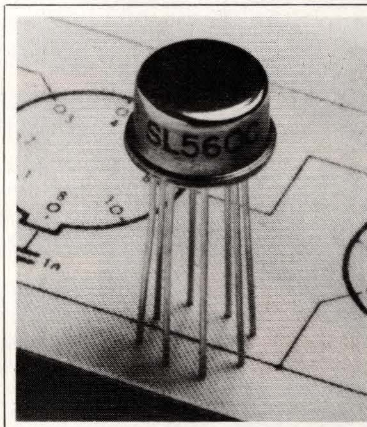
POWER CONTROL. Monitoring, controlling and regulating a power-supply system, Am6300 features a 2.5V±1% temperature-compensated reference, 100-mA 2.5 to 37.5V output for

New Products

ICs & SEMICONDUCTORS

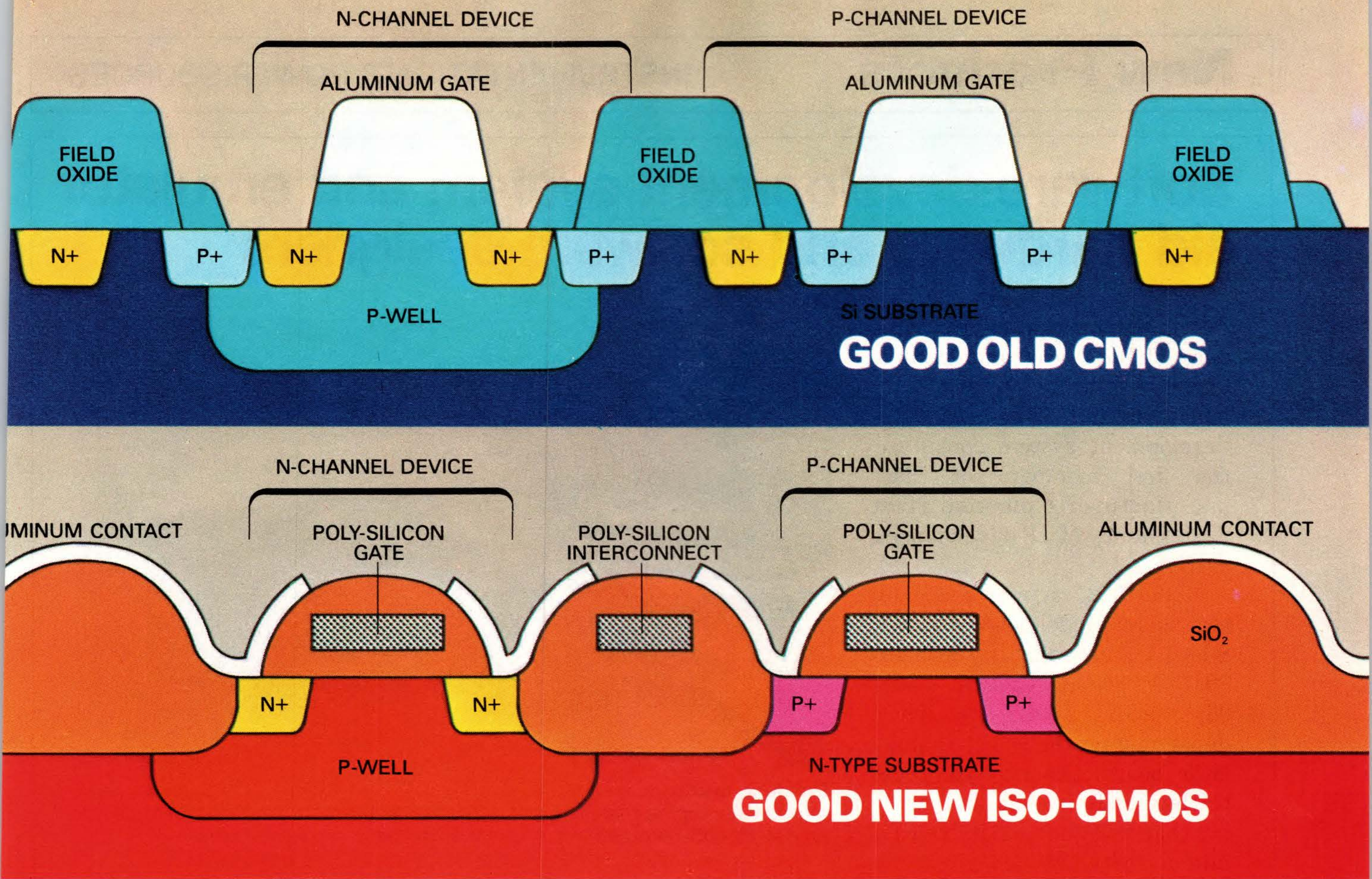
driving external power transistors, logic-control power-up enable for supply sequencing, and independent over/undervoltage and current-limiting shutdown circuits. Programmable functions include delays and rise-time control of the power supply's output as well as delays for overvoltage and current-limiting shutdown. Line regulation equals 0.02%; load regulation, 0.01%. Operating in either Local or Remote mode using TTL control inputs, the IC also furnishes internal thermal shutdown. From $5 (100). **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086. Phone (408) 732-2400.

Circle No 227



AMPLIFIER. A general-purpose 300-MHz integrated gain block, Model SL 560C low-noise amplifier provides signal gains to 40 dB and noise figures of <2 dB and accommodates 2 to 15V dc supply voltages. Integrating three closely matched npn transistors and all passive components required for load-line biasing and temperature compensation, it furnishes small-signal voltage gains flat to within±1.5 dB from 10 to 220 MHz with the 3-dB point at 250 MHz. Other features include bonded-out circuit nodes, transistor transition frequency (f_t) ≥1000 MHz and use of common-base or -emitter input transistor. $5.98 in TO-5 can; $2.58 (100) in 8-pin DIP. **Plessey Semiconductors,** 1641 Kaiser Ave, Irvine, CA 92714. Phone (714) 540-9979.

Circle No 228



When you talk leading edge, you're talking ISO-CMOS technology. And GTE Microcircuits.

So long, sapphire. Once, when you looked for speed, you looked anywhere but CMOS. Then, along came sapphire, and zing went the speed. And, zing went the price. What you gained in reduced power, fewer components, and overall system cost, you paid back with sapphire. Enter ISO-CMOS. Isolated Metal Oxide Semiconductor technology.

High speed. Low Power. ISO-CMOS uses N-type substrate in a planar bulk silicon process. To achieve maximum speed-to-power, ISO-CMOS utilizes silicon dioxide to isolate transistors. (Standard CMOS uses reverse-biased pn junctions.) The result is CMOS with an area-per-junction of P-MOS or N-MOS, the advantages of low-power CMOS and speeds approaching low-power Schottky and TTL. With typical power dissipation of 15mW.

Analog to digital. Same chip. If your application calls for digital control of analog information, look to GTE Microcircuits for answers. After all, who would know more about telecommunications than GTE.

A whole family of circuits. Between now and 1982, we'll bring out over 30 circuits in ISO-CMOS. All, single +5V supply. Si-gate circuits that give you the noise immunity and quiescent power dissipation of CMOS... and speeds of Schottky TTL.

Keep a sharp eye. During the third quarter of 1981, watch for our DTMF decoders and a line of Shottky TTL circuits pin-to-pin compatible with anybody's 74LS. Fourth quarter, an 8-bit microprocessor (68SC02), a 16K ROM (23SC16), or our new industry standard 2114, in CMOS. Standby power: 100 μA. First quarter '82, more logic circuits: a voltage translator, LCD drivers, and a family or Uncommitted Logic Arrays with up to 1,500 gates.

We'll be where you are. At a hundred GTE Microcircuits distributor locations worldwide. As they're introduced, our new ISO-CMOS chips will be right on your distributor's shelf. Along side our 2K, 4K and 8K RAMs. But you'll still call us for 16K, 32K, and 64K ROMs.

More on the way. Telecommunications. Logic. Memory. All in ISO-CMOS. Many, pin-to-pin compatible with the power hungry circuits you're using now. Plus, a 16K static RAM, and a 128K ROM. For a preview, ask for our new ISO-CMOS Short Form Catalog. Then, call your local GTE distributor for price and delivery.

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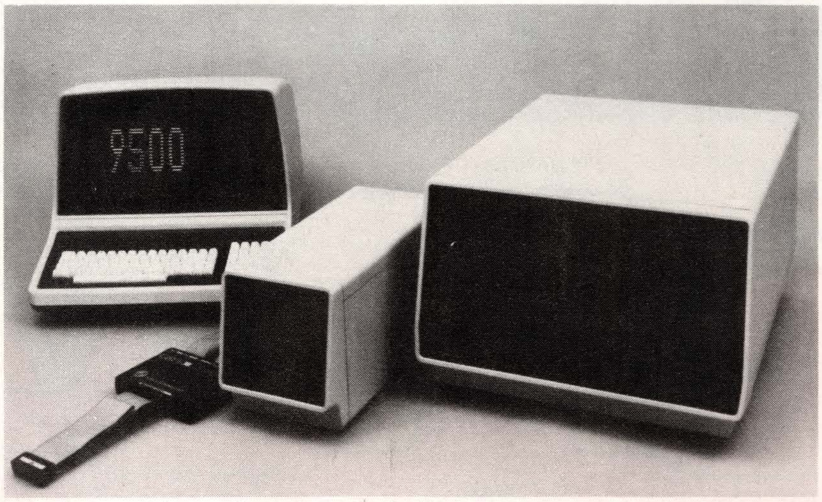
Software-development system and emulator aid hardware and software designers

Providing multiprocessor support for both programmers and design engineers, Models 9508 emulator and 9520 software-development system constitute the first members of their manufacturer's planned 9500 Series family of μP development systems.

Model 9520 supports one or two users; Model 9508 emulates 8-bit μPs, including the 8048/49, 8021/41, 8080A, 6800/02, 6801/03, 8085A, Z80A and 6809, depending on the selected emulator board. Planned additions to the family include an emulator that will support 16-bit μPs and a software-development system that will accommodate eight users via the UNIX operating system.



The first members *of a planned μP-development-system family, Model 9520 software-development system and Model 9508 emulator provide multiprocessor support for both hardware and software designers.*

Add 48k bytes to 64k

Model 9520 comes with a 64k-byte memory; you can specify an additional 48k bytes to enhance the instrument's multitasking capability—such as the simultaneous performance of text editing on one file, assembly of another and printing of yet a third. Two dual-density floppy-disk drives provide 1M bytes of on-line storage.

Other features include three RS-232, one RS-422 and one IEEE-488 ports. Macro assemblers generate programs for 8080, 8085A, Z80A, 6800, 6801 and 6802 μPs as well as the 8049 family, and the manufacturer plans to support other processors including the Z8000 and 8086. Planned for release this summer are PASCAL compilers for object-code generation for 8080, Z80, 8085, Z8000 and 8086 μPs.

Emulator frees host

You can download programs developed on Model 9520 to Model 9508 via an RS-232 port. (When available, the 16-bit emulator will accept downloaded programs via the IEEE-488 port.) Model 9508 operates in a stand-alone mode, so it makes no demands on its host computer except during uploading and downloading of programs. It comes with 8k of static RAM (an additional 8k is optional).

You can map this emulation memory anywhere in the target μP's address space, reducing the need for hardware prototypes during software development. To further reduce the hardware dependency of software debugging, Model 9508 can operate on either an internal or external clock.

Model 9508's 25 commands allow you to examine or change any memory location or μP register or fill or relocate large portions of memory. Four breakpoint types enhance the emulator's software-debugging capabilities: A hardware breakpoint works on instruction addresses; two complex breakpoints let you specify address-bus, data-bus and bus-cycle status and as many as eight external-logic-signal conditions; a fourth breakpoint triggers on target-μP register contents. You can specify a pass count of as many as 65,535 events or a delay of 65,535 counts.

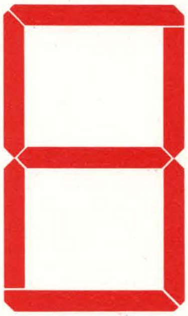
Other features include real-time trace and a software trace that indicates disassembled instructions and register contents.

Model 9520, $7495. Model 9508, $4995. Emulator boards, from $1975. Delivery, 45 days ARO.

Millennium Systems Inc, 19050 Pruneridge Ave, Cupertino, CA 95014. Phone (408) 996-9109. **Circle No 452**

A DRIVER EDUCATION COURSE FOR DESIGNERS USING LARGE AND BRIGHT DISPLAYS.

Today's bigger, brighter displays need high voltage drivers.



Are you designing a medical instrument that must catch the eye of a busy nurse from across a hospital ward? Or a critical cockpit readout that pilots must read in direct sunlight? Or a control panel for a nuclear power plant where one display must out-shine all others? Or perhaps a digital scale, taxi meter, cash register or gas pump?

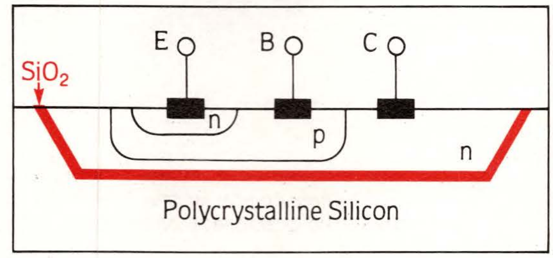
If you are one of the growing number of engineers facing these challenges, it's time you got to know a company named Dionics; and learned more about our monolithic high voltage drivers. They are the most reliable, straightforward way to take a TTL or MOS signal and drive a large and/or bright display.

Dionics: high voltage and high reliability.
Dionics has sold literally millions of high voltage drivers for every kind of display: gas or plasma discharge, vacuum fluorescent and electroluminescent up to 3 inches high. They drive digital and alphanumeric readouts, dot matrix panels, bar graph displays and more, with voltages to 280V. And they have earned the highest praise for quality and dependability from the industry's leading manufacturers.

The trouble with junction isolation.
Other manufacturers attempt to use a conventional technique called junction isolation to make their drivers. This method — while quite simple and relatively inexpensive — has an unavoidable shortcoming. As voltages approach 100V, the isolation between separated components begins to break down.

There are possible solutions to this problem, but they are all less than ideal. They tend to be technically or economically impractical at the manufacturing level. And at the design and application level, they clutter up board layouts, run up assembly costs and double or triple the chances of a component failure.

Dionics' bright idea: dielectric isolation.
At Dionics, we manufacture our high voltage drivers using a technique called

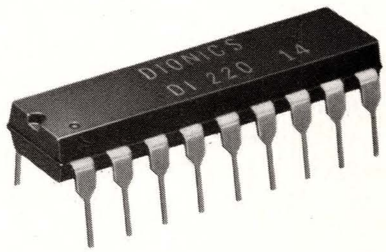


dielectric isolation. The various components within the monolithic circuit are isolated from each other in silicon dioxide (SiO_2); a form of quartz with all the electrical insulating properties of glass. You can use much higher voltage levels and eliminate the potential failure points created by the second "P" level found in junction isolation.

With dielectric isolation, circuit design proceeds as with totally discrete devices. There is no worry about interaction between components.

The breakdown voltage with dielectric isolation is typically greater than 500V. So designs, even those requiring outputs above 250V, remain simple, uncluttered, elegant. Lower parts counts, reduced production costs and dramatically improved reliability result.

Dionics drivers pay for themselves.
The advantages of Dionics high voltage



drivers do not come free. Manufacturing with dielectric isolation does cost a bit more than conventional techniques.

But consider the advantages of a clean, simple design — and the cost of even one service call to track down and replace a failed driver — and the conclusion is inescapable. A small initial investment in Dionics drivers pays for itself many times over.

Send for our enlightening new catalog.
If you are now, or may soon be, designing products with large or bright displays, you should have a copy of our new High Voltage Drivers Catalog. Use the reader service card, drop us a line or call, right now, (516) 997-7474. Then go ahead and make the displays as big and bright as you like. And leave the drivers to us. Dionics, Inc., 65 Rushmore Street, Westbury, New York 11590.

DIONICS

DIONICS INC., 65 RUSHMORE STREET, WESTBURY, NEW YORK 11590, (516) 997-7474 TWX 510 • 222 • 0974

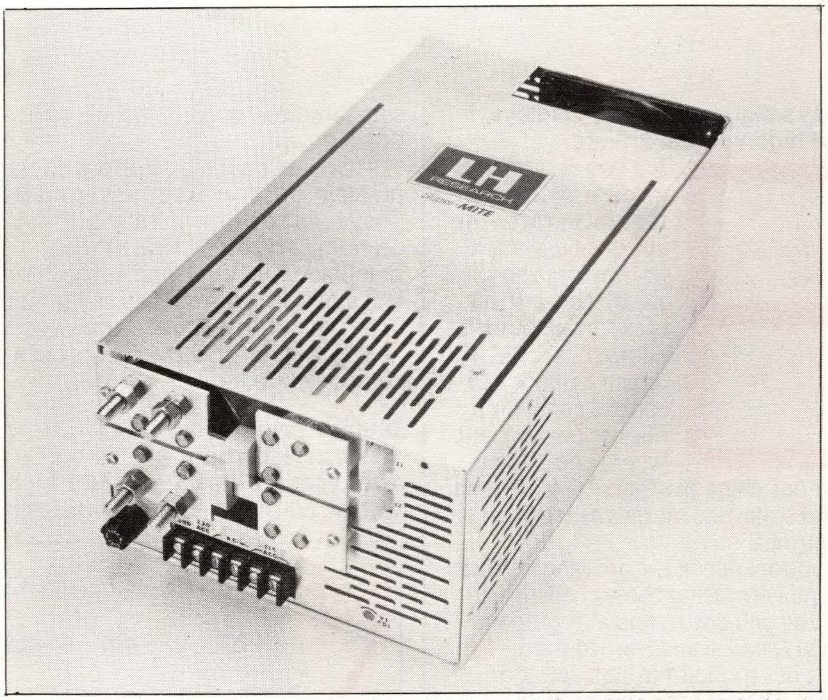
CIRCLE NO 122

1500W 5×8×11-in. closed-frame switcher uses custom control chip, power MOSFETs

Suited to high-speed ATE and scientific minicomputer applications, Model SM81 switcher features a custom control chip and four MOS power switching transistors. It switches at 40 kHz and delivers 1500W.

Despite a trend toward a reduction of power consumption per bit of computer memory, the supply's manufacturer sees a market for such high-power supplies, thanks to both the increasing number of bits per computer system and high-speed real-time computer applications requiring power-hungry ECL circuitry.

The 5×8×11-in. switcher operates on an 85 to 130V or 170 to 260V, 47- to 63-Hz input. Line regulation specs at 0.4% over each input range; load regulation equals 0.4% from zero to full load. Hold-up time after a power failure from a nominal 115 or 230V ac input equals 50 msec. Configurations offer single outputs ranging from 2V dc at 337A to 28V dc at 57A **(table)**.



With single-output ratings ranging from 2V dc at 337A to 28V dc at 57A, *Model SM81 offers current limiting, power-failure detection, remote-on/off capability, remote sense and overvoltage protection as standard functions.*

Simpler control

The supply's 4-transistor MOSFET configuration permits simpler control circuitry than that required by the 8-transistor bipolar configurations typically found in units with similar power ratings. Thus, the SM81 custom chip includes such switcher circuitry as the reference-voltage generator, sawtooth oscillator and pulse-width-modulation (PWM) comparator that control power-transistor switching, and the error amplifier that maintains constant output voltage. And it still has room for circuitry that lets the supply offer several standard features:

- Current limiting
- Undervoltage-sense and remote-enable functions that ensure controlled start-up and shutdown
- Power-good/power-fail circuitry, providing an open-collector TTL-compatible output that indicates output-voltage stabilization after turn-on and generating a signal at a fixed delay before the output goes out of regulation on input-power removal
- Overvoltage protection that disables the supply (input-power removal resets this circuit)
- Oscillator output that can synchronize other switchers to the SM81's switching frequency.

Options include an SCR crowbar circuit. UL component recognition and CSA certification are pending. The 20-lb supply's typical operating efficiency specs at 75%, and you can parallel units for extended power capability. $1295.

LH Research Inc, 14402 Franklin Ave, Tustin, CA 92680. Phone (714) 730-0162 or (617) 655-2120. **Circle No 453**

SM 81
OUTPUT CONFIGURATIONS

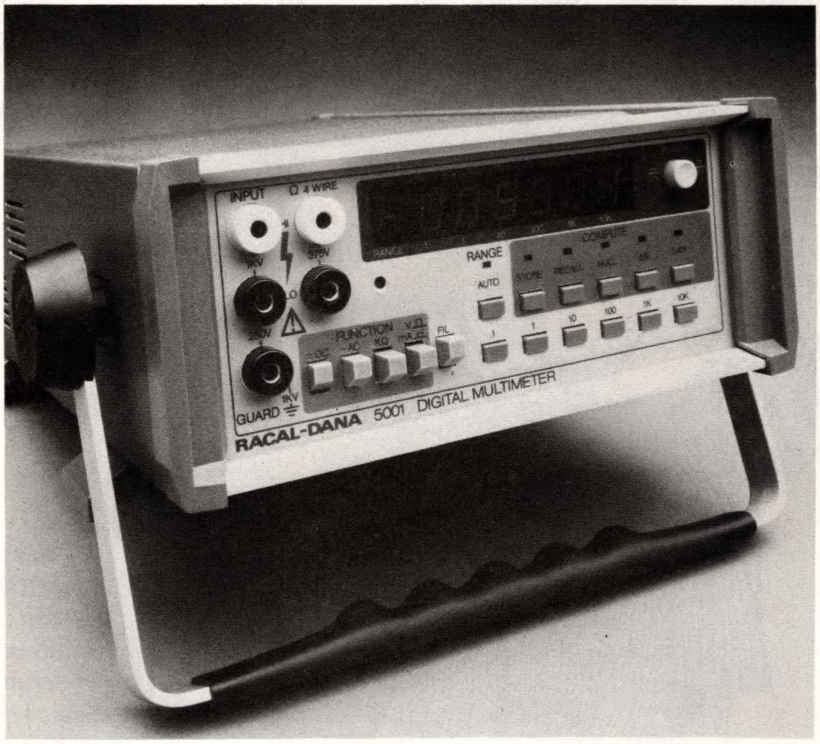
VOLTAGE (V DC)	CURRENT (A)
2	337
5	300
12	126
15	100
18	87
24	63
28	57

5½-digit true-rms DMM aims at low life-cycle cost

Model 5001 measures voltage to 1000V dc or 750V ac, current to 2A ac or dc and resistance to 99 MΩ. The 5½-digit instrument's manufacturer expects its 3-yr cost of ownership to be competitive with that of 4½-digit units.

Features helping to attain this cost performance include a built-in calibration function that reduces calibration time to less than 15 min and accommodates automatic calibration equipment. Additionally, built-in self-test and signature-analysis capabilities speed troubleshooting.

In addition to facilitating calibration and troubleshooting, the instrument's features also ease measurement tasks. For example, an automatic 2-wire/4-wire resistance mode makes the use of shorting bars unnecessary. To make 4-wire resistance measurements, you merely connect the sense leads; the instrument then automatically switches to the 4-wire mode.



Built-in calibration and signature analysis, *plus automatic 4-wire resistance-measurement capability, allow Model 5001 5½-digit DMM to compete in terms of cost of ownership with 4½-digit units.*

Deviation measurements

Other features include a Null function that lets you measure deviations from an initial value, a Percent Deviation function that expresses measurement deviation from a stored value, and a Low/Average/High function that stores the lowest, highest and average value of a user-selectable number of readings ranging from one to 10,000.

Filter features include a switchable single-pole analog filter, an integrating A/D converter that rejects noise at multiples of the power-line frequency, and a nonrecursive digital filter that averages the four most recent readings. When the instrument detects an input change of greater than 100 digits, this latter filter resets (ignores the older readings) to provide fast display updating.

The meter's metal case ensures immunity from RFI and EMI fields. DC accuracy specs at 0.007% of reading+3 digits (24 hrs, ±1°C), 0.02% of reading+5 digits (6 months, ±5°C).

A GPIB-interface option permits talk-only or addressable-talker operation. $1195.

Racal-Dana Instruments Inc, 18912 Von Karman Ave, Irvine, CA 92713. Phone (714) 833-1234. **Circle No 454**

NEXT TIME

EDN's July 22 issue is our 13th semiannual Product Showcase, an invaluable compendium of information on the most noteworthy new-product introductions of the past 6 months. You won't want to be without this fact-filled reference issue, which is organized into six key product areas:

- Components
- Computers and peripherals
- Hardware and interconnect devices
- ICs and semiconductors
- Instruments
- Power sources

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For more information, contact us at 5155 Old Ironsides Drive, Santa Clara, CA 95050. Phone (408) 727-0121.

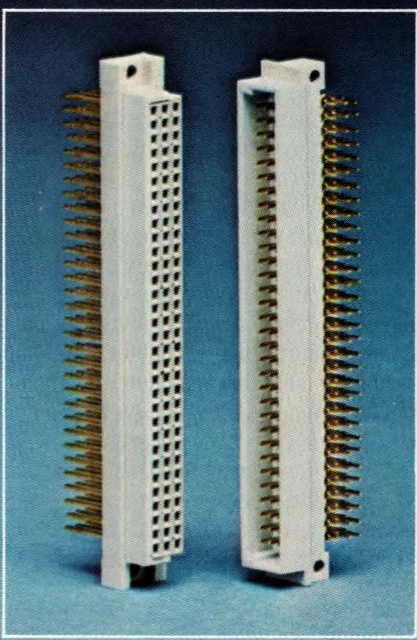
CIRCLE NO 124

Now!
The total high-density

Including design options conforming to

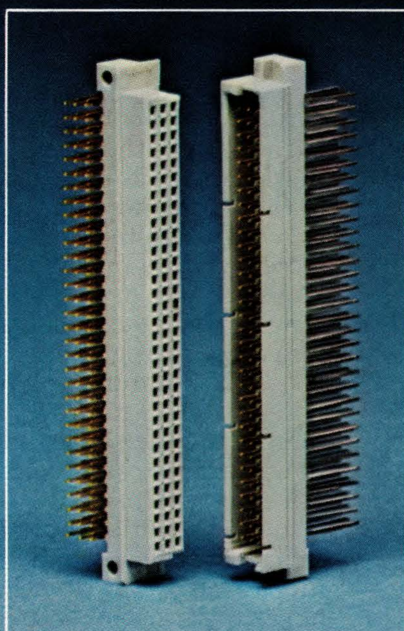
- 2-piece, high-density ".100 Grid" design permits greater packaging densities.
- Housings available in up to 96 contact positions to provide unlimited arrangements and configurations.
- Low mating forces for easy installation.

Standard Euroconnector
(PI Series):

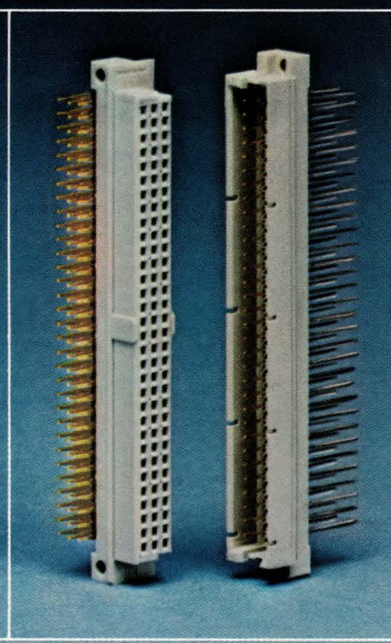


STD. PI SERIES
Conforms to DIN 41612, VG 95324 and IEC 130-14 specifications (with appropriate platings). Available in 2- or 3-row versions (48, 64 or 96 contact positions).

Reverse Euroconnector Types
(RPI Series):



STD. RPI SERIES
Reverse PI version features male contacts on back panel side for easy contact replacement . . . greater contact protection.



PRESS-FIT RPI SERIES
For solderless, press-fit applications. Contacts are gang-assembled into plated-through holes with semi-automatic insertion tool.

Now! Everything you'll ever want—or need—in a Euroconnector system. Every feature. Every design option. Every specification. Plus competitive pricing and all of the reliability you've been looking for.

They're all available—now—through one single, reliable American source: Burndy! Which means Burndy reliability. Burndy service. And Burndy technical assistance. All of which are solid reasons to check us out. We'd be happy to

From Burndy: Euroconnector system!

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- Fully interchangeable with all other Euro-Card connectors.
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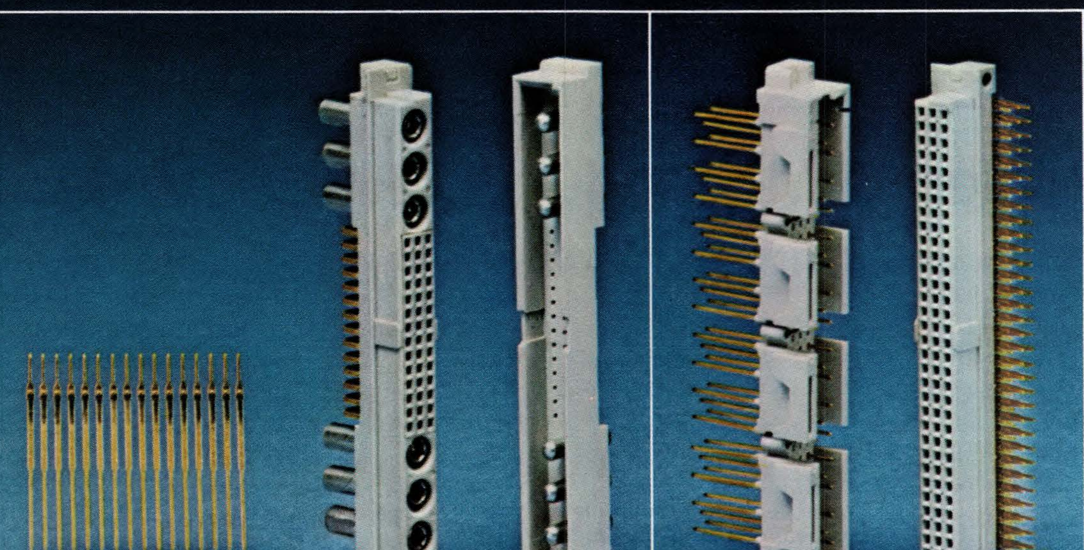

Designed for wirewrapping operations. Press-fit connection is gas-tight for low contact resistance even under severe environmental conditions. Power RPI version available for signal applications requiring power supply connections. Available with up to 42 signal contacts and 6 power contacts.

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CIRCLE NO 125

BURNDY CONNECTS

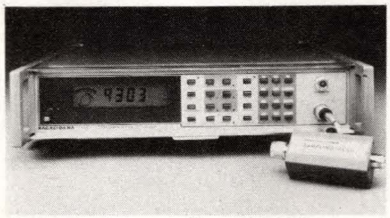
INTERNATIONAL SALES AND MANUFACTURING: BRUSSELS, BARCELONA, PARIS, ROTTERDAM, STOCKHOLM, STUTTGART, TURIN, ZURICH, ST. HELENS (ENG.), TORONTO, SYDNEY, TOKYO, MEXICO CITY, SAO PAULO

Autoranging GPIB-compatible RF-level meter measures 30 μV to 3V at 100 kHz to 3 GHz

Model 9303 measures true-rms levels from 30 μV to 3V in nine ranges at crest factors of at least 5 (14 dB) at over most of its operating range, and to 15 (24 dB) at each selectable range's low end.

The meter displays readings on a 4-digit LCD; a "pseudoanalog" display facilitates peaking and null adjustments.

An on-board μP supervises an automatic calibration sequence. It also permits computational functions: A Watts mode calculates power based on the measured voltage level and a value stored in an "ohms" reference memory; a Decibel mode lets the instrument display a reading in decibels relative to a value stored in its dB-reference memory. The instrument powers up with the value 223.6 stored in this memory to provide direct dBm indication (into a 50Ω load); you can also substitute your own value here.



Autoranging, self calibration and computational capability *highlight Model 9303. It measures 30 μV to 3V over a 100-kHz to 2-GHz range and displays voltage or relative stored reference values, decibels, watts, absolute and percent difference, or ratio.*

Specifications include 50Ω input impedance and input VSWR of ≤1.1 to 1 GHz and ≤4 to 2 GHz. Accuracy specs at ±1% of reading+20 μV over 18 to 28°C; 3% of reading+30 μV from 0 to 55°C. A GPIB interface is optional.

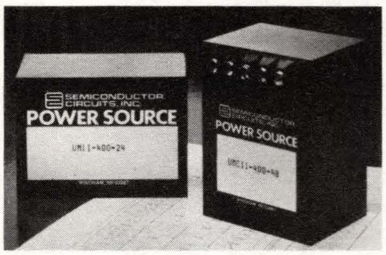
$3000. Delivery, 90 days ARO.

Racal-Dana Instruments Inc, 18912 Von Karman Ave, Irvine, CA 92713. Phone (714) 833-1234. **Circle No 455**

Encapsulated dc/dc modules deliver 5V, 4A

Designed for communications, process - control and marine applications, UM/UMC11-400 Series dc/dc converters deliver 5V at 4A in four mounting and input-voltage configurations.

PC-board-mountable Models UM11-400-24 and UM11-400-48 accept 18 to 36V and 35 to 70V inputs, respectively; chassis-mountable Models UMC11-400-24 and UMC11-400-48 accept 18 to 36V and 35 to 70V inputs, respectively.



Suited to telecommunications, process-control and marine applications, *UM/UMC11-400 Series dc/dc converters deliver 5V, 4A outputs from 18 to 36 or 35 to 70V inputs. They come in pc - board - or chassis - mountable configurations.*

Self-reset OVP

The devices operate at 75% efficiency and tolerate a 20°C case-temperature rise. They feature an automatic self-resetting overvoltage-protection circuit that shuts down the 24V-nominal-input models when their input reaches 38V and the 48V-nominal-input models when their inputs reach 75V.

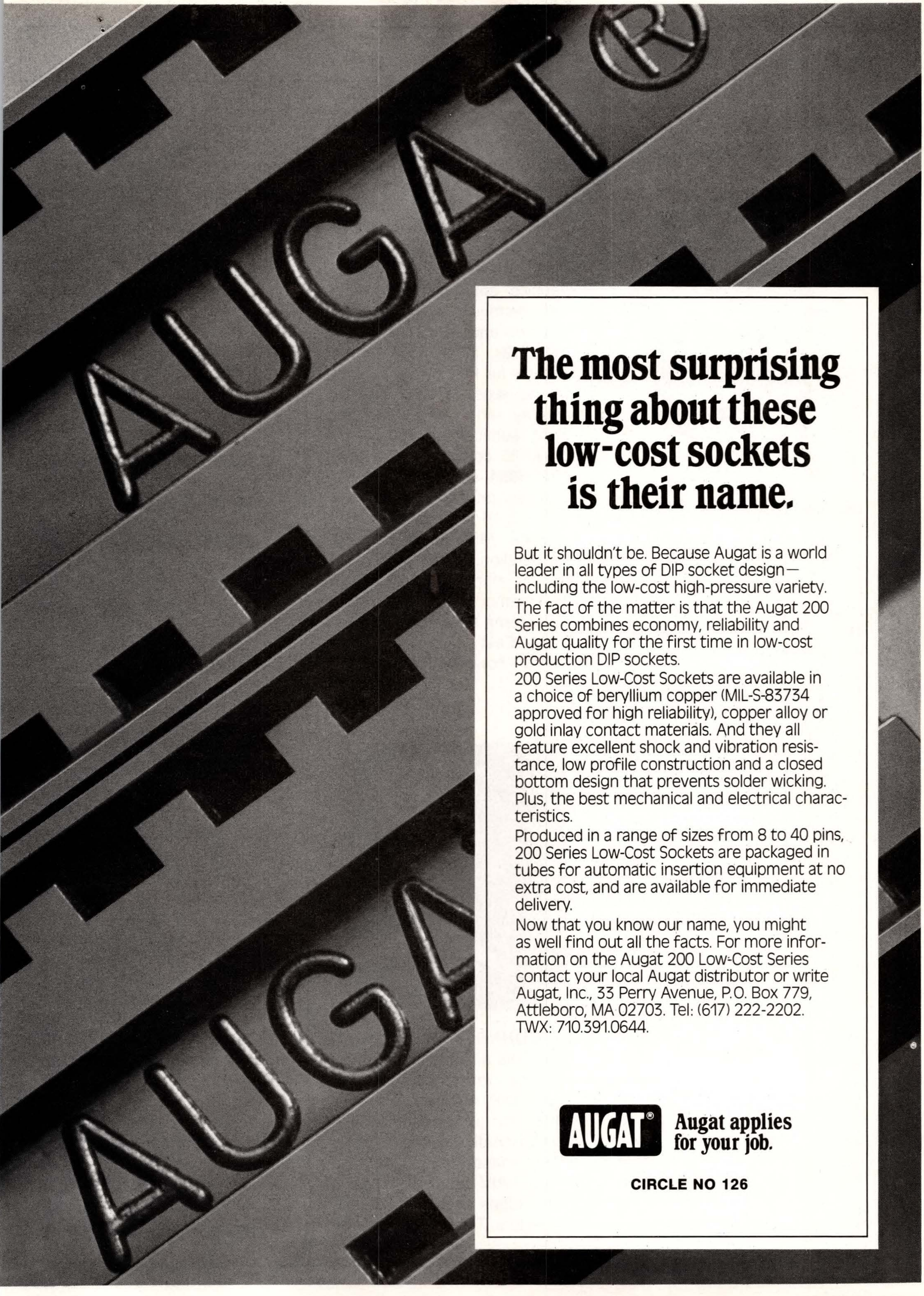
The 24V-input models can withstand a 60V continuous input without damage; the 48V models, 100V continuous. An input filter in each supply provides protection against power-line spikes.

Output protective functions include self-resetting power foldback that shuts down each converter under fault conditions, thus protecting the input supply—such as a battery—as well as the converter itself and the load.

The supplies provide 1500V dc I/O isolation. Line and load regulation each spec at 0.1%; noise and ripple is 7 mV rms, 50 mV p-p. Initial accuracy equals ±2%.

Each supply measures 2.5×3.5×2 in. and includes 4-40×0.1-in. mounting inserts for attachment to pc boards or chassis. $120. Delivery, 4 to 6 wks ARO.

Semiconductor Circuits Inc, 49 Range Rd, Windham, NH 03087. Phone (603) 893-2330. **Circle No 456**



The most surprising thing about these low-cost sockets is their name.

But it shouldn't be. Because Augat is a world leader in all types of DIP socket design—including the low-cost high-pressure variety.

The fact of the matter is that the Augat 200 Series combines economy, reliability and Augat quality for the first time in low-cost production DIP sockets.

200 Series Low-Cost Sockets are available in a choice of beryllium copper (MIL-S-83734 approved for high reliability), copper alloy or gold inlay contact materials. And they all feature excellent shock and vibration resistance, low profile construction and a closed bottom design that prevents solder wicking. Plus, the best mechanical and electrical characteristics.

Produced in a range of sizes from 8 to 40 pins, 200 Series Low-Cost Sockets are packaged in tubes for automatic insertion equipment at no extra cost, and are available for immediate delivery.

Now that you know our name, you might as well find out all the facts. For more information on the Augat 200 Low-Cost Series contact your local Augat distributor or write Augat, Inc., 33 Perry Avenue, P.O. Box 779, Attleboro, MA 02703. Tel: (617) 222-2202. TWX: 710.391.0644.

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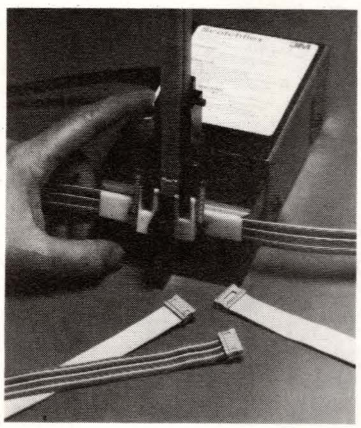
CIRCLE NO 126

New Products

INSTRUMENTATION & POWER SOURCES

DATA-ACQUISITION SYSTEM. Focus 5000 FORTRAN-controllable real-time system accommodates >1000 I/O channels and features >100,000-measurements/sec capability, 16-bit max accuracy and >85 types of analog and digital I/O boards. Combining the ANDS5400 data-acquisition system with the ANDS7000 controller and software, it utilizes the ANALIB library of >35 calls, including I/O, timing/synchronization, Boolean algebra and engineering subroutines. Comprehensive exerciser, diagnostic and self-test packages are also available. From $22,900. Delivery, 60 days ARO. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880. Phone (617) 246-0300. TWX (710) 348-0425. **Circle No** 229

SOFTWARE-DEVELOPMENT, MEMORY BOARDS. MSC 8801 and 8802 multiprocessor software-development stations run under CP/M 2.2, with MP/M and CP/NET also available. They include a Multibus-compatible Z80A-based computer, 64k or 80k bytes of RAM, two double-density 8-in. floppy-disk drives, a 7-card-slot Multibus chassis and heavy-duty system power supplies. Other features include provision for as many as eight serial communications channels, two 50-pin cable connectors for parallel I/O interfaces, three BNC connectors for video-graphics applications, a 12-in. CRT terminal with full-ASCII keyboard and an 80-cps printer. The 512k MCS 3611 add-in memory for PDP-11/70 computers replaces DEC's MK11-CE memory and plugs into the MK11 semiconductor box. For LSI-11/23 computers, the 256k MSC 4804 utilizes 64k RAMs, occupies one Q-bus slot and comes in 18- and 22-bit-address versions. MSC 8801 development station, $7985; MSC 3611 2-board memory, $4400; MSC 4804 memory, $2200. **Monolithic Systems Corp,** 84 Inverness Circle East, Englewood, CO 80112. Phone (303) 770-7400. **Circle No** 230



DIP-CONNECTOR TERMINATOR. This automated assembly machine terminates 14- or 16-pin DIP connectors to flat cable, in jumper or daisy-chained configurations, at rates >600 terminations/hr. Operating from a 120V supply, it employs plastic tubes containing 25 DIP connectors. The Scotchflex 3406 and 3416 connectors feature a rivet-top design that provides high cover retention; plastic posts form rivet-like heads when the connector is terminated. Beryllium-copper contacts are selectively gold plated. Tin-plated contacts are also available for soldering applications. Termination machine, $945.50; 14-pin DIP connector, $0.88 (1000). **3M Co,** Box 33600, Saint Paul, MN 55133. Phone (612) 733-9214. **Circle No** 231

μC DEVELOPMENT SYSTEM. For high-level-language and future 16-bit-μP applications, Starplex II employs two Z80A μPs in a master/slave configuration. The master processor accesses 64k of RAM and controls the operating system. The slave processor also has 64k of RAM and controls user programs. A typical configuration comprises two Z80A-based CPUs, 128k of RAM, 1M bytes of 8-in.-floppy-disk storage (two drives), video monitor and keyboard; it also features a disk-based operating system, debugger, text editor, assembler, linker, FORTRAN, BASIC, utilities and diagnostics and a universal programmer interface for PROMs and Monolithic Memories' PAL devices. A spooled printer permits simultaneous printing and editing, compiling or assembling. Optional high-level-language support of PL/M and PASCAL is available, as are code generators for 8080/8085 and Z80/NSC800 processors working with both these high-level-language compilers. $15,950 to $18,600; upgrade kit for Starplex I, $3000. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051. Phone (408) 737-5000. TWX 910-339-9240. TLX 346353. **Circle No** 232

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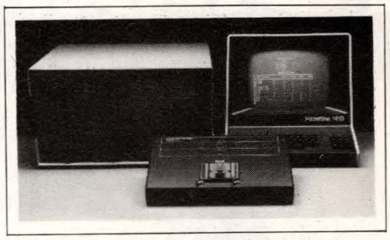
New Products

INSTRUMENTATION & POWER SOURCES



GATE-ARRAY TEST SYSTEM. For testing gate arrays and custom digital ICs, Inspector 200/4G is a 48-pin digital system compatible with all MOS families. TBASIC-4 test software permits development of test programs for custom chips. A set of utility programs permits creation, editing and merging of test programs. Decisions, branches, subroutines and calculations performed on data input from the tester can be implemented during testing. Test electronics includes three power supplies programmable to 25V, 48 programmable device pins and a parametric measurement unit. \$29,590. **Pragmatic Designs Inc,** 950 Benicia Ave, Sunnyvale, CA 94086. Phone (408) 736-8670. **Circle No 233**

TEST-PROGRAM SOFTWARE. Incorporating improvements to Version 5.1 of its company's LASAR test-program-generation software, Version 5.2 can reduce development time for functional test programs for LSI and VLSI pc boards. Improvements in the DYSOGN software module, which determines the fault coverage achieved by test patterns, result in 2- to 4-times-shorter run times. The package also provides the company's TML high-level modeling language and 15 additional LSI models and >125 SSI/MSI models. A new data format, LSRTAP, permits users to devel-

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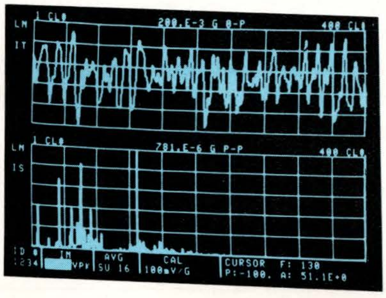
Nicolet's new 100A MINI-ANALYZER is powerful, yet portable and easy to use...and also lower in price.

It's as simple as a doctor's stethoscope for you to use in diagnosing the cause of vibration or noise in real time ... from .005 Hz to 20,000 Hz (0.3 to 1,200,000 CPM)

It is specifically designed to get answers to real problems fast, simply and accurately. We listened carefully to the ideas from many of the 1000's of Nicolet users throughout the free world doing noise or vibration testing in such industries as petrochemical processing, power generating, paper production and vehicle design and manufacturing. They wanted a unit that anyone could learn to use and take into the field at a price anyone could afford.



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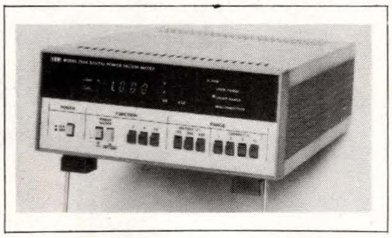
New Products

INSTRUMENTATION & POWER SOURCES

op and maintain their own post-processors. Supplied free to current LASAR software-license holders; $180,000 for the first installation. **Teradyne Inc,** 35 Morrissey Blvd, Boston, MA 02125. Phone (617) 482-2700. TWX 710-321-1055.

Circle No 234

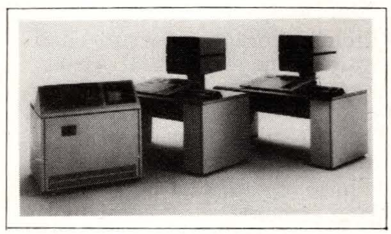


POWER-FACTOR METER. Measuring power by using both the power-ratio method and by the ratio-of-power-to-true-rms volt-amperes method, Model 2524 operates over a range from 0.5 lag to 1 to 0.5 lead at voltages of 120, 240 and 480V and currents of 1, 2, 5 and 10A. Watt (or VARS) measurements can be performed over a 120W to 4.8 kW (or VARS) range. Accuracy for both power-factor measuring methods specs at ±0.015. True-rms voltage and current accuracy equals ±0.5% of reading+1 digit. Frequency range spans 40 to 400 Hz. From $2500. **Yokogawa Corp of America,** 2 Dart Rd, Shenandoah, GA 30265. Phone (404) 253-7000. **Circle No 235**

BIT-SLICE DEVELOPMENT. The AmSys 29/10 development system, with optional integrated logic analyzer, provides for the symbolic development of microcode and features a high-speed control-store emulator, target-system clock control and logic-state monitoring. Its writeable control store replaces control-

store PROM with high-speed RAM, and clock-control logic adds breakpoint and single-step capability. A single-card microprogram sequencer furnishes microprogram familiarization and software-module testing. The AMDASM meta-assembler supports microcode development and permits definition of a mnemonic instruction set for any microinstruction format. The optional high-speed trace unit (Am29/6310) with logic-state-analyzer capabilities performs real-time event and count measurements to 10 MHz on a 48-bit-wide sample. As many as 256 time and data samples can be stored. $20,500 for basic system including 1k×64 bits of writeable control store; high-speed trace unit, $5990. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086. Phone (408) 732-2400.

Circle No 236



CAD/CAM SYSTEM. The Designer M medium-scale multi-application CAD/CAM system provides the same level of performance and functionality as its manufacturer's Designer IV system. Suiting applications ranging from mechanical design and drafting to printed-circuit design, cartography and IC design, it consists of the company's CGP-80 graphics processor with 80M-byte fixed-disk and 7-in. 1800-bpi magnetic-tape drives, two raster-scan interactive design workstations with 19-in. CRT and 17×24-in. digitizer command tablet, system console and a CAD/CAM-software application package. All application packages except the IC-design package are supported by a common database. A maximum of three tasks, two interactive and one batch, can be simultaneously supported. A pen plotter, photoplotter or paper-tape punch/reader and communication links such as CVNET and Graphics Network Architecture are optional. $180,000. **Computervision Corp,** 201 Burlington Rd, Bedford, MA 01730. Phone (617) 275-1800. TLX 923345.

Circle No 237

POWER SUPPLIES. Incorporating 3½- or 4½-digit digital meters, 10V/10A to 200V/0.7A HWD constant-voltage/current units regulate load voltage to 0.01% and line voltage to 0.005%. Ripple equals <500 μV rms. Recovery time remains within 100 μsec. Remote programming and sensing capability and series or parallel operation are also provided. $660 to $875. Delivery, stock to 8 wks ARO. **Incom International Inc Controlex/Eanco Div,** 539 Jacksonville Rd, Warminster, PA 18974. Phone (215) 672-4800.

Circle No 238

8. ● **Circuit Testing Update/No. 8 in a series from Hewlett-Packard.**

AFTER THE DECISION TO TEST, HOW DO YOU CHOOSE THE RIGHT IC TESTER?

Yes, incoming inspection is generally the best place to spot, and stop, faulty digital ICs. Because failures can cost 10 times more to spot at the board level; 100 times more in a completed system; and a whopping 1000 times more in the field. But how do you choose the best IC test solution?

Start with a few key questions.

1) Are programs available for the ICs you need to test? Check the manufacturer's program library. Make sure it covers enough devices to start paying off your hardware investment now.

2) Are programs available individually so you can tailor your library to your own needs? Are they easy to access and update?

3) Can you customize programs or write your own if necessary? What aids are built in to simplify custom programming and editing?

4) How tough should a test be? You'll probably want to do more than functional (truth table) testing. Performing both functional and DC parametric testing (input/output voltage and current) can let you weed out up to 95% of the faulty ICs. But it's also important to know how DC parametric testing is done. Loading one output pin at a time probably won't simulate use conditions. It won't catch metallization masking and other process problems. Make sure you can do full fanout testing.

5) Do you get a printout of failure information? How much does it cost? This can be valuable information for evaluating marginal failures and for obtaining statistical failure data.

6) What features contribute to high throughput? Ask about hardware reconfiguration. You don't want a complicated setup for each new device tested. Get the facts on clocking frequency. High frequency doesn't necessarily mean higher throughput, nor does it mean AC testing. Make sure your operators can handle setup, program loading, and operation with little training. And find out how difficult it is to interface to IC handlers for automated and environmental testing.

When HP's Digital IC Testers make sense.

HP has two Digital IC Testers to choose from. The 5045A test system at $12,250* and the 5046A test/programming system at $28,200*. When you're looking for cost-effective IC testing and program generation, HP can help.

Our program library is perhaps the largest available. You can buy just the programs you need, choosing from more than 2100 digital ICs, including many memory devices. And the library keeps growing. For custom programming, the 5046A Digital IC Test System includes a desktop controller with software that simplifies programming and editing. Use the controller — a standard HP 9825B — for other control tasks via Hewlett-Packard Interface Bus, too.

Figure 1. — Over 2100 IC test programs to choose from

```
SUMMARY:
PASS        261, =  89.1% OF TOTAL
FAIL         32, =  10.9% OF TOTAL
TOTAL TESTED = 293
CONTINUITY FAIL   9, = 28.1% OF TOTAL FAILS
FUNCTION   FAIL  10, = 31.3% OF TOTAL FAILS
FAN OUT    FAIL  31, = 96.9% OF TOTAL FAILS
```

Figure 2 — Failure information includes statistical test summary

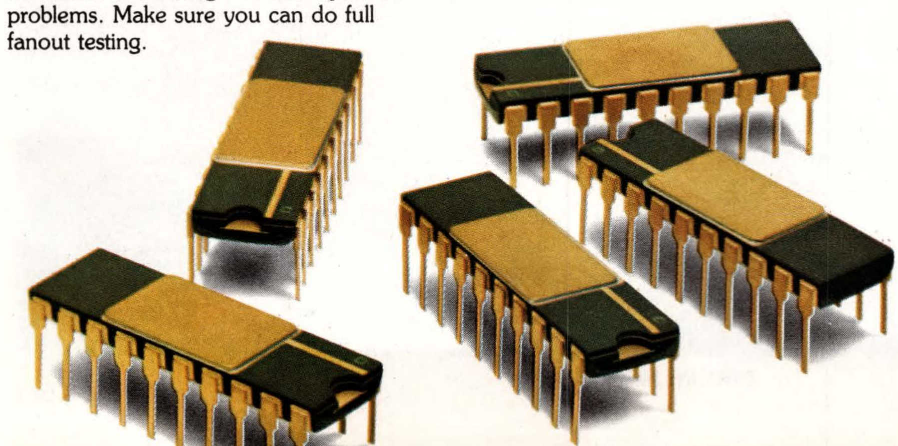
To ensure high throughput, we've kept things simple. If you can operate a dollar bill changer, you can operate our tester. You simply insert a magnetic programming card (Fig. 1), put an IC in the test socket and press the test button. Install one of many compatible automatic IC handlers and it's even easier. . .faster too. And when package widths change, you simply plug in another test socket. There's no time consuming hardware reconfiguration.

Finally, HP incorporates parallel pin testing to weed out more faulty or marginal devices. What's more, hard copy printout of test results and statistical data (Fig. 2), is standard. It all adds up to comprehensive testing and high throughput at low cost. . .a good combination.

Getting closer to a decision.

We have data sheets and application information that can help you choose the system you need. Contact your local HP Field Engineer. Or, write to Hewlett-Packard, 1820 Embarcadero Road, Palo Alto, CA 94303. Or call the HP regional office nearest you: East (201) 265-5000; West (213) 970-7500; Midwest (312) 255-9800; South (404) 955-1500; Canada (416) 678-9430.

*Domestic U.S.A. price only.



HP Circuit Testers — The Right Decision

02104A

CIRCLE NO 130

HEWLETT PACKARD

New Products

INSTRUMENTATION & POWER SOURCES

PORTABLE SCOPE. Model 880 provides four channels, each with a high-voltage differential input, which can directly accommodate voltages associated with 600V 3-phase power lines or 600V dc supply systems. The input's common-mode voltage permits application of a 350V rms or ±500V dc signal to both inputs of each channel (at sensitivity of 100 mV). Amplifier bandwidth specs at 7.5 MHz with >50-nsec rise time. Phase measurement is displayed by screen marker, while phase angle between the zero-crossover marker and degree marker is read out in 1° steps on a separate digital display. Safety features include insulated control knobs and front panel. $4950. Delivery, 60 days ARO. **Marconi Instruments Inc,** 100 Stonehurst Ct, Northvale, NJ 07647. Phone (201) 767-7250. TWX 710-991-9752.

Circle No 239

INTERFACE / INSTRUMENT COUPLER. Furnishing a programming GPIB interface, the pc-board-mounted Model 350 interprets a computer's digitally coded ASCII programming instructions and latches, optically isolates and converts them into two analog (0 to 1 to 0 to 10V) outputs for ATE systems. Accuracy equals ±0.2%; resolution, 0.1%. As many as 30 address configurations are available. A listen-only function permits address override, enabling the unit to listen to all bus transactions whether addressed or not. A negative-output line and SRQ facility are also featured. £490. **Hendry Electronics Ltd,** 2 River Rd, Arundel, West Sussex, BN189DH, England. Phone (0903) 882255. TLX 877285.

Circle No 240

DEVELOPMENT SYSTEM. Suiting programmable-data-logging, controller and prototyping applications, Digilog provides a 10k FORTH PROM- and stack-based 1802 operating system with 32k dynamic RAM, supports a video display or terminal and features storage for as many as 500 lines of high-level source code. An editor, assembler and compiler and a control panel with 8-digit LCD, 17 touchpad keys, a 20-bar-segment LCD and beeper for audible output are also

Winning performance down to the wire. Multiwire.®

Jim Hill, Vice President Products and Services,
Systems Engineering Laboratories,
Fort Lauderdale, Florida

Reporting the results of a test of three circuit board technologies, Jim Hill of Systems Engineering says, "We're a big winner with Multiwire."

In this test, identical technical assignments were initiated with Multiwire, multilayer and wirewrap to produce two new double floating point processing boards for Systems' 32 bit scientific minicomputers. The 15" x 17" boards were to contain an average of 300 IC's.

Multiwire was the victor hands down. For good reason.

High Speed Electrical Performance

"Multiwire allows us to build high performance systems without sacrificing noise margin," says Hill. The copper circuitry of Multiwire provides consistent and controllable electrical characteristics so important to high speed logic.

Custom Design

Even the most difficult high density board configurations and specifications are achieved through Multiwire design technology.

Fast Turnaround

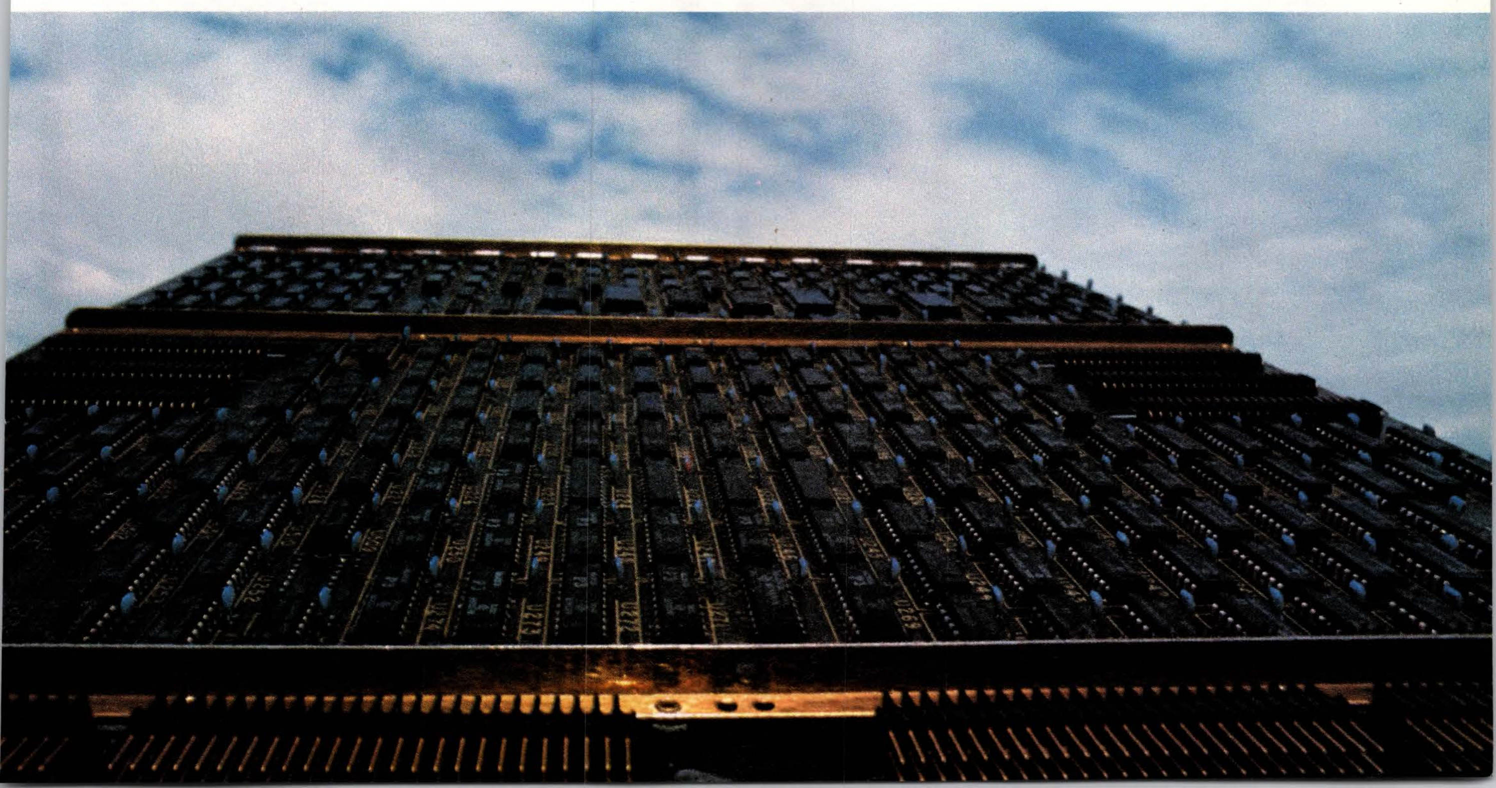
Multiwire delivered boards four to six months faster than multilayer.

Performance. Design. Delivery. Multiwire gives you all to make you a big winner, too. Challenge us with your next assignment.

Multiwire Division, Kollmorgen Corporation,
31 Sea Cliff Avenue, Glen Cove, N.Y. 11542.

CIRCLE NO 132

MULTIWIRE® DIVISION
KOLLMORGEN CORPORATION

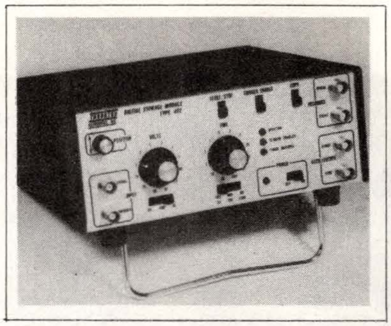


INSTRUMENTATION & POWER SOURCES

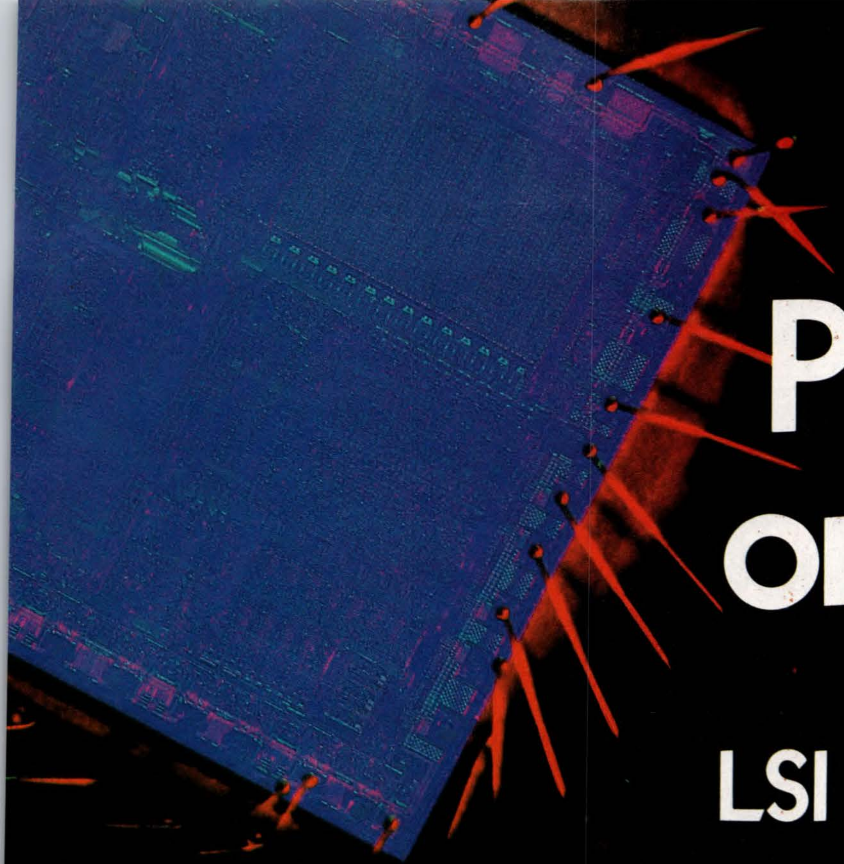
provided. The unit additionally furnishes a real-time clock and calendar, five 16-bit timers, a 16- and 32-bit integer-arithmetic package, serial RS-232C port and 16 I/O lines. From $2885, including charger/interface unit. **Golden River Corp,** 7315 Reddfield Ct, Falls Church, VA 22043. Phone (703) 827-9090.
Circle No 241

STORAGE SCOPE. Furnishing a 4k-byte memory and dc to 10-MHz (−3 dB) bandwidth in Normal mode, the dual-trace Model DSO4020 also provides switch selection of 1k-byte portions of stored waveforms. Other features include expansion to 50× with dot joining, pretrigger viewing, unattended transient-capture capability and operation as a conventional 5-mV-sensitivity scope. Refresh mode refreshes the display upon each trigger input; Roll mode mimics a strip-chart recorder, permitting the signal to scroll across the screen. I/O includes external-clock output and input, Ready and Gate facilities. Sensitivity equals 5 mV/cm to 20V/cm in 12 ranges. **Gould Inc,** 3631 Perkins Ave, Cleveland, OH 44114. Phone (216) 361-3315. TWX 810-421-8580.
Circle No 242

STORAGE MODULE. The digital Type 492 converts analog-input signals into digital codes and stores them in a 1k×8-bit memory. The memory contents are then reconverted into analog



signals at a fast rate for stationary-scope-trace oscilloscope display or at a 4-sec rate for strip-chart recording. You can thus use the module to convert any scope with external trigger input into a storage scope. 36 ranges of sampling periods from 0.005 sec to 2000 hrs are available. Timing accuracy is crystal controlled with error ≤±0.01%. From $595. **Thornton Associates Inc,** 87 Beaver St, Waltham, MA 02154. Phone (617) 899-1400. **Circle No 243**



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September 28–October 2, 1981
March 29–April 2, 1982

Choosing the right LSI gate array and effectively designing it for your application

KEY TOPICS

- Digital bipolar and MOS gate technologies
- Gate-array companies
- The system translation
- Design of gate arrays
- Gate arrays of the future

BIPOLAR LINEAR CIRCUIT DESIGN

September 21–25, 1981

Process specification, biasing techniques, and resistor design, and layout techniques

KEY TOPICS

- Bipolar wafer processes
- Bipolar component structures
- Specification of processes
- Design of transistors and resistors
- Circuit design techniques for linear circuits
- Layout of linear circuits

MOS DIGITAL CIRCUIT DESIGN

September 14–18, 1981

Transistor logic structures, transistor design, circuit analysis and introductory layout techniques

KEY TOPICS

- MOS wafer processes
- Basics of MOS transistor theory
- Logic simulation (introductory only)
- Conversion of logic to NMOS/ CMOS logic structures
- Sizing of transistors and circuit simulation
- Layout of cells and preliminary composite plan
- Use of graphic systems (introductory only)

CIRCLE NO 134

Each Seminar is an intensive one-week program which combines lecture and workshop exercises directed toward the graduate engineer with less than six months experience in designing ICs or the systems engineer unfamiliar with IC design. Each seminar is $1200 (includes all materials and books) and is held at the ICE Design Center, Scottsdale, Arizona. Seminar text is available separately for $500 each.

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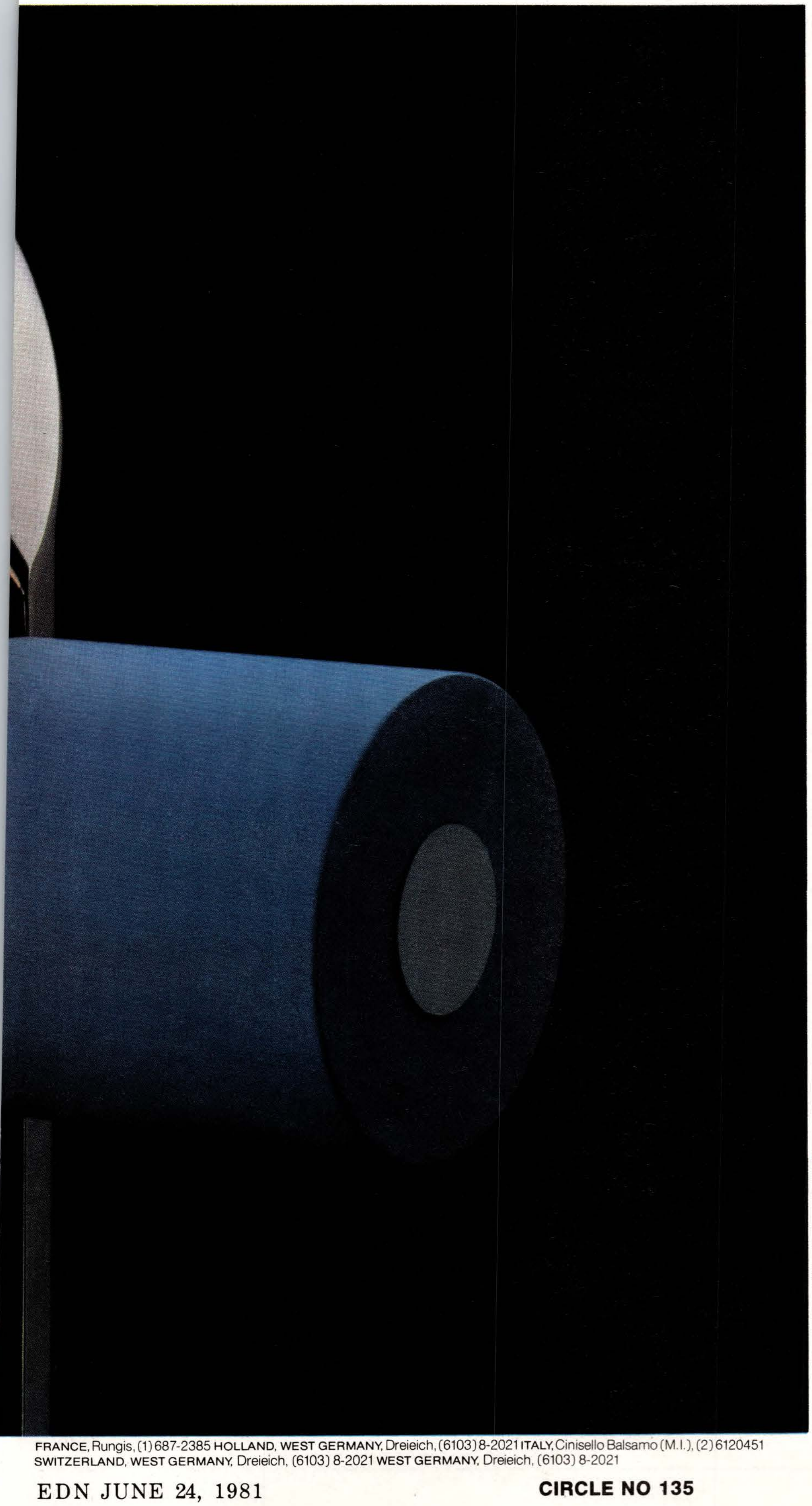

Our TULIP® contact will have it. Even after 40 years.

Aging tests on T&B/Ansley BLUE MACS® insulation displacing connectors showed that after forty years, our exclusive TULIP® contact will retain at least 92% of its initial contact energy, even with conductor creepage or deformation. Your benefit is long-lasting contact integrity even after forty years.

Impressive. How did we make it so durable? With the unique, patented shape of our beryllium copper TULIP® contact. The two contact slots have been designed to provide high contact pressure and maintain mechanical stability. They also provide up to four separate points of contact on each conductor.

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Every single BLUE MACS® mass assembled flat cable-connector system incorporates the TULIP® contact.

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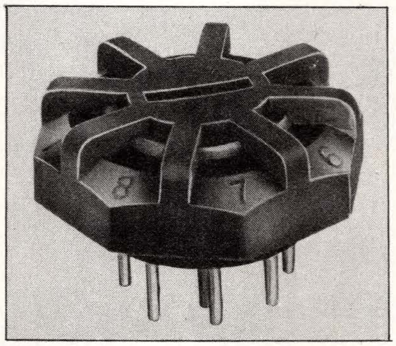
CIRCLE NO 135

Rugged $1 subminiature rotary switches spec 10,000-operation contact life

Compatible with pc-board mounting, Series S-119 rotary switches come with two to eight positions and feature a novel design that uses fewer moving parts than most switches. The entire mechanism is built into a plastic part whose lobes divide the contact positions and provide a detent.

The switch design achieves a highly positive feel in operation—the switch actually snaps into a new position when indexed by hand or with a screwdriver. Pins and internal connections are gold plated for extended reliability—contact life specs at 10,000 detent operations.

Switch contacts are rated for 100 mA at 25V dc, and initial contact resistance specs at 50 mΩ. Dielectric strength equals 500V rms, and operating range spans −10 to +60°C.



High reliability is a prime feature *of S-119 rotary switches. With a 10,000-operation life, their gold-plated contacts have high corrosion resistance in applications involving extremes of temperature and humidity.*

Inexpensive construction

S-119 switches have no expensive stampings. A dog-legged-shaped pin provides a common center terminal that acts as a pivot point for a contact.

The contact, a torsion spring, moves between several stationary detented areas on a single U-shaped outer pin. Its legs scissor the center contact, and the scissoring action provides a forward thrust on the torsion-coil contacts, which mate against the stationary contact points on the U-shaped pin.

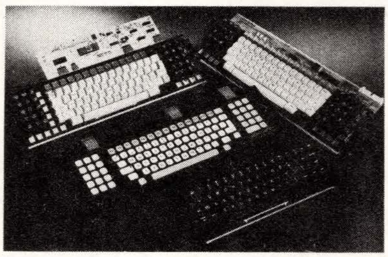
$1 (OEM qty) for an 8-position device. Delivery, 16 wks ARO.

***TEC Inc, 2727 N Fairview Ave, Tucson, AZ 85705. Phone (602) 792-2230.* Circle No 457**

Fully sealed membrane keyboards find use in low-cost terminals

Designed for industrial, home and commercial applications, these membrane keyboards include two full-travel designs (hard-contact and capacitance) and one touch-panel unit. All feature sealing and venting to protect the signal-generating elements.

In the capacitive unit, floating-pad capacitor plates located between the screened-on drive and sense pads minimize stray-capacitance problems. A matrix encoder automatically grounds unused sense and drive lines, providing shielding to reduce the effect of electrical noise. The unit features tactile feel and n-key rollover.



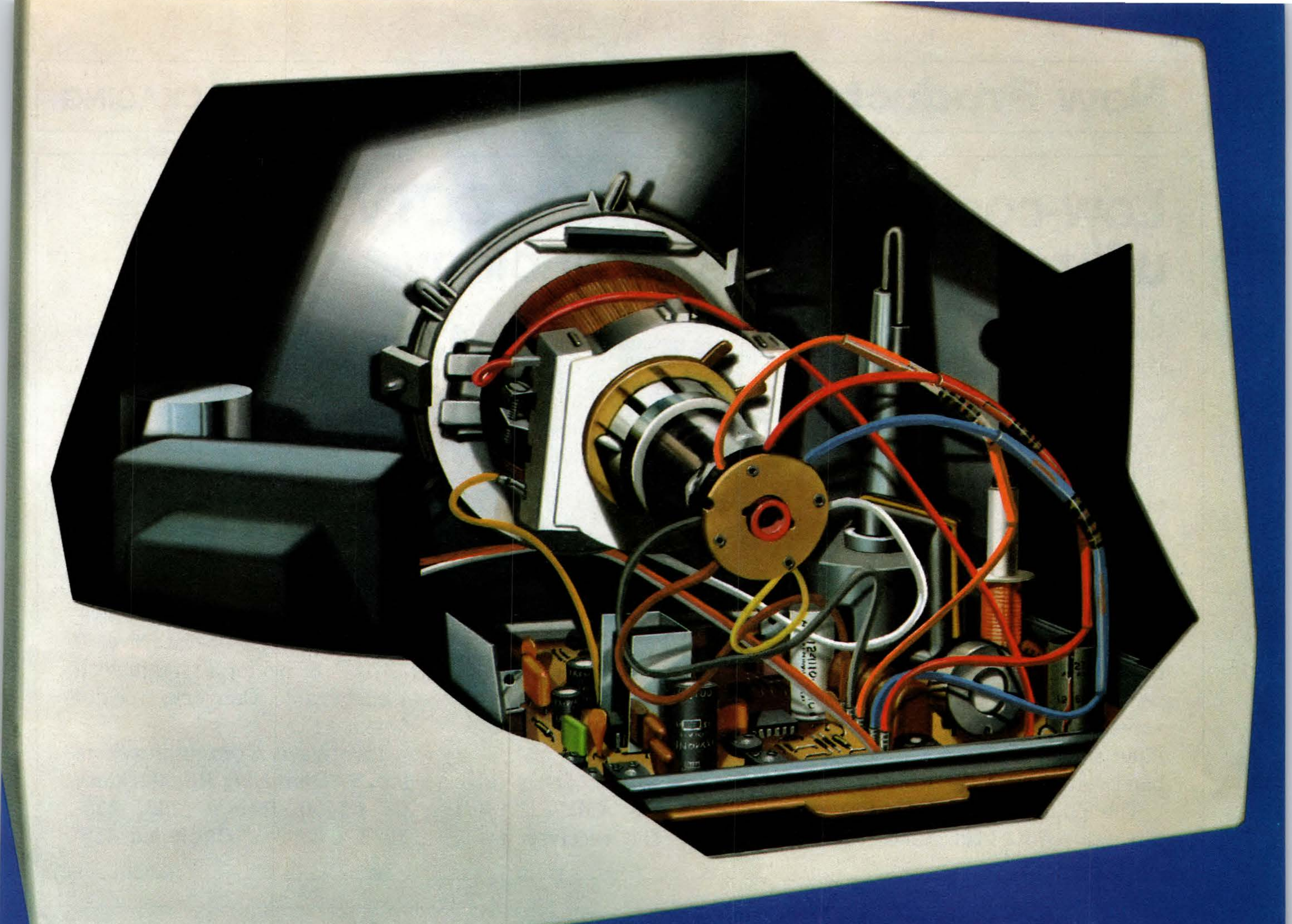
Designed for low-cost-terminal applications, *this line of membrane keyboards includes flat touch panels and hard-contact and capacitive designs.*

The hard-contact keyboard comes in matrix-only and encoded versions that furnish 2-key rollover. Both versions provide standard or low-profile key modules that meet the newest European standards for display workstations.

The touch-panel unit provides an alternative terminal interface for applications that don't require high throughput. Legends are screened directly onto the embossed panel surface. To screen out contaminants, this keyboard is channel-vented through baffles from the spacer and lower circuit layers.

Fully encoded 70-key capacitance unit, $65; matrix-only 70-key hard-contact device, $45; touch-panel unit, $30 (OEM qty). Delivery, 3 to 4 months ARO.

***Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600.* Circle No 458**



Imagine the advantages Motorola's simple new building block system will give your design engineers

Motorola's new Alpha Series is more than a new generation of 12" and 15" display modules. Its design, though remarkably simple, redefines the standards by which you will measure the performance of your terminals.

Greater reliability

On-going tests project a dramatic 75% increase in MTBF over even our own most reliable MD series.

Greater reliability is a result of synergistic elements at work at Motorola. Paramount is product design. The Alpha Series makes extremely efficient use of fewer components and incorporates integrated circuits throughout the system.

Advanced manufacturing processes and revolutionary testing equipment at Motorola's unique multi-million dollar facility in Joplin, MO, are designed to improve the quality and reliability of the Alpha Series.

Enhanced video performance

Motorola has extended resolution and bandwidth in the Alpha Series for sharper alphanumeric presentation. Center resolution has been increased from 1000 to 1200 lines; corners from 750 to 950 (P4 phosphor). Bandwidth has been stepped up from 22 MHz to 30 MHz (−3Db). Compare geometry and linearity specifications and you'll find that Motorola's Alpha Series ranks among the highest in the industry.

Design flexibility

Whether your requirements call for composite video, true TTL compatibility or direct drive, the versatile Alpha Series can handle a wide signal input variation. Horizontal scan rate is available at 15.7 or 18.7 kHz. The streamlined chassis of the new display allows you more flexibility in your mechanical design. Ease of access to the controls and unique options such as 24 vdc operation and 20 pin ribbon cable add to making the Alpha Series extremely adaptable display modules.

Motorola displays the character of your business.

MOTOROLA

Display Systems

1299 E. Algonquin Road Schaumburg, IL 60196
312/397-8000

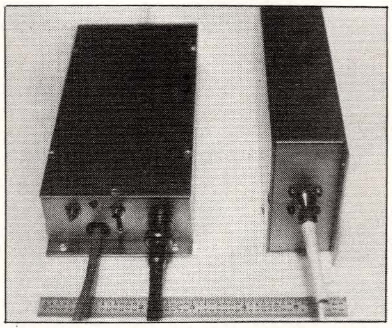
CIRCLE NO 136

Low-cost, wide-bandwidth CCTV link utilizes fiber-optics technology

System 8211 transmits high-resolution monochromatic or composite color-video signals as far as 2 km without equalization or repeaters.

The 8211T transmitter employs an LED (mounted in an AMP 227240-1 connector) as its source. It can handle video inputs of 0.5 to 2V p-p. Depth of modulation, preset for a 1V p-p input, can be internally matched to the application. The transmitter features a peak emission wavelength of 820 nm, 75Ω input impedance and a 20-MHz bandwidth.

The 8211R receiver drives 1V p-p into a 75Ω load. Its silicon PIN-diode detector is also housed in an AMP 227240-1 connector. The receiver has a typical bandwidth of 20 Hz to 20 MHz and includes gain adjustment. Responsivity at 850 nm equals 0.5 μA/μW.



Available complete with connectorized fiber-optic cable, *System 8211 transmits high-resolution composite-video signals to 2 km without requiring repeaters or equalization.*

Connectorized fiber-optic cable is optional. The transmitter and receiver modules measure 3×6×1.5 in. Power requirements stand at ±18V dc for the transmitter and −18V dc for the receiver.

Both modules operate over 0 to 70°C. $2595 for a system with 1 km of cable. Delivery, stock to 6 wks ARO.

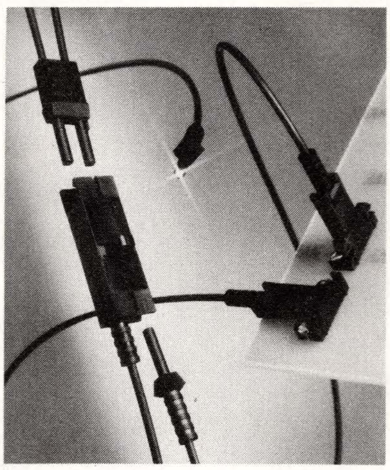
Lightwave Communications Inc, 57 Glen Hills Rd, Meriden, CT 06450. Phone (203) 238-3078. **Circle No 459**

Connector system lowers fiber-optics costs

Mounting quickly and easily, this line of connectors aims at the data-transmission market characterized by 10M-bps data rates and 10 to 30m distances. The family includes seven basic components: single- and dual-position plugs, single- and dual-position bulkhead (feed-through) receptacles, a splice housing and single-position active-device mounts for TO-92 and TO-18 packages.

The system is compatible with any 1000-μm all-plastic fiber. Termination requires no special tooling, epoxy or polishing steps. To attach a plug, you merely strip off the protective jacket and insert the fiber from the rear of the body until the jacket bottoms inside the plug cavity. You then cut off the protruding fiber flush with the plug's tip.

The entire operation takes about 15 sec. A brass retention clip in the plug anchors the fiber in place to withstand an 8-lb axial pull. Depending on how you cut the fiber, insertion loss can range from 2 to 4 dB; using an index-matching liquid reduces losses by at least 50%.



To significantly lower the cost of short-haul links, *these $0.25 (10,000) fiber-optic connectors are designed to accommodate 1000-μm plastic fibers and low-cost TO-18- and TO-92-style active devices.*

When mating the plug to a receptacle or active-device mount, an audible snap indicates proper positioning. Disconnection requires a 6-lb extraction force. $0.25 (10,000).

AMP Inc, Harrisburg, PA 17105. Phone (717) 780-8851. **Circle No 460**

Mallory tantalum capacitors earn top MIL reliability ratings.

In solid tantalums, Mallory is now qualified to provide Level S, the highest reliability rating, for styles CSR 13 and CSR 91. Level S, under MIL-C-39003, means a life failure rate of only 0.001% per 1,000 hours. Here is our current QPL line-up in solids:

MIL Style	Mallory Type	Life Failure Rates
CSR13	TER	M, P, R, **S**
CSR23	TXE	M, P, R
CSR33	TXR	M, P
CSR91	TNR	M, P, R, **S**

In wet slug tantalums, we have become the first source qualified at Level R, under MIL-C-39006, for style CLR69 — the extended capacity range wet tantalum, which makes our wet QPL list look like this:

MIL Style	Mallory Type	Life Failure Rates
CLR10	XTM-XTK	L, M, P
CLR14	XTL-XTH	L, M, P
CLR17	XTV	L, M, P
CLR65	TLX	L, M, P, R
CLR69	TXX	L, M, P, **R**

They're all available from authorized Mallory Distributors. Send for our latest QPL bulletins. Mallory Capacitor Division, Mallory Components Group, P.O. Box 372, Indianapolis, Indiana 46206. (317) 636-5353.

MALLORY

ELECTRICAL/ELECTRONIC GROUP

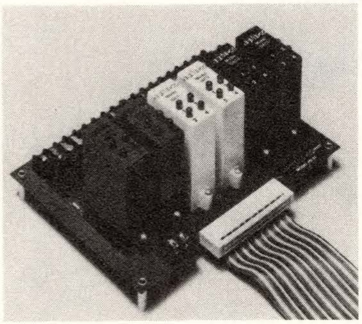
EMHART

CIRCLE NO 137

C8100

New Products

COMPONENTS & PACKAGING

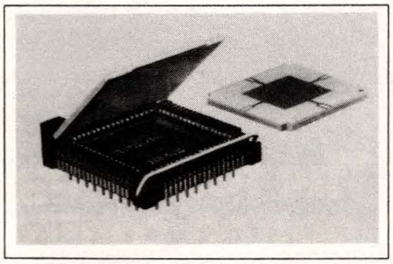


INDUSTRIAL I/O SYSTEM. This high-density power-I/O system consists of universal mounting racks accommodating plug-in ac-input, ac-output, dc-input or dc-output Quad Paks modules. Providing four basic I/O circuits, each color-coded unit features 4000V rms optical isolation. Logic signals are TTL compatible with a nominal 5V dc rating. The ac-output module contains a snubber network; the dc-input module, circuitry to eliminate the adverse effects of contact bounce. Model PB24Q mounting rack holds six modules providing 24 inputs and/or outputs. Furnishing a direct connection to LSI-11 μCs, Model PB32DEC handles as many as eight Quad Paks. Quad Paks, from $40; Model PB24Q, $115; Model PB32DEC, $150. **Opto 22,** 15461 Springdale St, Huntington Beach, CA 92649. Phone (800) 854-8851. **Circle No 292**

F-O CONNECTORS. For single and bundled fiber-cable terminations, these single- and multichannel units feature metal-to-metal coupling that maintains fiber alignment and prevents

fiber separation without wave washers or springs, according to the manufacturer. Insertion losses can spec at ≤2 dB using the company's fiber-optic contacts and appropriate cable. You can make hybrid contact combinations utilizing multichannel connectors and power, coaxial or thermocouple cable. The standard MIL-C-38999 insert pattern is also available. **Bendix Corp,** Electrical Components Div, Sidney, NY 13838. Phone (607) 563-5324. **Circle No 293**

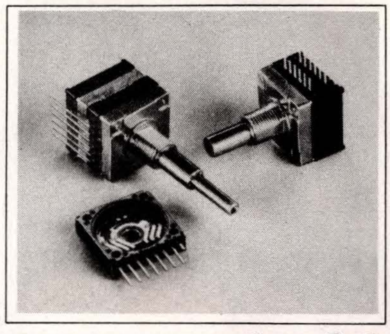
COMPONENTS & PACKAGING



CHIP-CARRIER SOCKET. A 68-lead production/test socket that accepts the JEDEC leadless Type A chip-carrier package, this unit features a socket footprint conforming to the JEDEC standard (0.1×0.1-in. grid). The socket lid can act as a heat sink or can be provided with clearance for a device-mounted heat sink. Other features include 0.342-in. profile for mounting on 0.5-in. centers; 0.015×0.12-in. beryllium-copper contacts; device-to-socket and socket-to-pc-board orientation, external-probing capability and a UL-listed socket-body material. $5.79 (1000) with gold-plated leads. **Textool Products Dept,** Electronic Products Div/3M, 1410 W Pioneer Dr, Irving, TX 75061. Phone (214) 259-2676.

Circle No 290

ROTARY SWITCHES. Sealed against contaminants and solvents used in wave soldering and intended for use in logic circuits, Series 850 programmed sealed 0.85-in.-square units feature life expectancy of 50,000 cycles min and resistance to shock and vibrations. Mounting directly on a pc board, they come with as many as 28 positions, four sections and seven outputs

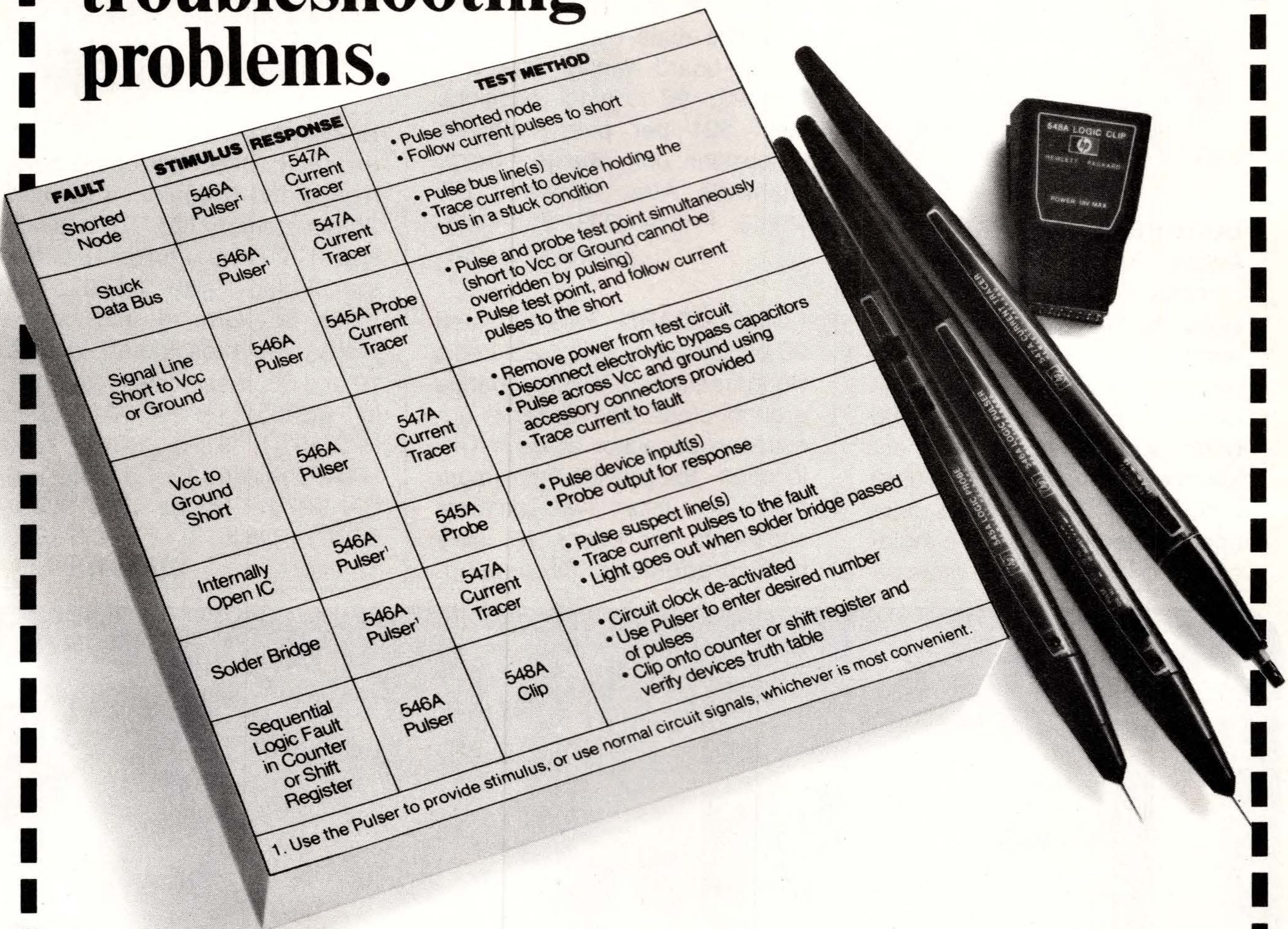


common per section. Both standard and specially coded outputs are available, and mounting can be either parallel or perpendicular to the pc board. Each switch section can be used alone, with as many as three other sections and with or without a housing. $3 (1000) for 1-section, 10-position BCD-coded unit. **Oak Switch Systems Inc,** Box 517, Crystal Lake, IL 60014. Phone (815) 459-5000.

Circle No 291

Mail us this ad

and we'll help you discover simple, effective solutions to difficult troubleshooting problems.



HP's IC Troubleshooters make troubleshooting digital circuits fast and less frustrating. Take a look at the chart and see why more than 50,000 people use these simple, rugged, low-cost Hewlett-Packard instruments.

LOGIC PULSER stimulates IC's in-circuit for testing. Automatically drives the circuit to its opposite state. No unsoldering components or trace cutting. $140-$195*

LOGIC PROBE shows pulse activity: high, low or bad level, single pulse or pulse trains. High input impedance. Overload protected. Automatic. More convenient than a scope. $90-$220*

LOGIC CLIP with 16 LED's display state of up to 16 IC pins at once. High input impedance. Overload protected. Automatic. $145-$200*

CURRENT TRACER inductively senses and displays logic current pulses. Finds shorts and stuck nodes with no unsoldering or trace cutting. Uses in-circuit current or pulses from Logic Pulser. $400*

*Domestic US prices only.

Order now, or call your nearby HP sales office for complete information, or write Hewlett Packard, 1820 Embarcadero Road, Palo Alto, California 94303.

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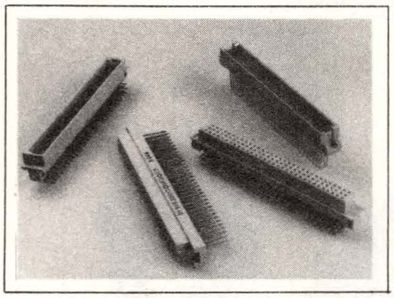
New Products

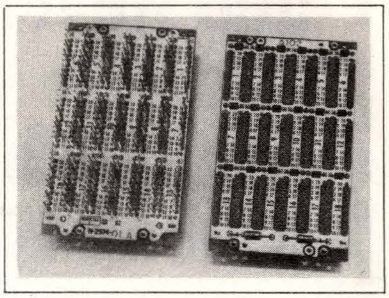
COMPONENTS & PACKAGING



EUROPEAN CONNECTORS. Models P1 and RP1 plug-and-receptacle units are European-standard, 2-piece, high-density pc-board-type connectors. Featuring shock and vibration resistance and low insertion and withdrawal forces, P1 connectors meet VG 95324, DIN 41612 and IEC 130-14 standards (with appropriate plating), come molded in two lengths with 2- or 3-row housings and have contacts spaced on 0.1-in. centers. Contact arrangements of 32, 48, 64 and 96 are available. Model RP1 (reverse P1) is an inverted version of the P1 connector, providing male contacts on the mother-board wiring side and featuring 96 contact positions max. \$21 per pair (100) for 96-position unit. **Burndy Corp,** Richards Ave, Norwalk, CT 06856. Phone (203) 838-4444.

Circle No 268

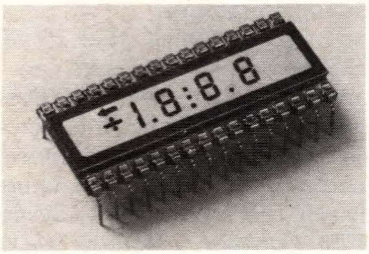
LOGIC BOARD. This UL-listed 20-pin Schottky/utility 2D Logic Board features a low-impedance ground plane and ceramic decoupling capacitor at each DIP location to provide maximum noise immunity. Two tantalum capacitors for every 18 DIPs furnish additional decoupling.



Holding any mix of 14-, 16-, 18- or 20-pin DIPs, the board suits high-speed-Schottky, TTL and 20-pin-memory ICs. The 1-block size (H-2974-01) holds 18 DIPs; the 2-block size (H-2975-01) holds 36. Ground and power planes are presoldered to pins 10 and 20, respectively, for each IC location. H-2974-01, \$92; H-2975-01, \$170. **EECO Inc,** 1601 Chestnut Ave, Santa Ana, CA 92701. Phone (714) 835-6000. TWX 910-595-1550.

Circle No 269

COMPONENTS & PACKAGING



LCD. The 1.6×0.7-in. Model FE2201 features 3½ 0.2-in.-high characters (seven segments), three decimal points, a colon, plus/minus sign and overrange arrow. Designed primarily for multimeters, it comes in transmissive, reflective and transflective modes with either DIP connector pins attached or in a pinless version for use with elastomeric connectors. Operating-temperature range spans −20 to +55°C or −20 to +80°C. Red, blue and green readouts are available on special order. **AND,** 770 Airport Blvd, Burlingame, CA 94010. Phone (415) 347-9916. TWX 910-374-2353.

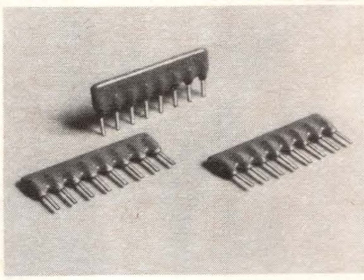
Circle No 270

F-O LINK. Model SPX4101 kit contains all components necessary to construct a dc to 200k-bps 5m digital fiber-optic data link. Included are the manufacturer's Sweet Spot LED and monolithic Schmitt-trigger detector, an AMP Optimate field-appliable connector, Mitsubishi ESKA SH-4001 plastic fiber, pc board and TTL/CMOS driver. The LED furnishes peak output at 820 nm and a spectral bandwidth of 35 nm. No special tools, polishing or adhesive are required for fiber termination. $39.95. **Honeywell Optoelectronics Div,** 830 E Arapaho Rd, Richardson, TX 75081. Phone (214) 234-4271. TLX 730890.

Circle No 271

CONNECTORS. Featuring 10 or 20 contacts, respectively, Type MS 3106A-18-1S and 3106A-28-16S ceramic/metal instrumentation devices have a voltage rating of 700V dc and a current rating to 10A with a 40°C rise in operating temperature. The receptacles can be used in vacuums to $\leq 10^{-10}$ torr, pressures to 100 psig and temperatures from −200 to +450°C; the exterior plug withstands a temperature range of −55 to +125°C. Receptacles come with weldable or vacuum flanges. Standard flange size equals 1.33 in. OD for 10-conductor units and 2.75 in. OD for 20-pin devices. Approximately $200 (100). **Ceramaseal Inc,** New Lebanon Center, NY 12126. Phone (518) 794-7800. TLX 145442.

Circle No 272



RESISTOR NETWORKS. SIP low-profile (0.2-in. max seated height) networks come in environmentally protected conformally coated packages and provide >150 standard 50V dc- or rms-rated versions. Resistance ranges from 47Ω to 1 MΩ with ±2% tolerance standard. TC equals ±200 ppm/°C; TC tracking between resistors, ±50 ppm/°C. Available in 6-, 8- and 10-pin versions, standard circuit configurations include pull-up/pull-down and terminator designs. $0.39 (1000) for typical 8-pin, 7-resistor network. **Centralab Inc,** Box 2032, Milwaukee, WI 53201. Phone (414) 228-7380. **Circle No 273**

F-O CONNECTOR. This fiber-optic SMA-connector system features 1-dB typ, 1.5-dB max insertion loss with 50/125-μm fiber without index-matching fluid. Repeatability equals ±1 dB over 500 rematings. Typical installation time equals 90 sec. Installation requires the manufacturer's Model 92204 cleaving tool and a standard crimping tool. Coupler and two connectors, $120. **T&B Optoelectronics,** 920 Rte 202, Raritan, NJ 08869. Phone (201) 685-1600.

Circle No 274

F-O TELEMETRY LINK. Furnishing a return fiber-optic link that controls input attenuation, calibration and standby functions at the transmitter, this system, manufactured by the English Electro Optic Developments firm, consists of a 20-cm-long×8-cm-dia transmitter unit interconnecting fiber-optic links in lengths to 500m and a receiver/control unit with optional IEEE-488 interface. Transmitter input sensitivity equals 200 μV, system gain specs at 28 dB, total harmonic distortion measures <2% and passband flatness specs at ±0.5 dB. With a heavily shielded battery-operated transmitter and fiber-optic-cable transmission and control links, the system can operate in field strengths to 100 kV/m. $13,900 to $19,100. Delivery, 90 days ARO. **Amplifier Research,** 160 School House Rd, Souderton, PA 18964. Phone (215) 723-8181. TWX 510-661-6094.

Circle No 275

OCTOPLUS

The Sprague Monolithic Arrays That Provide the Muscle of 8 SCRs in a Single DIP.

Sprague UTN-2886B and UTN-2888A SCR arrays are expressly made for use with microprocessors which are strobing power loads. Compatible with TTL, LSTTL and CMOS, they will interface to high-current loads including lamps, relays, and solenoids.

Each array contains eight SCRs with integral current limiting and gate-to-cathode resistors.

The combining of SCRs in one DIP reduces component count, assembly time, and circuit space while improving overall circuit reliability. Each of the isolated devices within the array is capable of continuous and simultaneous operation at 200 mA or 250 mA, at ambient temperatures to +50°C. The arrays operate from an unfiltered half-wave (50 or 60 Hz) or full-wave (100 or 120 Hz) rectified source.

For Engineering Bulletin 29401, write to: ***Technical Literature Service, Sprague Electric Company, 491 Marshall St., North Adams, Mass. 01247.***

For application engineering assistance, write or call Mark Heisig, Don Bird, or Paul Emerald, Semiconductor Division, Sprague Electric Co., 115 Northeast Cutoff, Worcester, Mass. 01606. Telephone 617/853-5000.

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CIRCLE NO 146

Robotic-vision module helps inspect flat parts

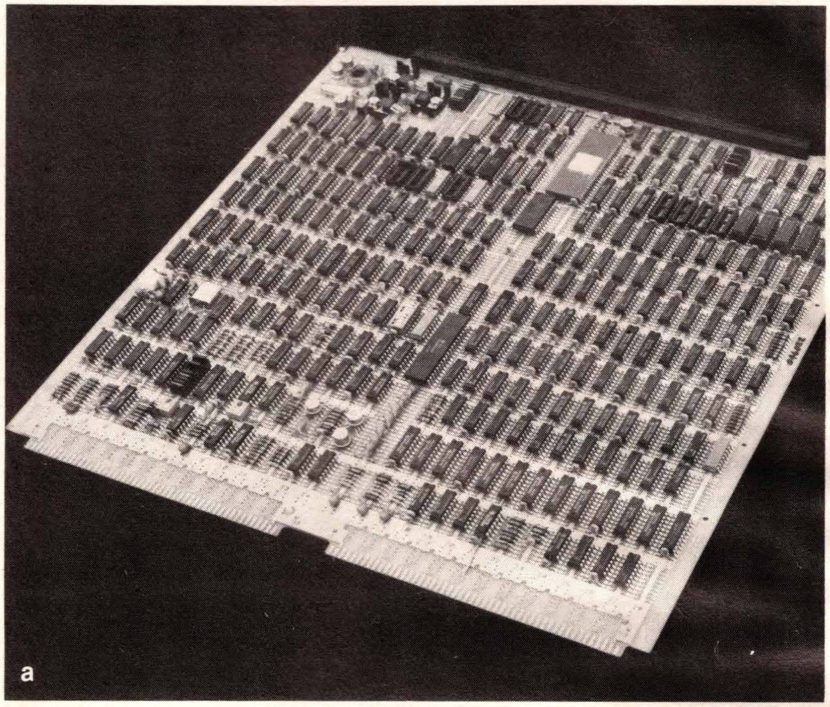
Model 4200 literally provides "eyes" for computerized industrial robots engaged in parts sorting, automated assembly and process control. It visually determines part size, shape, number and orientation, and it can count the number of holes in a part and classify their size characteristics as well. An optional hardware character generator can print all this information on a CRT monitor.

Combines hardware, software

Consisting of a Model 2000 video-image-analyzer board and a Model 1000 FORTRAN-based software package, Model 4200 provides Data General minicomputers with a wide range of high-speed image-analysis, processing and graphics functions. A single 15×15-in. board, it plugs directly into the host's backplane. Indeed, the software makes the module almost immediately operational.

Compatible with EIA RS-170, the module accepts raster-scanned video inputs from standard vidicon or solid-state cameras in real time. In 1/60 sec, it digitizes and stores a full screen of data (320×240 pixels), either as 16 gray-scale levels or 16 RGB colors. Because the software operates on binary (black and white) images, a video-input-translation RAM establishes threshold levels.

After storing the scanned part's data in image memory, an 8X300 μP run-length-encodes the image. Coding speed varies with the processed image's window area. A small window (128×128 pixels, for example)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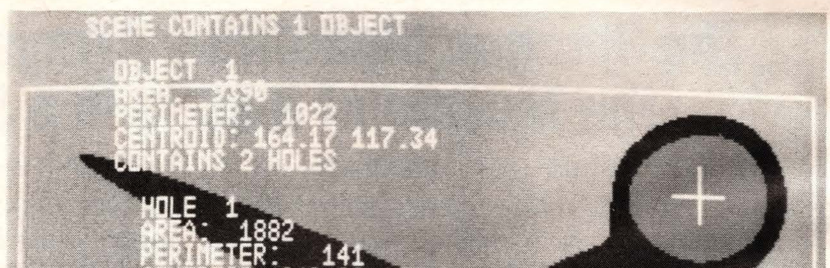
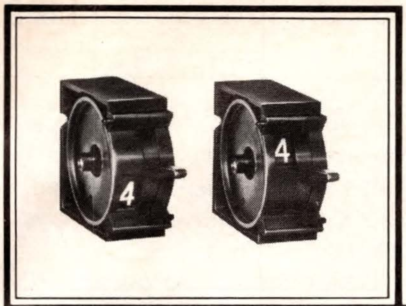
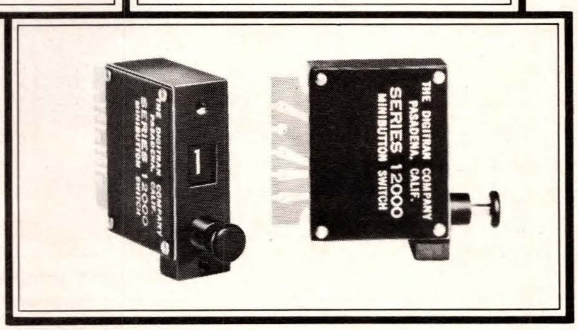


b

Containing all the hardware and software *needed to perform a wide range of video-graphics processing and analysis tasks, the 15×15-in. Model 4200 board* ***(a)*** *plugs into a Data General minicomputer's backplane. It accepts RS-170 standard video inputs and connects directly to common TV monitors. A sample 4200 output* ***(b)*** *shows a pair of scissors digitized to 320×240 resolution. Crosshairs indicate the center of mass as well as the centers of the two holes, and overlayed alphanumerics describe the scissors' key measured parameters.*



Quality at your fingertips



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Switches for every conceivable purpose, with an almost unlimited selection of output codes and options.

Sizes ranging from .315″ to .570″ in width and from .961″ to 2.000″ in height. Large easy-to-read characters, with optional lighting, including LED on some. Environmentally sealed or unsealed.

MIL-SPEC? We set the standards.

Our keypads have great tactile feel and redundant contacts. They're available in 6-, 12-, 16- and 20-key arrays, plus custom configurations for the volume OEM user.

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takes about 0.1 sec; a full screen, 0.8 sec.

Host does final processing

The coded images get processed by the host using connectivity analysis—a method that divides a binary image into its connected components. This analysis consumes 0.17 sec and proceeds in parallel with the run-length encoding. With processing time directly proportional to image area, a 256×256-pixel area thus takes about 1 sec for measurement and display.

The values of key geometric parameters, such as area, perimeter, centroid, moment of inertia, and elongation and compaction indices, are available after object processing. Minimizing the number of parameters that classify a part helps increase inspection speed. \$5148 (100). Delivery, 60 days ARO.

Octek Inc, 7 Corporate Pl, South Bedford St, Burlington, MA 01803. Phone (617) 273-0851. **Circle No 461**

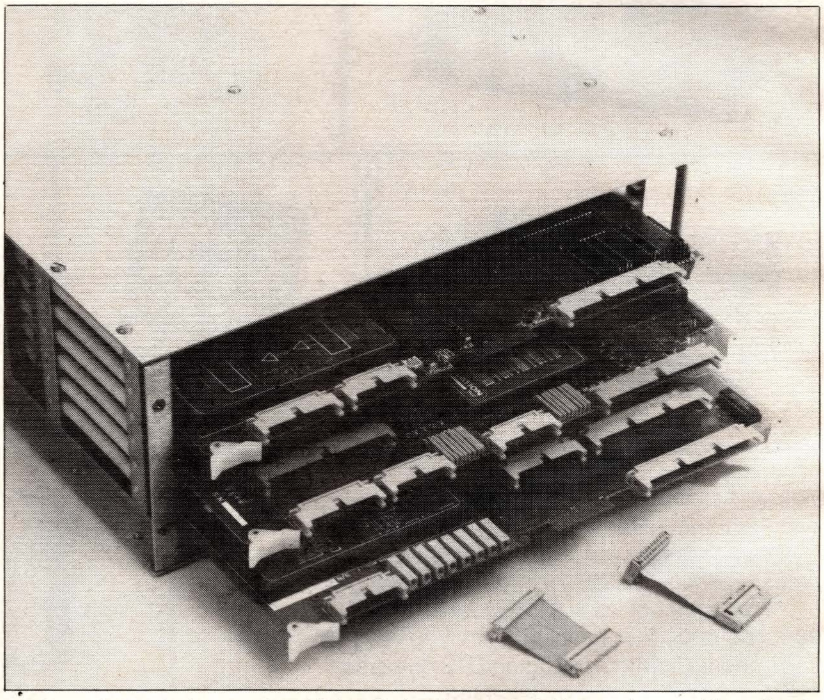
Data-acquisition boards house process-control firmware

Multibus-compatible, Midax Series data-acquisition and control boards come with a system debugger and a ROM-resident firmware package that supports all digital I/O functions. Termed DTFIRM, the firmware package includes industrial and scientific data-handling subroutines and tests, providing an integrated low-cost solution to process-control, machine-control and test-and-measurement applications.

A basic system of two boards contains an 8085A CPU, 24k bytes of PROM, 16 bytes of dual-ported read/write memory, two serial I/O ports, a counter/-timer and frequency I/O measurement section, and 12-bit A/D and D/A converters. A floating-point math processor is optional.

Sixteen single-ended or eight differential analog-input channels furnish software-programmable A/D gain selection. Full-scale input ranges vary from 10 mV to 10V, unipolar or bipolar.

Four D/A-converter outputs support 48 digital output lines. Output ranges cover 0 to 10V and ±10V at ±10 mA. Expansion boards can increase the A/D channels to 64 single-ended or 32 differential and the D/A channels to 44.



µP-based stand-alone units, *Midax Series data-acquisition and control boards can perform independent process-control and measurement tasks. With its dual-ported memory structure and on-board DTFIRM software, a board can alternatively function as an intelligent slave to a host computer on the Multibus.*

Models DT302 and DT304 offer nonisolated and low-level voltage inputs, respectively. Model DT305 provides isolated inputs with ±250V common-mode capability. \$4295.

Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. Phone (617) 481-3700. **Circle No 462**

A LITTLE GOOD NEWS FOR DATA GENERAL OEMS.

Look what we've put together for you. A desk top computer that doesn't take up the whole desk.

It's called MPT.

And look what's inside this little thing; a 16 bit microNOVA™ computer. 60 K bytes of memory. 80 column by 25 line screen. Full keyboard with 10-key numeric pad. And up to 716 KB of on-line storage on two 358 KB mini diskettes. (Also available with one diskette. Or none.)

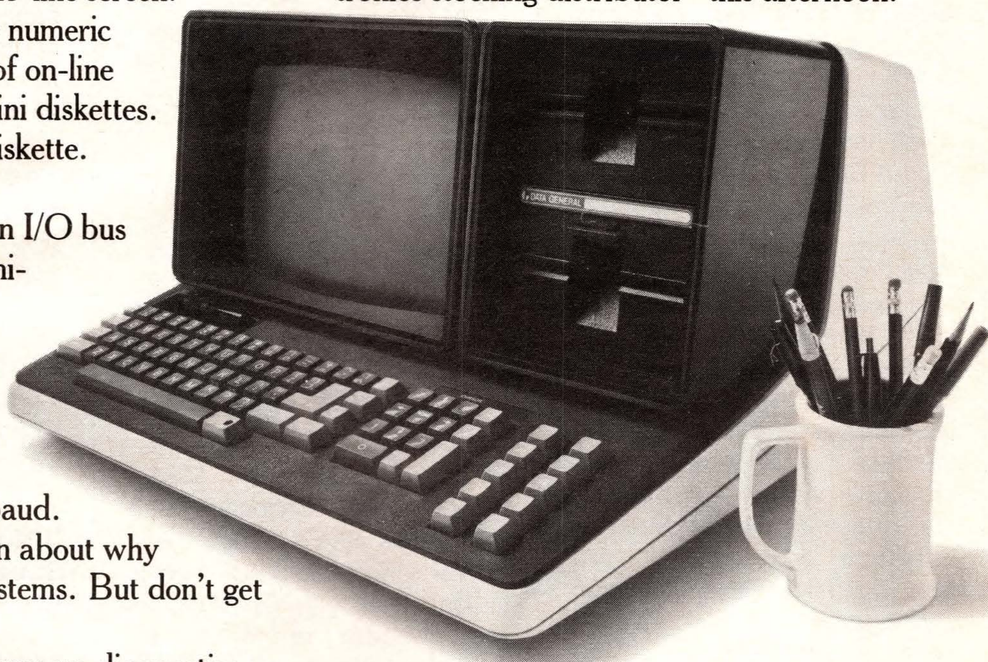
Out back you'll find an I/O bus that accepts the standard microNOVA peripherals. As well as your own interfaces. And two synchronous/asynchronous communications ports, programmable to 19.2K baud. Standard. (We could go on about why that's an option on other systems. But don't get us started on that.)

Also standard are power-up diagnostics that check out the whole system before it accepts your diskettes. So you and your software shouldn't be accused of hardware problems.

MPT is upwards compatible with the microNOVA, NOVA® and ECLIPSE® computers you're probably using now. And because it uses a run-time version of MP/OS, you're going to be able to develop your software with your MP/OS and AOS operating systems. In PASCAL, FORTRAN, BASIC.

You can get to work on your MPT software now. By calling your local Data General sales office. Or writing us at MS C-228, 4400 Computer drive, Westboro MA 01580.

Or if you really want to move, you can pick one up at your local Data General industrial electronics stocking distributor* this afternoon.



You'll find MPT very easy to take. Partly because of the $4071 price (USA price, 2 diskette version, OEM quantity 20). And partly because the whole thing weighs just 30 pounds.

Remember when you decided to become a Data General OEM? That was a very intelligent decision on your part.

MPT is good news for every Data General OEM. And bad news for those who are not.

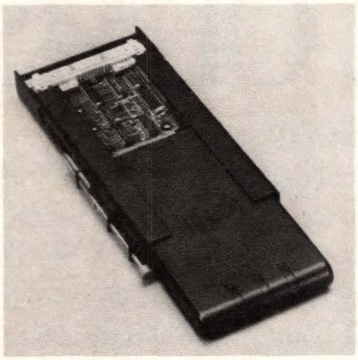
Data General
We take care of our own.

*SCHWEBER, HALL-MARK, KIERULFF, ALMAC/STROUM, and in Canada, R.A.E. and FUTURE.

CIRCLE NO 147

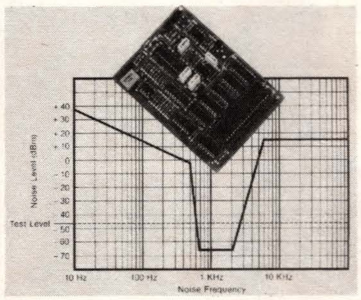
New Products

COMPUTER-SYSTEM SUBASSEMBLIES

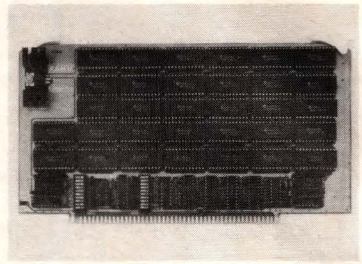


BUBBLE MEMORY. Featuring removable bubble cassettes designed to provide compact permanent memory storage in harsh environments, the basic Plug-A-Bubble iPAB system consists of a 128k-byte bubble-memory cassette and holder. Optional are a chassis housing two cassette holders and an iSBX bus-interface card with cabling. The chassis fits into the same space as a 5¼-in. floppy disk; the cassette and holder can interface directly with the iSBC processor via the iSBX bus or can attach to a user-designed interface. Housed in a 1×3.8×7.75-in. cast-aluminum cartridge, the bubble cassette contains its manufacturer's 7110 1M-bit bubble-memory unit plus the 7220 controller and other bubble support chips and provides 48-msec average access time and 12.5k-bytes/sec burst data-transfer rate. $2550; chassis, $810; bus interface $265; additional cassettes, $1915 (100). **Intel Corp,** 1302 N Mathilda Ave, Sunnyvale, CA 94086. Phone (408) 734-8102. **Circle No 244**

OPERATING SYSTEM. Providing a CP/M-compatible interface to its manufacturer's MDX- or SD Series board-level μC components, M/OS-80 supports all CP/M system calls. Additional features not usually provided by CP/M include the ability to designate a master library disk, file expansion beyond the 256k CP/M limit to >65M bytes, random-file-accessing techniques, file-protection attribute bytes, direct access to a system clock and interrupt handling. The system also furnishes >14 utility programs not offered by CP/M, including a System Spooler program. $199 on diskette, with bootstrap PROMs, $249. **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006. Phone (214) 323-6000. **Circle No 245**

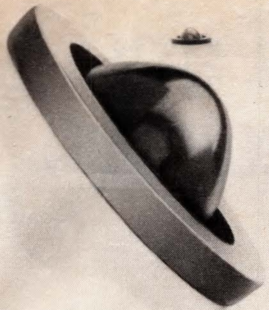


DTMF RECEIVER. Model M-937, when connected to a telephone line's voice pair, converts incoming DTMF signals to logic-level outputs. Used as the decoder in telephone-switching equipment, it counts rotary dial pulses. Dynamic range specs at −45 dB, and sensitivity is externally adjustable from −46 to −20 dBm. Meeting CEPT, CCITT and USITA central-office recommendations for DTMF receivers, the 4.5×3.3×0.7-in. card provides selectable output formats, including binary, 2-of-8 (2-of-7), 1-of-12 or blank. Additional outputs include valid data strobe and dial-pulse and DTMF-mode indications. $115 (10). **Teltone Corp,** Box 657, Kirkland, WA 98033. Phone (800) 426-5918. TWX 910-449-2862. **Circle No 246**



RAM BOARD. A 64k fully static memory board for S-100/IEEE-696 computers, RAM 17 can run with 6-MHz Z80s and 10-MHz 8086/88s, features <2W dissipation and DMA operation and provides freedom from alpha-particle soft-bit errors. Meeting all IEEE-696 specs including 24-bit addressing (permitting 16M bytes max of system memory), it can be addressed on any 64k-page boundary and disabled in 16k blocks. The upper 8k block can also have 2k windows disabled to allow for memory-mapped peripherals. Kit, $1095; assembled, $1395. **CompuPro,** Box 2355, Oakland Airport, CA 94614. Phone (415) 562-0636. **Circle No 247**

SPEECH SYNTHESIZER. Speaking as many as 255 utterances (sentences, phrases, words and phonemes), the TDS910 accepts 1-of-16 switch-closure, parallel 8-bit-binary or serial-ASCII input. Three on-board 32k EPROMs or ROMs in a typical system can provide a 70-word output, but external expansion to >1M bytes of speech-parameter storage is possible. Custom vocabularies (in PROM) can also be furnished based on a user-supplied cassette. The unit comes with an audio amplifier. $395; standard-vocabulary ROM (numbers, five words), $95. **Stynetic Systems Inc,** Flowerfield, Bldg 1, Saint James, NY 11780. Phone (516) 584-5596. **Circle No 248**



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It's only because we've had other important things to talk about—like how our Variable Height Brite-Lites are visibly brighter and how our Super Brite-Lites give you 25 times more brightness.

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CIRCLE NO 148

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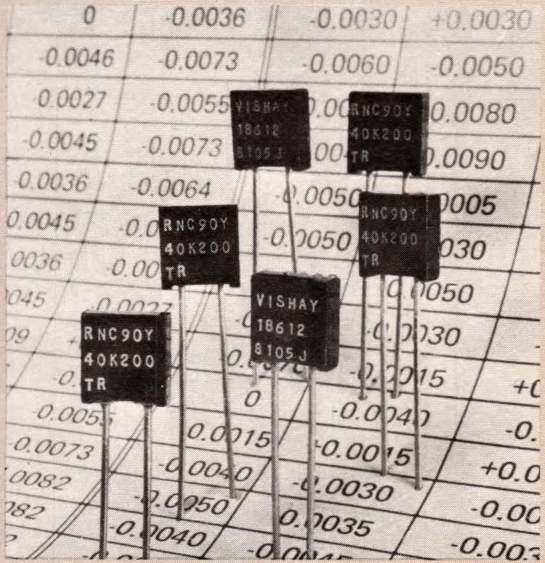
It takes superior performance to achieve "R" level reliability in a precision resistor



. . . and Vishay does it.

For critical military and industrial applications, Vishay's RNC90Y-S555 is rated at "R" level reliability for values up to 40.2K ohms and at "P" level up to 100K ohms. (Based on specification MIL-R-55182/9c for established reliability precision resistors).

Compare these standard specifications:

- **Resistance tolerances:** ±0.005% to ±1.0%
- **Load life stability:** 0.05% Δ R (0.3 watts @ +125°C)
- **Rise time:** 1 ns
- **Current noise:** <0.025μ V (RMS)/volt
- **Thermal EMF:** 0.05μ V/°C
- **Voltage coefficient:** <1ppm/volt

For more details on Vishay's precision resistors, write

Vishay Resistive Systems Group
of Vishay Intertechnology, Inc.
63 Lincoln Highway, Malvern, PA 19355
or call
(215) 644-1300

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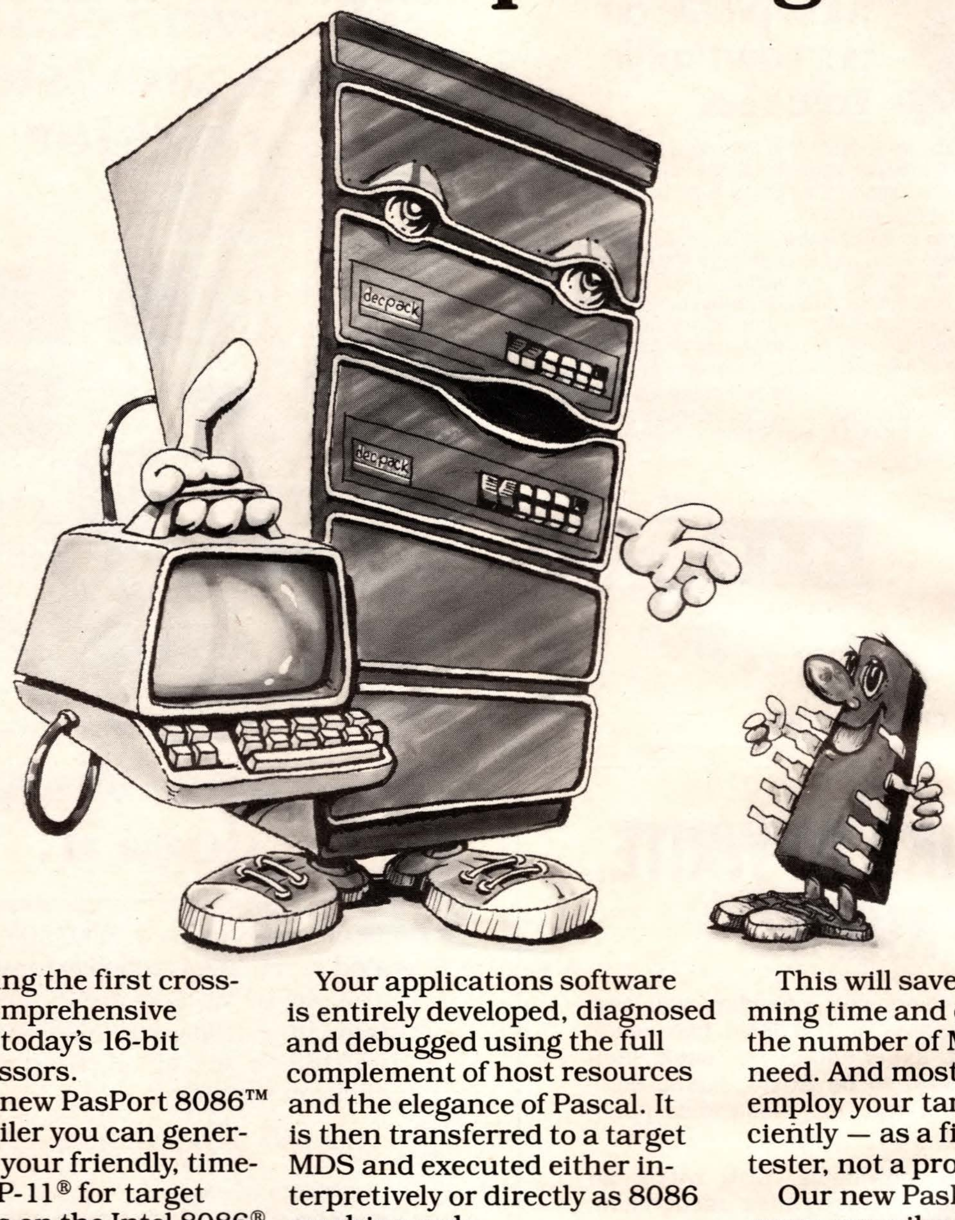

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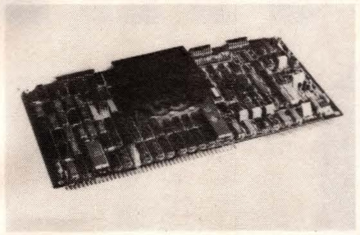
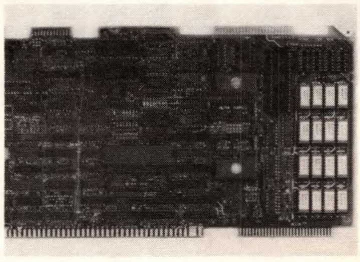
CIRCLE NO 151

New Products

COMPUTER-SYSTEM SUBASSEMBLIES



DISK-DRIVE CONTROLLER. A single-board unit compatible with the Multibus host interface, MSC-9205 is based on its manufacturer's MSC 9000 Series module, which provides data-buffering and error-correction functions for 5¼- or 8-in. Winchester drives. The controller supports 20-bit addressing and furnishes 8- or 16-bit DMA data transfer, DMA command transfer and 8080 and 8086 compatibility. Alternate sectoring on each track, variable interleaving, 22-bit error detection and 11-bit error correction, data separation, automatic position verification and automatic retry are also featured. $795. **Microcomputer Systems Corp,** 432 Lakeside Dr, Sunnyvale, CA 94086. Phone (408) 354-0536. **Circle No** 249



COMPUTER BOARDS. These 16-bit single-board computers with 128k bytes max of on-board RAM can run large programs at 8 MHz with no Wait states on a card that conforms to the Multibus form factor. Units in the CPC 86 Series come in 5- or 8-MHz 8086-CPU versions with 128k or 32k bytes of on-board RAM or without RAM. The boards and software are compatible with Intel's SBC 86/12A and the manufacturer's DEBUG 86 and RS 86 support packages. Other features include a serial port and 24 parallel programmable I/O lines and sockets for 32k max of EPROM using 64k EPROMs. GPC 86-532 (5 MHz, 32k RAM), $1845; GPC 86-5128 (5 MHz, 128k RAM), $2695; 8-MHz versions, $2095 and $2925, respectively. **Microbar Systems Inc,** 1120 San Antonio Rd, Palo Alto, CA 94303. Phone (415) 964-2862. **Circle No** 253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GPD Box 65, Shawsheen Village Station, Andover, Mass 01810.
Telephone: (617) 475-5982. Telex: 94-7150 GPD Andr.
CIRCLE NO 153

New Products

COMPUTER-SYSTEM SUBASSEMBLIES

BUBBLE-MEMORY BOARD. Billed as the smallest available bubble-memory subsystem, the <11-in.[2] BLX-9252 operates at low power levels (<5W, operating), is BLX/Microbus compatible and provides for incremental on-board expansion. Featuring 32k bytes of nonvolatile storage and upwardly compatible with the 1M-bit BLX-9012 version scheduled for release later this year, it can detect as many as three random errors or a 12-bit error burst and correct any error bursts up to three bits long. <\$1000 (100). Delivery, 4 to 6 wks ARO. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051. Phone (408) 737-6285. TWX 910-339-9240.

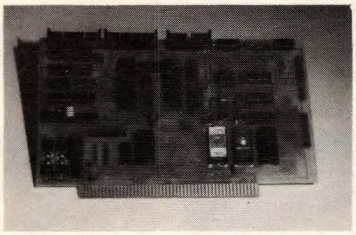
Circle No 254

CONTROLLER. A single-board system featuring a Motorola 6809 μP, Model ACS 09 offers five 28-pin sockets for installing 8-bit-wide memory circuits and a software-controlled ACIA/modem serial port with RS-422 or RS-232C signaling. Supporting memory-mapped addressing by means of a PROM and I/O-page STD Bus signaling, it conforms to all STD Bus mechanical standards and provides an STD Bus 56-pin connector. The ACS 09-OEM comes with sockets only; the ACS 09-PRO version is supplied with the manufacturer's D-FORTH in EPROM and one 2k×8 RAM installed. ACS 09-OEM, \$295; \$345 with 2k of RAM; ACS 09-PRO, \$395. Delivery, stock to 6 wks ARO. **Datricon Corp,** Suite 200, 7911 NE 33rd Dr, Portland, OR 97211. Phone (503) 284-8277.

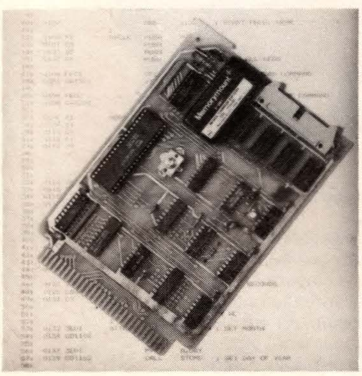
Circle No 255

New Products

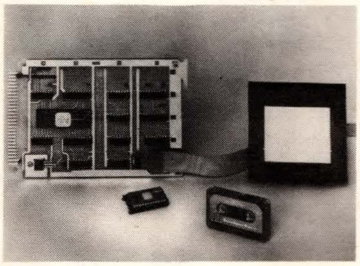
COMPUTER-SYSTEM SUBASSEMBLIES



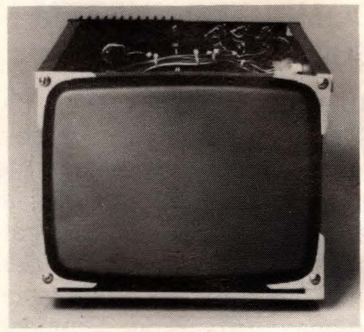
μC CARD. Based on the 6809 μC, the QCB-9 for S-100-bus systems includes a floppy-disk controller capable of handling as many as three single-sided, single-density mini-floppy drives. It also features an RS-232C serial port with 14 user-selectable baud rates, two 8-bit parallel ports, byte-wide memory capability and three 28-pin sockets for up to 24k bytes of EPROM or 12k bytes of RAM. Accepting all JEDEC-standard-pinout memory ICs, the board provides I/O addressing and on-board power regulation. $395 for 2k-EPROM, 1k-RAM version. **Logical Devices Inc,** 781 W Oakland Park Blvd, Ft Lauderdale, FL 33311. Phone (305) 565-8103. **Circle No 256**



CLOCK/CALENDAR. In addition to furnishing STD Bus systems with a completely programmable crystal-controlled clock/calendar, Model ANC-7332 provides two parallel programmable I/O ports. Output can be seconds, minutes, hours (12 or 24), day of week, date, month and year. Other features include battery-backup operation for 5 months (with on-board trickle charger); leap-year identification; power-failure interrupt generator with user-selectable voltage threshold; and real-time user-selectable interrupt generator for 1024-Hz, 1-sec, 1-min or 1-hr time intervals. A user-selectable I/O-port address is also included. $197. **Antona Corp,** 13600 Ventura Blvd, Suite A, Sherman Oaks, CA 91423. Phone (213) 986-6651. **Circle No 257**



CASSETTE CONTROLLER. Mating a Braemar CM-600 digital minicassette transport (or other unit) to a Z80 STD Bus system, the CCB-1 board uses a 2716 EPROM to provide compatibility with the Mostek DDT-80 ROM-based operating system. Plugged into the CPU board or auxiliary memory board, the EPROM redirects the paper-tape I/O without changing the Mostek output commands. Features include capability for as many as 20 files per minicassette and 18k bytes of formatted storage, error checking, 11 tape commands, CRC and user-selectable functions that include selection of I/O port addresses and read-after-write operation. $280, including EPROM and manual. **Tektronics,** 322 E Deepdale Rd, Phoenix, AZ 85022. Phone (602) 866-1926. **Circle No 258**



MONITOR. Sporting a 9-in.-diagonal CRT, Model 1955 features magnetic deflection for improved point-by-point image construction, vertical sensitivity adjustable from <1.5 to >150V for 18-cm deflection and dc to 15-kHz vertical bandwidth. Horizontal sensitivity is adjustable from <1.8 to >150V for 24-cm deflection; horizontal bandwidth equals dc to 1.5 kHz. P4 white phosphor is standard, but other phosphors are also available. $575. Delivery, 4 to 6 wks ARO. **Wavetek Indiana Inc,** Box 190, Beech Grove, IN 46107. Phone (317) 787-3332. TWX 810-341-3226. **Circle No 259**

DISPLAY CONTROLLER. STD Bus compatible, the 7911/HDC Hex Display Controller is an I/O-mapped card that automatically decodes, drives and multiplexes as many as 17 digits of hexadecimal information on a remote display as far as 6 ft away. Operating as write-only memory and occupying 16 I/O-mapped address locations, it can be addressed to any $X0 base address by on-board switches. 12 data registers are organized as two groups of six; the remaining four registers are used for display blanking. A decimal-only version furnishes special-symbol displays and digit blanking. $133 to $190 (100). **Matrix Corp,** 1639 Green St, Raleigh, NC 27603. Phone (919) 833-2837. **Circle No 260**

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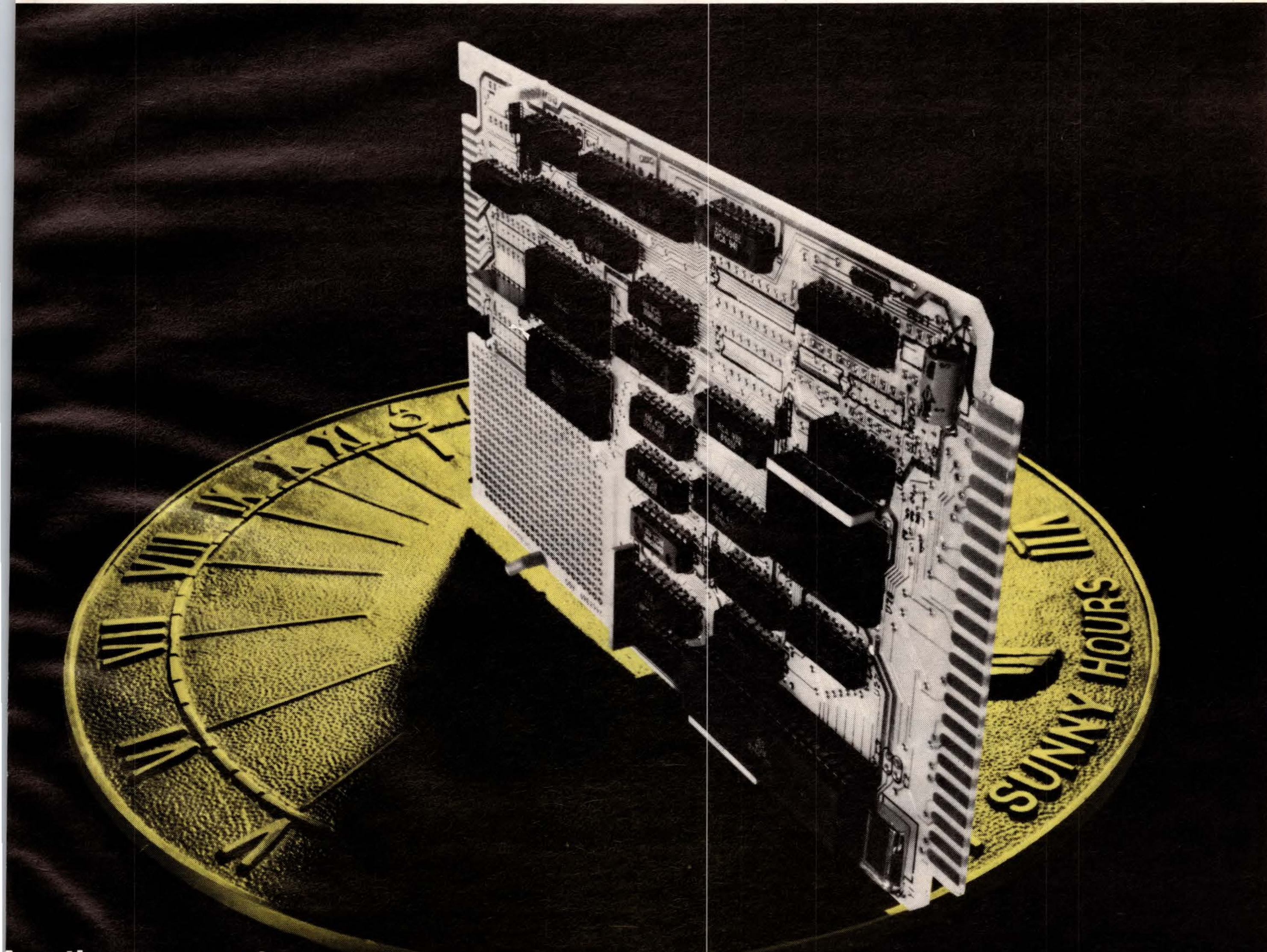


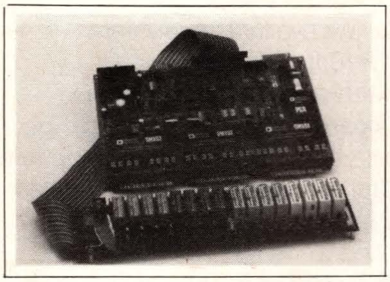
Another reason to switch to CMOS.

CIRCLE NO 156

RCA

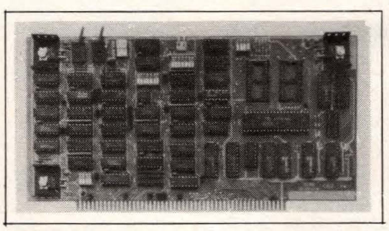
New Products

COMPUTER-SYSTEM SUBASSEMBLIES

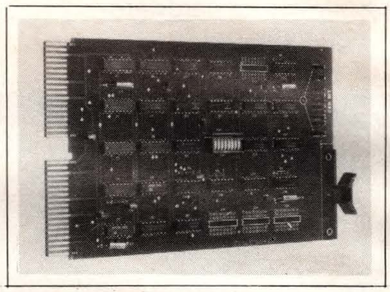


DIGITAL-I/O SUBSYSTEM. A 16-channel unit, µMAC-4020 interfaces with its manufacturer's µMAC-4000 single-board measurement and control system. It provides eight input and output channels and a selection of plug-in ac and dc input and output modules. The modules convert high-level ac/dc inputs/-outputs to TTL levels and feature optical isolation to 2500V ac rms, individual plug-in fuses for high voltage surge- and short-circuit protection and LED status lights. AC modules incorporate zero-voltage switching, can sense or switch ac voltages of 90 to 140V or 180 to 280V and have a 3A current rating. DC modules include contact-debounce circuitry; dc signals can be 60V on the output and 10 to 32V on input. $139; modules, $22 or $24. **Analog Devices Inc,** Box 280, Norwood, MA 02062. Phone (617) 329-4700.

Circle No 261

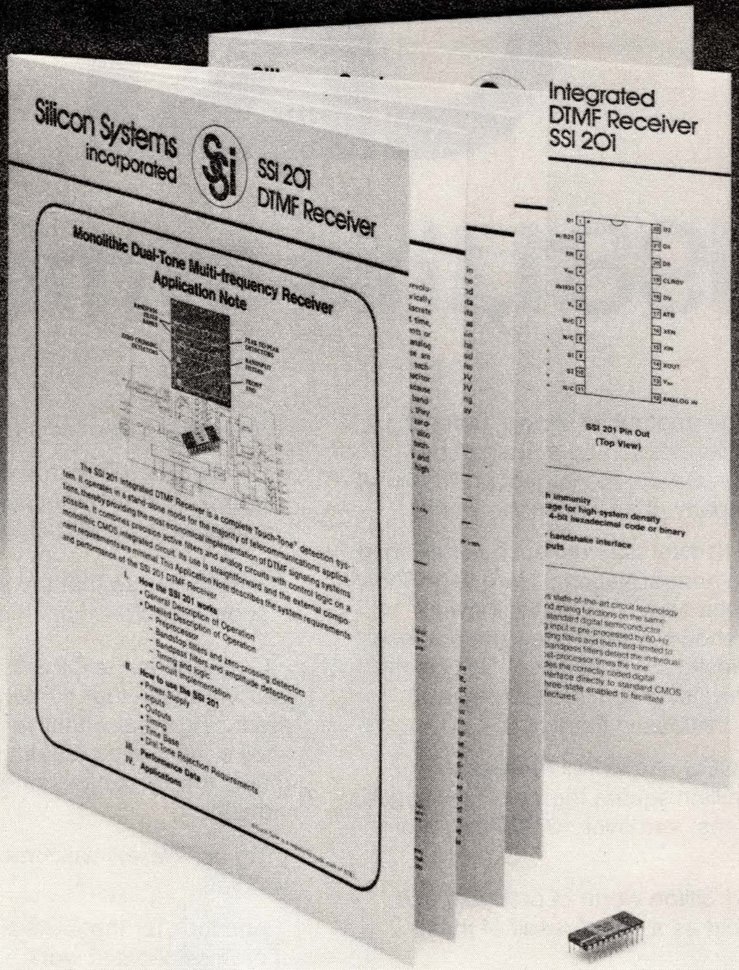


CPU BOARD. For S-100 systems, the Z80 based Model CB2 operates at 2 or 4 MHz (DIP-switch selectable) and includes sockets for two 2716 or 2732 EPROMs or HM6116 2k RAMs. Run/stop and single-step switches permit system evaluation without the need for a front panel. Firmware vector jumps and an output port to control eight extended address lines allow use of >64k of additional memory. The 2048/4096×8-bit EPROMs or the 2048×8-bit RAM can be DIP-switch addressable or disabled. $344; kit, $260. **SSM Microcomputer Products,** 2190 Paragon Dr, San Jose, CA 95131. Phone (408) 946-7400. **Circle No 262**



LOGIC MODULES. For DEC LSI-11 µCs, Model P03 parity controller and Model BT03 bootstrap module are packaged on dual boards. The parity controller operates with any LSI-11-compatible memory module with an 18-bit word length and in systems with 4M bytes max memory storage. It contains a control and status register with switch-selectable address; contents are continuously displayed on LED indicators. The bootstrap module provides space for a 32×16 PROM array, which can be located in one of two switch-selectable address ranges in the upper 4k I/O address bank. A clock-status register permits program control of the line time clock. Parity controller, $300; bootstrap module without PROMs, $200; with PROMs, $250. **Dataram Corp,** Princeton Rd, Cranbury, NJ 08512, Phone (609) 799-0071. TWX 510-685-2542. **Circle No 263**

THE STANDARD ONE-CHIP SOLUTION FOR DTMF RECEIVER APPLICATIONS



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A Question of Law

Edited by Jesse Victor

US Supreme Court partially opens door to patenting of computer programs

David Pressman, Attorney at Law
San Francisco, CA

Although computer software has become one of the fastest growing, most important and most innovative areas of electronics, the US Patent and Trademark Office has in the past rejected almost any patent claim that contained a computer program, contending that a program or algorithm, like a mathematical formula, is based on a law of nature and hence unpatentable. And several federal-court decisions have indirectly sustained this position, holding not that a computer program is *essentially* unpatentable, but that it does not constitute patentable subject matter.

However, in two recently decided and sharply divided cases, the US Supreme Court has opened the door to the patenting of computer software by substantially broadening the rights of inventors to obtain patents on computer-program-related processes and inventions. And although the two rulings are a long way from a blanket endorsement of software patents, many patent lawyers feel that the decisions will effectively permit patenting of most computer programs, *provided they are claimed in association with hardware.* The two decisions will also provide much-needed guidelines to the Patent Office and, it's hoped, help reduce the current backlog of approximately 3000 pending computer-program-related patent applications.

Computer controls rubber-molding process

The first of the Court's two decisions, *(Diamond v Diehr and Lutton),* decided March 3, involved a suit brought by Federal-Mogul Corp of Detroit against Sidney A Diamond, US Commissioner of Patents and Trademarks. Two of the company's employees, Diehr and Lutton, had invented a process for molding rubber, using a computer to calculate the precise time that the heated mold should be opened.

The optimum time, temperature and other key parameters relating to the molding process were not new developments; they have been well known in the industry for some time and governed by an industry-standard equation. Diehr and Lutton's contribution, however, involved the continuous measurement of mold temperature and the use of a computer to repeatedly calculate the optimum molding time and automatically open the mold at the correct time.

In 1975, the Patent Office rejected the Diehr-Lutton patent application, and the decision was affirmed by the Patent Office Board of Appeals. Both the Patent Office and the Board of Appeals contended that the Diehr-Lutton application sought protection for a computer program, which had been held nonpatentable subject matter by earlier Supreme Court cases.

Federal-Mogul appealed the Patent Office's decision to the Court of Customs and Patent Appeals (CCPA). The Court reversed the decision and ordered the Patent Office to approve the Diehr-Lutton application because it claimed a rubber-molding process and not a computer program as the patentable subject matter. The Patent Office (with the assistance and concurrence of the US Dept of Justice) then appealed the verdict to the US Supreme Court, which upheld the CCPA's decision in a narrowly decided 5-to-4 decision. (The majority opinion was written by Justice Rehnquist and concurred in by Justices Burger, Stewart, White and Powell. A strong, lengthy dissent was written by Justice Stevens and concurred in by Justices Brennan, Marshall and Blackmun.)

Supreme Court holds invention patentable

The Court's majority held that the inventors were not attempting to patent a mathematical formula or a set of instructions for a computer but rather a rubber-molding process. The Court further ruled that even though Diehr and Lutton's patent claims involved an equation and the use of a computer for solving the equation, the fact that the claims also specified the molding process itself, the temperature monitoring and the opening of the molding press brought the invention into the protectable realm.

The Court's dissenters countered that the invention's only novelty was the use of a computer to solve the molding-process equation. They further contended that the present case differed from an earlier 1978 Supreme Court case *(Parker v Flook),* which had upheld the Patent Office's refusal of a patent, solely in the way the claims were drafted. The dissenters thus argued forcefully that had Flook merely drafted his claims to include a computer-related process or apparatus as did Diehr and Lutton, he would also have been awarded a patent under the majority's reasoning.

Because the Court's majority, however, did not address this latter point, the solution for computer-program-related patents is clear to many patent attorneys: If you claim computer-related inventions along with the process or apparatus used with the computer program, the claim will be held to be patentable subject matter, provided it defines an invention meeting the usual requirements of patentability.

The second Supreme Court case *(Diamond v Bradley)*, decided March 9, involved two Honeywell Information Systems employees, Bradley and Franklin. Their 1975 patent application sought to protect a "computer data structure" for transferring information from a computer's scratchpad memory (in its CPU) to the main memory, so that the scratchpad's information would become accessible to a programmer. The invention consisted of a firmware module for directing data transfers back and forth between the scratchpad and main memory.

Patent Office rejects Bradley-Franklin application

The Patent Office examiner and the Board of Appeals held that the Bradley-Franklin patent application centered on a combination of known hardware plus an algorithm for controlling the hardware. The Patent Office therefore contended that the algorithm was the invention's only novelty, and it rejected the application as thus directed to nonstatutory (ie, unpatentable) subject matter.

Honeywell appealed to the CCPA, which unanimously reversed the Patent Office, holding that the Bradley-Franklin invention centered on a combination of hardware, and hence patentable subject matter, and not on an algorithm. The Patent Office again appealed the case to the Supreme Court, where a tie (4-to-4) vote resulted (one Justice of the Diehr-Lutton case's majority abstained, evidently because of a conflict of interest). The Supreme Court in effect, then, took no affirmative action on the case, letting the CCPA's decision stand by inaction.

It seems clear in this case, as in the Diehr-Lutton application, that Bradley and Franklin succeeded because the patent attorney who drafted their claims cited enough hardware (the computer memories and the means or method for shifting the data between them) to convince the judges that their invention centered on patentable subject matter.

Two grounds for opposing software patents

The Patent Office's basic reluctance to patent computer programs probably rests primarily on practical grounds: its fear that patenting software would lead to a tremendous increase in workload without a concomitant increase in funding by Congress. But practical considerations aside, the patent law itself states (Sections 100 and 101): "Whoever invents or discovers any new and useful process ["process" includes new uses of old inventions], machine, manufacture, or composition of matter ...may obtain a patent." And most intelligent people

Electronics industry cool to Supreme Court decisions

Electronics-industry reaction to the recent Supreme Court decisions on computer patents has been decidedly mixed.

Bell Telephone Laboratories' lawyers reacted favorably to the Court's rulings. A strong advocate of patents for computer-implemented systems, Bell Labs will reinforce its patent efforts as a result of the rulings, predicts general legal and patent counsel Seymour E Hollander.

The decisions, however, have met with far less enthusiasm from some other major electronics firms, which will continue to rely on trade-secret contracts (EDN, May 13, pg 215, May 27, pg 271 and June 10, pg 255) and copyrights for software protection.

Xerox Corp will continue to depend heavily on trade-secret protection. Comments corporation patent attorney Ron Zibelli: "I can't say I'm ready to commit the resources of the company [to patenting software] on the basis of these two cases."

IBM Corp, on the other hand, relies more heavily on copyrights for software protection, a course that could be eased by recent amendments to the patent/copyright law (see pg 133 in this issue). "We believe the copyright is the best program-protection mechanism," a company spokesman says. "It is simple to obtain, easy to enforce and provides appropriate protection."

Relying strongly on trade-secret protection, Intel Corp sees little reason to change its policy. Contending that the Supreme Court's two decisions have not changed the law regarding software patents, general counsel Roger Donovoy summarizes the justices' decision as: "if an invention is patentable anyway, we won't throw it out merely because it uses programs."

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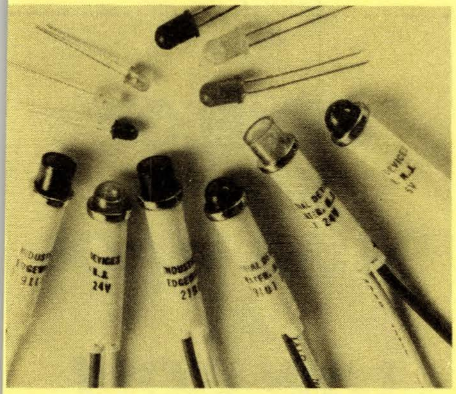

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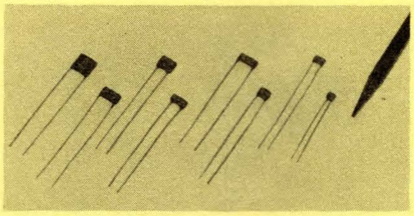

MONOLYTHIC® CERAMIC CAPACITORS. Type 1C through 5C reliable resin-coated capacitors now available in broad range of capacitance values, voltage ratings, and sizes. Time-proven layer-built construction with temperature characteristics C0G, X7R, and Z5U. Write for Bulletin 6201G. **Sprague Electric Co.,** 491 Marshall St., North Adams, Mass. 01247. (413) 664-4411.
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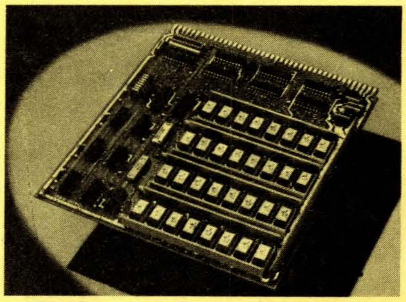

When should you use Mini/Bus®?
Board is crowded, you need more room for signal interconnections, want to avoid multi-layers. Use MINI/BUS® PC board bus bars.

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Chandler, AZ 85224
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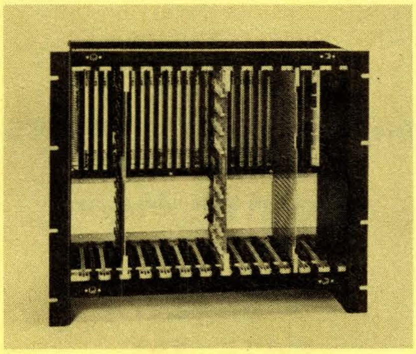

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G.U.C. PRODUCTS
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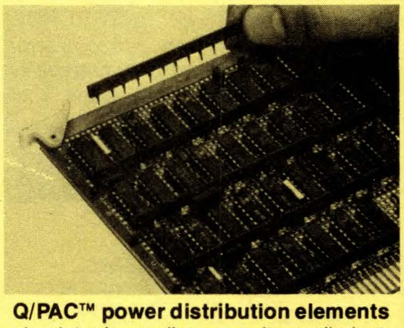

Q/PAC™ power distribution elements obsolete decoupling capacitors, eliminate on-board power and ground traces and extra board layers. Q/PAC elements maximize packaging density; minimize signal interconnection problems. Capacitance values to 0.05 μf per inch; lengths to 16". Contact Q/PAC product specialist at ROGERS CORPORATION, Chandler, AZ 85224, (602) 963-4584. EUROPE: Mektron N.V., Gent, Belgium JAPAN: Nippon Mektron, Tokyo.
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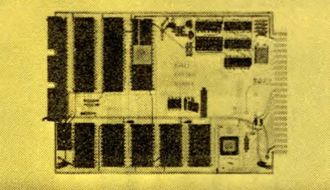

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6800 MPU, serial I/O, parallel I/O, RAM, EROM, 44-pin 4½" x 6½" PCB

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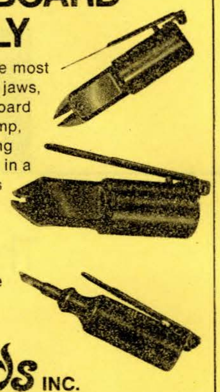

Simonds Inc. offers the most complete line of tools, jaws, and die sets for P.C. Board processing. Cut & Crimp, Cut & Bend, and Cutting Dykes are all available in a wide variety of shapes and working angles. Trimming and forming die sets are also available for further lead processing. Write for FREE catalog today.

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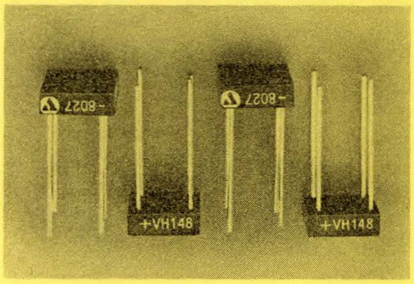

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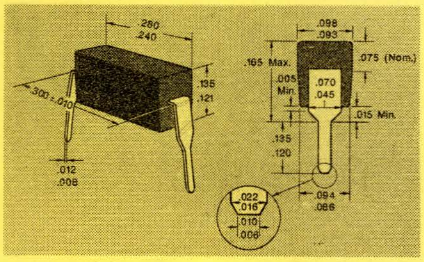

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A Question of Law

find it incomprehensible that a program, or a programmed machine, should not automatically be regarded as a "process" or "machine."

The Patent Office's theoretical grounds for rejecting computer-program patents has rested on its position that laws of nature, mental processes, physical phenomena and abstract ideas have been held not to be processes (in the sense of Sections 100 and 101) and hence are not patentable. Thus, because a computer program is basically an algorithm, and an algorithm is similar to a law of nature or mental process, it also is not patentable.

Before these latest decisions, two previous Supreme Court decisions have upheld the Patent Office's reasoning. In *Gottschalk v Benson* (1973), an algorithm for converting BCD numbers to binary form was refused protection. And in the aforementioned *Parker v Flook*, claims to a process for computing an alarm limit were also refused.

Hardware is the key to patent approval

Despite such adverse Supreme Court decisions and the Patent Office's past reluctance to approve patents for computer software, the Court's two recent decisions seem to provide a feasible way of patenting computer programs, provided that some hardware can be associated with the programming steps.

But don't expect a flood of software-patent approvals to follow. Computer programs, per se, are not yet patentable. And the Court has decided only two cases on limited grounds.

Therefore, in view of the closeness and narrowness of the Supreme Court decisions and the Patent Office's continuing antiprogram attitude, legislation from Congress would clearly seem to be required to unambiguously settle the issue of software patents. EDN

David Pressman, JD, BSEE, received the Juris Doctor degree from George Washington University and a BSEE from Penn State University. A member of Eta Kappa Nu and Sigma Tau, he is registered to practice before the US Patent and Trademark Office, is a member of the California and Pennsylvania Bar Associations and is on the Board of Directors of the California Inventors Council. Formerly a field engineer at Philco-Ford Corp, a patent examiner with the US Patent Office and a patent attorney for Philco-Ford, Elco Corp and Varian Associates, Pressman is currently in private practice specializing in patent law. He is also the author of *Patent It Yourself!—How to Protect, Patent and Market Your Inventions* and a lecturer in patent, trademark and copyright law at San Francisco Community College.

8086 Strike Force

Intel announces the M8086, the most powerful 16-bit military microprocessor available today.

Intel's new M8086 now gives designers the architectural base to launch an attack on previously inaccessible military applications. Offering up to an order of magnitude higher performance than previous devices, the M8086 is the most powerful 16-bit military microprocessor available today.

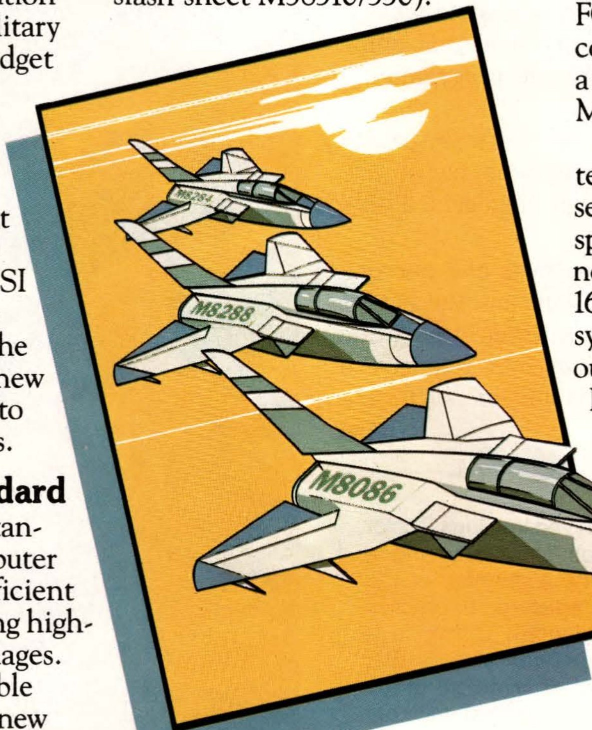
But just as importantly, Intel also offers the M8086-compatible support components and development tools you need to build complex VLSI systems for military applications. Components such as those shown in the table. Plus the industry's most complete array of hardware/software support tools. That's the *system* solution you need to deliver your military products—hitting time, budget and performance targets precisely. That's the 8086 Strike Force.

Proving once again that Intel puts military equipment manufacturers in command of the latest advances in VLSI technology. From our JAN-approved 8080A, through the M8085 and M8048, to the new M8086: Intel is committed to delivering military solutions.

The new military standard

The M8086 sets a new standard for military microcomputer applications. With super-efficient architecture for implementing high-level block-structured languages. A full megabyte of addressable memory space. A powerful new instruction set, including hardware Multiply and Divide. Plus flexible system configurability through the Multibus™ interface. All of which makes it possible to use the M8086 in applications that used to require multiple-chip CPUs, such as bit-slice designs and minicomputers. And because Intel designs M8086 systems for future expansion, you'll be able to take advantage of further enhancements—such as co-processors and IO processors—as military versions become available.

The HMOS*-process M8086 and support components are ready today to be drafted into your hi-rel military systems. All components conform to Class B standards of MIL-STD-883B, Method 5004, while meeting all military inspection criteria and lot conformance testing requirements of Method 5005. Futhermore, the M8086 family has been selected for military standardization under the MIL-M-38510 program (JAN slash sheet M38510/530).



The M8086 Family (Class B, MIL-STD-883B T_A: −55° to 125°C)	
Microprocessor/Support Components	
M8086	Microprocessor
M8282/3	Octal Latches
M8284	Clock Generator and Driver
M8286/7	Octal Transceivers
M8288	Bus Controller
Standard Memories	
M2114A	4K Static RAM (1K x 4)
M2148H	4K Static RAM (1K x 4
M2147H	4K Static RAM (4K x 1)
M2118	16K Dynamic RAM (16K x 1) T_A: −55° to 85°C
M2716	16K EPROM (2K x 8)
M2732	32K EPROM (4K x 8)
M3636	16K Bipolar PROM (2K x 8)
Peripherals	
M8251A	USART
M8253	Counter/Timer
M8255A	Programmable Peripheral Interface
M8259A	Interrupt Controller

Getting your products off the ground

You can begin designing your next generation of 16-bit military microcomputer systems today, using Intel's total hardware/software support tools. Hardware support such as the Intellec® Series III Microcomputer Development System, with ICE-86™ in-circuit emulation. And software tools like the RMX/86™ real-time multitasking executive, PASCAL-86, FORTRAN-86 and PL/M-86 compilers, ASM-86 assembler, and a full range of utility and M8080A/M8085A conversion software.

To stay at the forefront of VLSI technology, and capture larger segments of military business, specify the M8086 family for your next design. It's the only *complete* 16-bit military microcomputer system available today. To find out more about the M8086 and Intel's full line of military products, contact your local Intel sales office/distributor, and ask for our *Military Products Catalog*. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. (408) 987-8080.

*HMOS is a patented Intel process.

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January 7, 1981 issue of EDN

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ANALOG MULTIPLEXER
HI-516
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REF
D/A
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ANALOG TO DIGITAL CONVERTER
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Harris Technology at Work

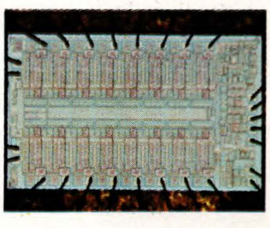
Harris mux technology delivers max system performance.

Industrial controls. Medical instrumentation. Telemetry. Data acquisition systems. Whatever the application, systems designers look to Harris Semiconductor for the industry's most advanced family of analog multiplexers. All feature Harris' unique Dielectric Isolation (DI) processing. And that means outstanding performance and reliability.

Ultra-High Speed. Looking for unprecedented speed? The HI-516 and HI-518 are prime examples. How about 600 ns settling to 0.01% accuracy! And these two speedsters can be configured under logic control for 16-channel or 8-channel differential (HI-516), or 8-channel or 4-channel (HI-518) operation, for maximum flexibility:

HI-516/518

- ☐ Single/Dual Operation — 16/8 Ch.
- ☐ Mode Programmable
- ☐ Fast Access Time — 100 ns
- ☐ Fast Settling Time — 600 ns (.01%)
- ☐ Low Leakage — 35 pA
- ☐ Low Charge Injection — 0.3 pC
- ☐ High Off Isolation — 80 dB



HI-524 — WORLD'S FIRST VIDEO MUX!

- ☐ 4 Video Channels
- ☐ High Input B.W. — 20 MHz
- ☐ Fast Access Time — 150 ns
- ☐ High Off Isolation — 72 dB (5 MHz)

Low Cost — Low Power. Popular Harris multiplexers like the HI-506/507 and HI-508/509 include 16-channel and 8-channel differential versions that are TTL, DTL and CMOS compatible:

HI-506/507/508/509

- ☐ 16 and 8-Channel Versions
- ☐ Access Time — 300 ns
- ☐ Off Isolation — 75 dB
- ☐ Low Power Dissipation — 4mW/Ch.
- ☐ Low Cost — 63 cents/channel (1K qty)

Input Protected — Low Power. Overvoltage protection? Take a look at the Harris HI-500A Series. These clever muxs withstand loss of power supply voltages and overvoltages up to 20 volts without faulting the output or any input channels. This feature gives you another competitive edge in system reliability:

HI-506A/507A/508A/509A

- ☐ 16 and 8-Channel Versions
- ☐ Access Time — 300 ns
- ☐ Analog Input O.V. Protected
- ☐ Low Power Dissipation — 0.5 mW/Ch.

Optimum Quality. Choose from five HI-500 Series quality grades to complement your application needs:

Commercial/Industrial (0°C to +70°C)
1. Standard, Dash 5 code
2. High-Reliability, Dash 7 code

Military (−55°C to +125°C)
3. Standard, Dash 2 code
4. MIL-STD-883B, Dash 8 code

High-Temperature (0°C to +200°C)
5. Standard, Dash 1 code

FREE WALL CHART! Harris multiplexers give you max performance. At competitive prices. And off-the-shelf delivery. For more examples of Harris technology at work, request your copy of the Harris Linear and Data Acquisiton Products wall chart.

Use the Harris Hot Line, or write to:
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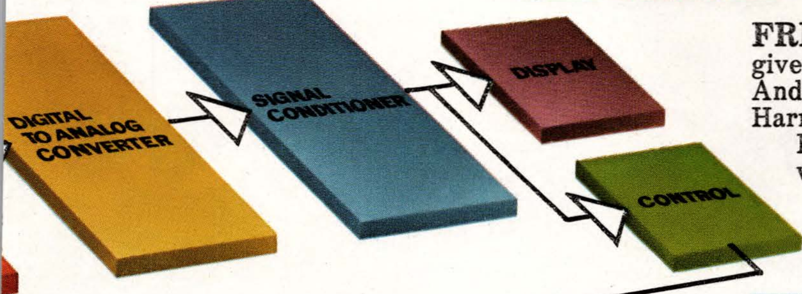

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HI-529 Low-Level Multiplexer

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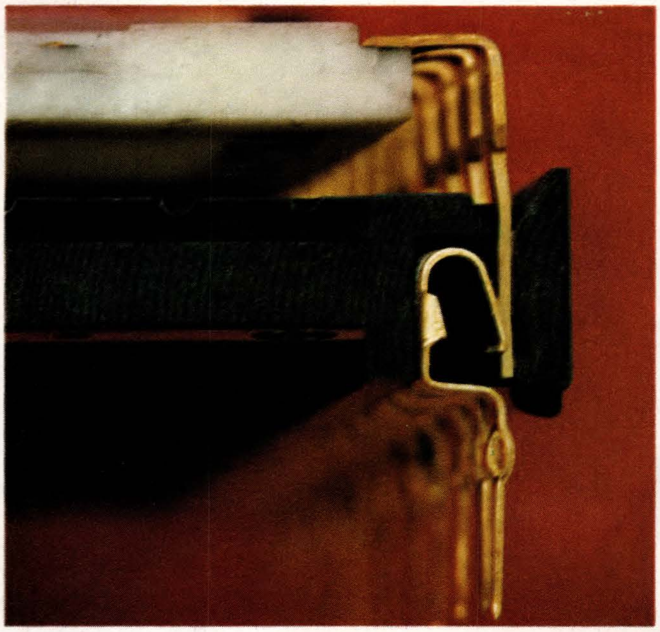
.to achieve GAS TIGHT RELIABILITY in a low profile socket



RN single leaf high compression contact provides maximum pressure against your IC lead.

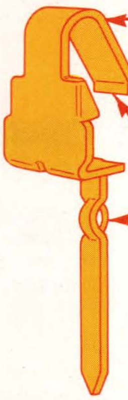
You know the secret of gas tight reliability in a low profile DIP socket. It is the "squeeze" or force the contact exerts on your IC lead. RN single leaf high compression contacts exert a "normal force"* that is 4 to 5 times greater than conventional dual leaf contacts. Result? RN low profile ICL series sockets are MIL-SPEC qualified (MIL-S-83734) to meet the toughest gas tight performance standards in the world.

You can't buy a more gas tight low profile socket—anywhere! And, our prices compare very favorably with any comparable socket.

*NORMAL FORCE means force at right angles to the IC lead.

MIL-S-83734 Environmental Test Data for ICL Series DIP Sockets

Test	Procedure	Results
Initial Contact Resistance	MIL-S-83734 Paragraph 4.7.15	R_C=7.0mΩ average
Corrosive Atmosphere	MIL-S-83734 Paragraph 4.7.16 10-25 ppm $(NH_4)_2S$, 4 hours	R_C=8.5mΩ average
Moisture Resistance	MIL-S-83734 Paragraph 4.7.14	$R_i \geq 10^{12}\Omega$
Thermal Shock	MIL-S-83734 Paragraph 4.7.13	No Damage
Mechanical Shock	MIL-S-83734 Paragraph 4.7.11	No Discontinuity
Vibration	MIL-S-83734 Paragraph 4.7.1	No Failures R_C=7.0mΩ average (final)
Socket Durability	MIL-S-83734 Paragraph 4.7.12 After 50 Cycles	R_C=7.8mΩ average



Contact available in phosphor bronze, beryllium copper, with tin or selective gold plating.

High compression contact design provides longer spring length for maximum pressure against IC lead.

"Side-wipe" design meets flat, smooth side of IC lead for perfect contact.

Self-lock lead holds socket firmly during wave soldering and prevents solder wicking.

Superior contact design

WRITE FOR COMPLETE DETAILS and latest RN catalog with full specs, dimensions and material data.

MAIL THIS COUPON NOW

Send me full details on your gas tight low profile ICL series sockets right away.

RN 800 E. Eighth St. New Albany, IN. 47150

Name ____________________ Title ____________________

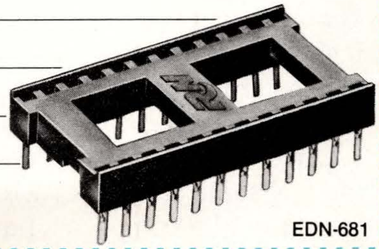
Company ____________________ Phone ____________________

Address ____________________

City ____________________ State __________ Zip __________

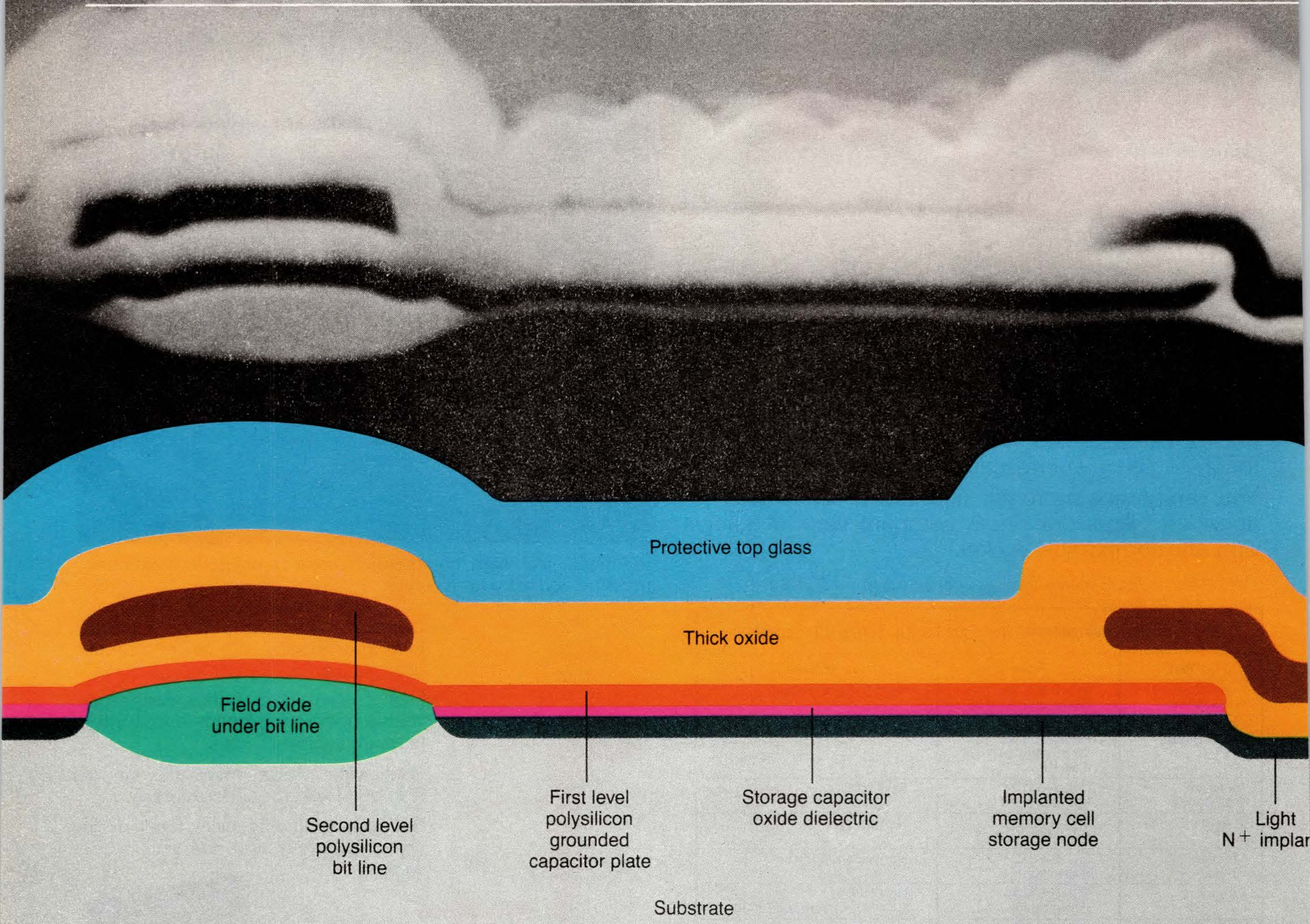
My possible application is ____________________

☐ Please send MIL-S-83734 Test Results



EDN-681

THE BUSINESS OF DESIGN



By now, you're probably aware that no less than 18 manufacturers have or will introduce their own version of a 64K RAM. And that each version will be at least a slightly different design. So how will you choose one intelligently? How will you base your decision knowing that each manufacturer feels strongly justified in choosing the architecture and manufacturing process it will use?

One of the best ways to evaluate any semiconductor memory is to look at a company's past experience in producing them. Look beyond the performance specifications and find out just how much they know about the business of design.

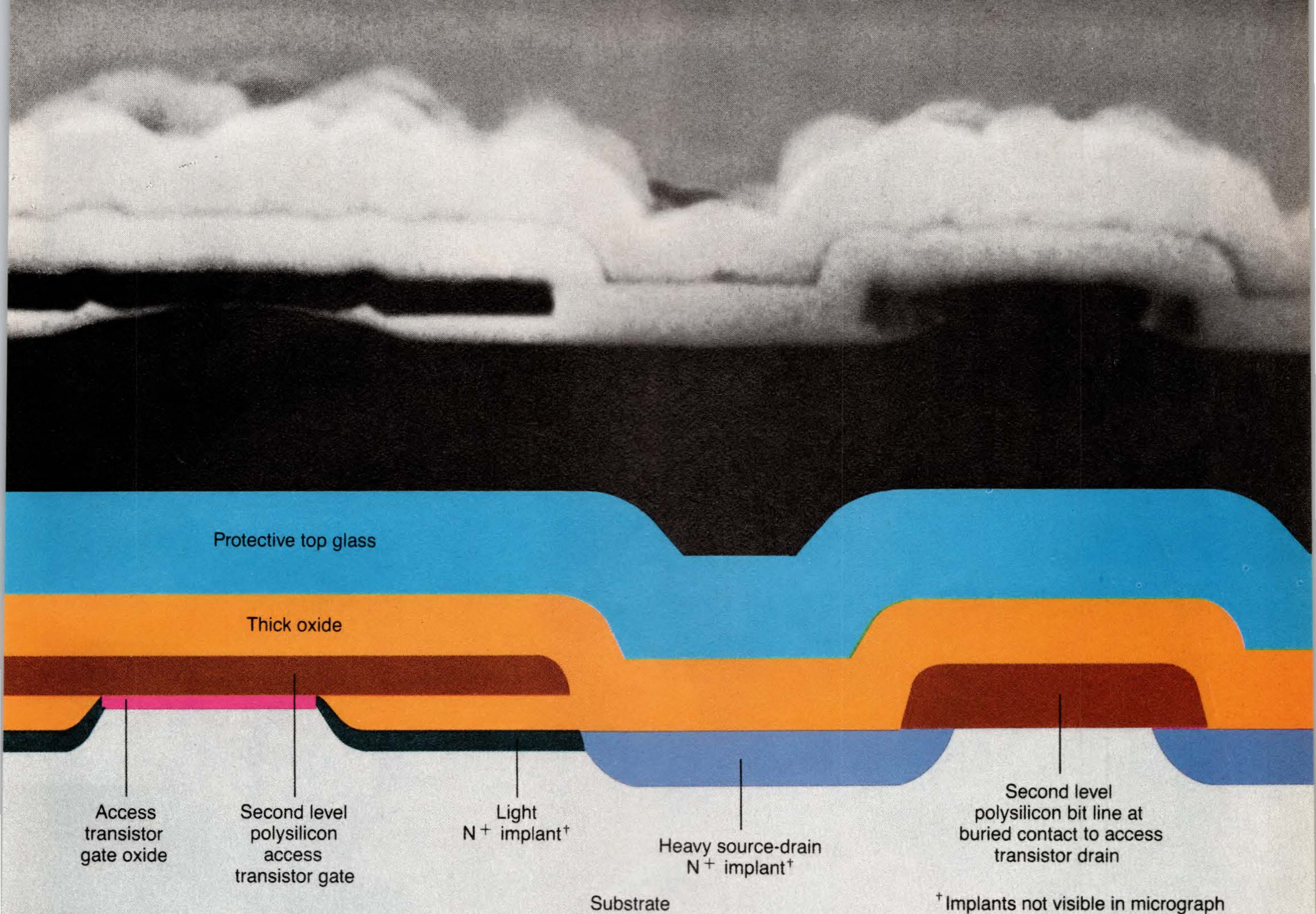
At Mostek, the business of design means that the ultimate challenge for our designers is to enhance the manufacturability of every device we make so that it can be produced reliably, in volume. It means that we incorporate and refine, wherever practical, the same proven design techniques that helped us achieve world dominance at the 4K level, and to an even greater extent, at the 16K level.

But it also means that we fully investigate and develop new approaches and new circuitry to satisfy the new constraints inherent in progressively sophisticated MOS memories.

A good example of this business-like approach to design is the use of polysilicon bit lines in our Scaled POLY 5* process.

How to choose a 64K RAM wisely after examining the specs.

MOSTEK.



Though diffused bit lines are undeniably correct for our industry-standard MK4116, VLSI geometries precluded their efficient use in the MK4164. Consequently, we needed a new way to maximize the usable signal generated from the smaller area available for storage cells. So we switched to polysilicon bit lines. This switch significantly improved the capacitor-to-total-cell area ratio and resulted in 50% more usable signal to the sense amplifiers than if we had used diffused bit lines with the same layout rules.

Though the switch to polysilicon bit lines is just one example of numerous MK4164 design innovations, it is representative of the driving force behind all of them: Improved manufacturability. Because for us, achieving higher levels of manufacturability is not only a noble design goal, it's also smart business. It's why we make and ship more dynamic RAMs to more companies than anyone else in the world. And it's how we intend to maintain that distinction.

To find out more about the added confidence that designed-in manufacturability can give you, send for our 64K RAM brochure that explains it in detail. Write Mostek, 1215 West Crosby Road, Carrollton, Texas 75006. (214) 323-6000. In Europe, contact Mostek Brussels, 660.69.24.

CIRCLE NO 180

The 10-Bit DAC Race Is Over!

PMI's High-Speed DAC-10 Just Became The Leader in Linear Wonderland

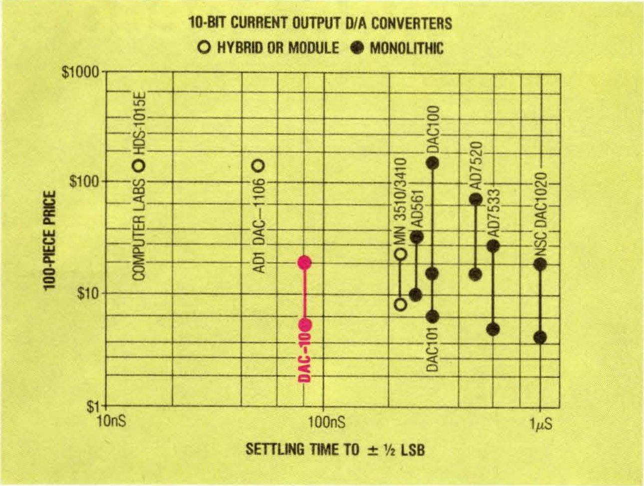
"Oh dear! Oh dear! I shall be too late!," the White Rabbit said as Alice saw him take a watch out of a waistcoat pocket, look at it and then hurry on. In Alice's Wonderland, the White Rabbit was always rushing off in new directions but arriving there too late.

In Linear Wonderland, a lot of circuit designers are like the White Rabbit. They constantly race the clock to complete development of new linear circuits, only to find that PMI's gotten there first.

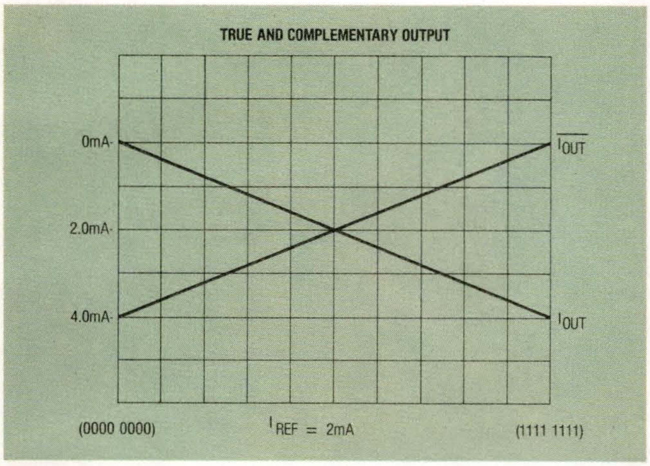
Our new DAC-10 is a case in point. Every linear house has been racing to come up with an affordable high-speed 10-bit D/A converter. Now PMI has one. With a speed of 85ns and a pinout compatible with our industry standard DAC-08, the low-priced DAC-10 will make further development of 10-bit current output DACs unnecessary. PMI is understandably proud of its accomplishment.

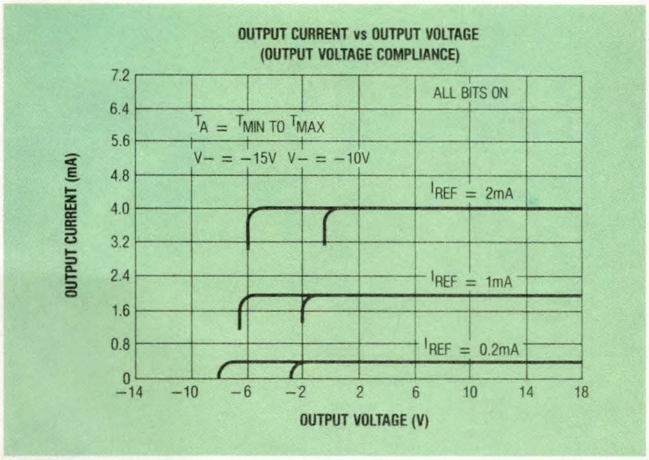
The DAC-10 is not just a modified DAC-08. It's a brand new product, redesigned to achieve the *speed* of the DAC-08 but with 10-bit resolution and ½ LSB full-scale accuracy. Trimming is achieved with zener zapping to avoid the long-term instability problems associated with laser trimming.

All that at attractive domestic prices starting at $5.50 for commercial grades and $14.50 for military grades. A comparison of the speed/resolution/price tradeoffs in existing 10-bit DACs will show you exactly why the PMI DAC-10 is destined to become the 10-bit industry standard, just like the DAC-08 became the 8-bit standard.



The White Rabbit looked at his watch again, then dipped it in his cup of tea to see if he liked what it said any better. If you're still not sure the DAC-10 looks good to you, PMI can give you some other ways of looking at its performance.





While the DAC-10 may have come along too soon for our competitors, we think equipment designers will say it's just in time. Think of the possible applications:

- 10-bit 2μsec A-to-D converter
- Tracking A-to-D converter
- CRT graphic display driver
- High-speed waveform generator
- Programmable current source
- Programmable attenuation/gain
- Voltage output with simple resistor termination

Whatever your application, send for our "Quick As A Rabbit" DAC-10 sample or give us a call.

And tell your engineering friends who design linear circuits they can stop work on their 10-bit DACs and get started on something else. When they get to where they're going, PMI will already be there . . . waiting for them to catch up.

If someone beat you to the coupon, write to us. Or circle **#251** for literature.

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Check the box for your
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☐ DAC-10 ☐ Literature

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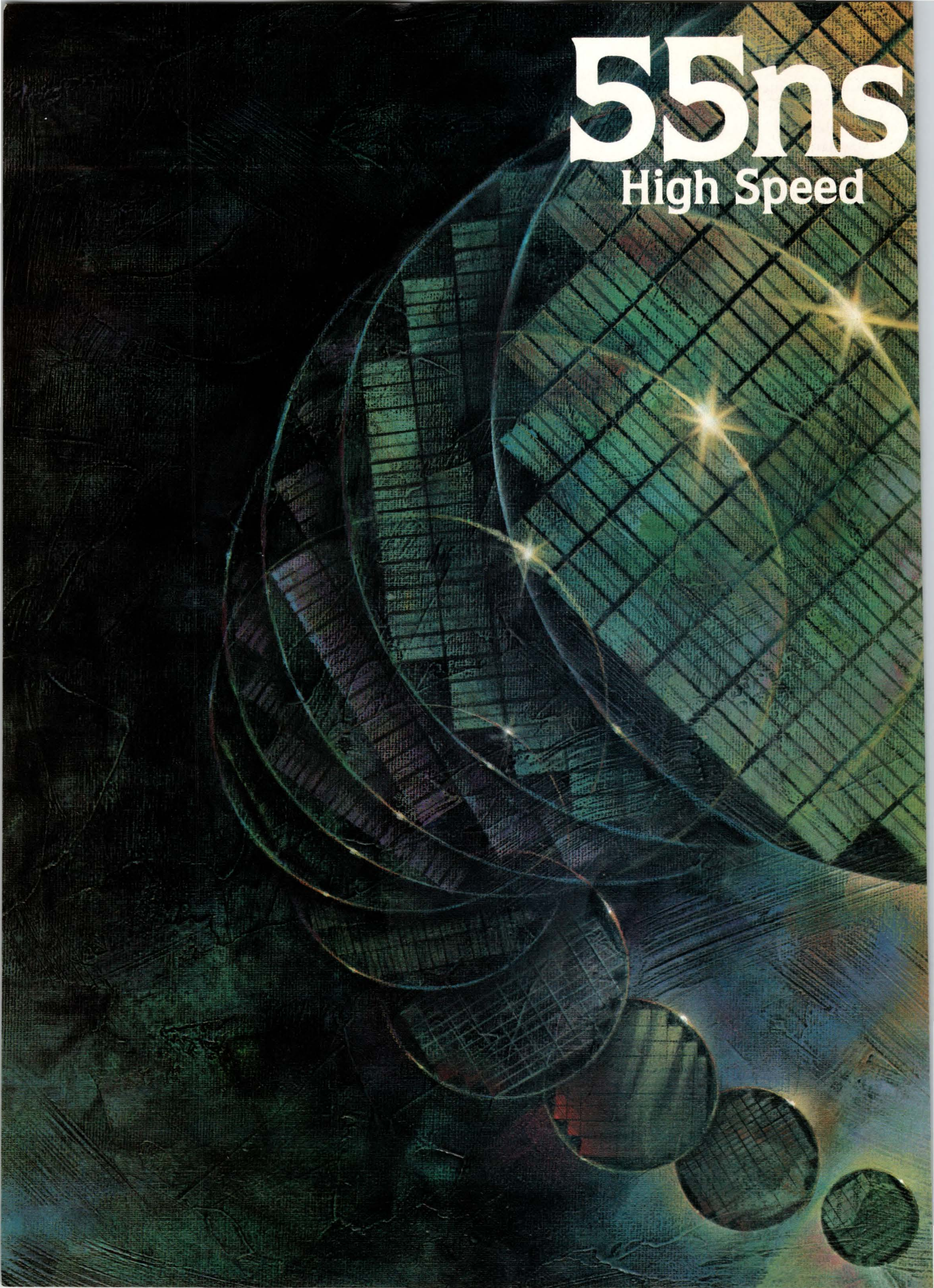
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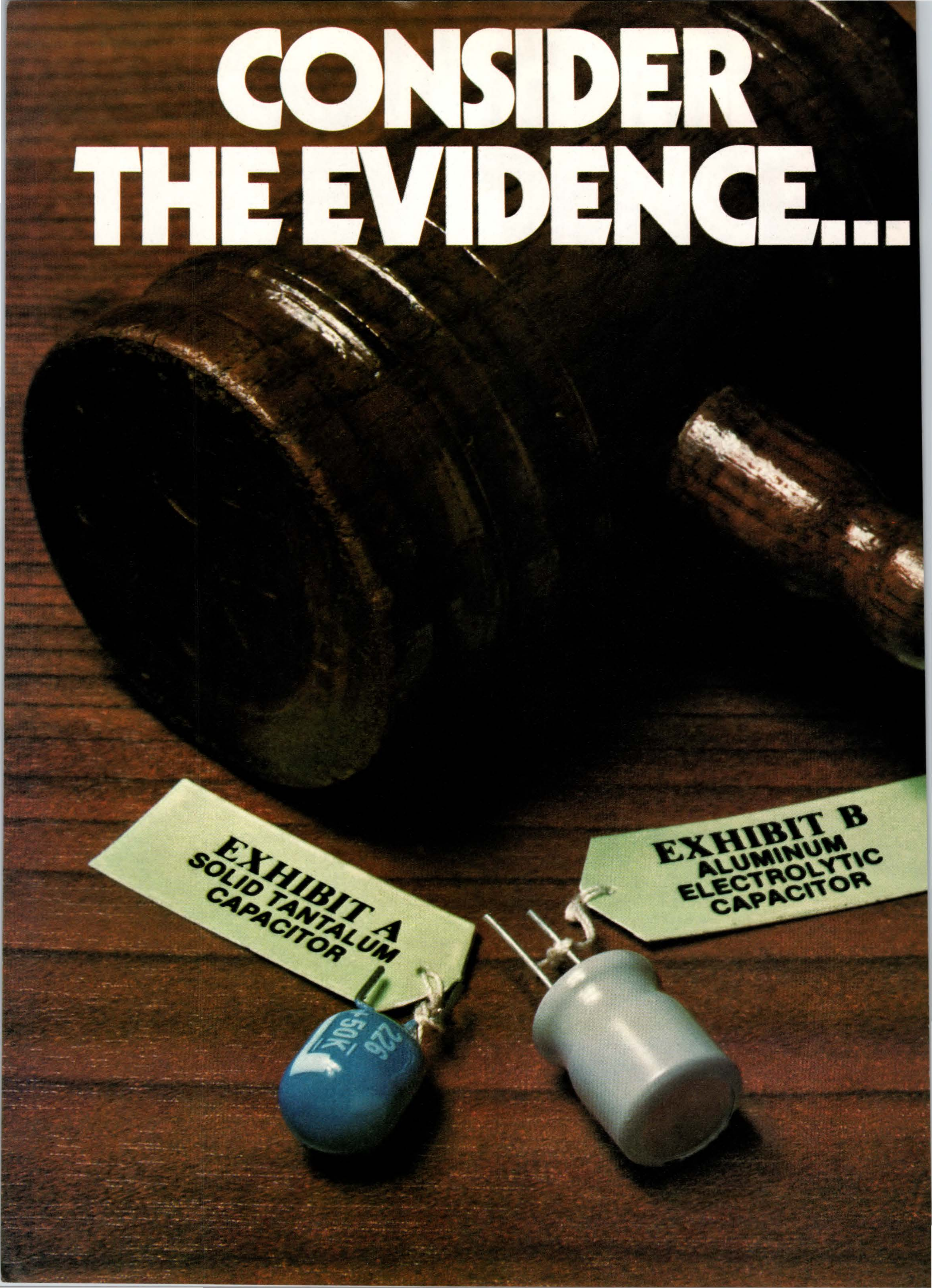
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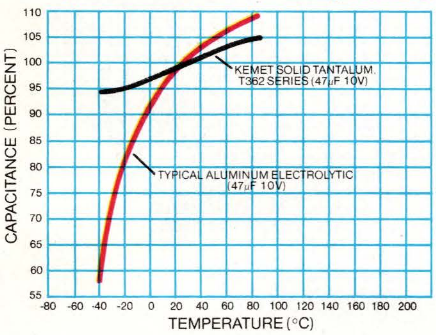
Will Aluminum Electrolytic Replace Solid Tantalum? You be the judge...

When you examine all the facts, it's an open-and-shut case in favor of KEMET® Solid Tantalum Capacitors: No "wear-out" mechanism. Better parametric performance over wide temperature ranges. Better long-term stability. Aluminum electrolytics just don't hold up under cross-examination. Here's the incriminating evidence:

Superior capacitance and dissipation factor stability with temperature.

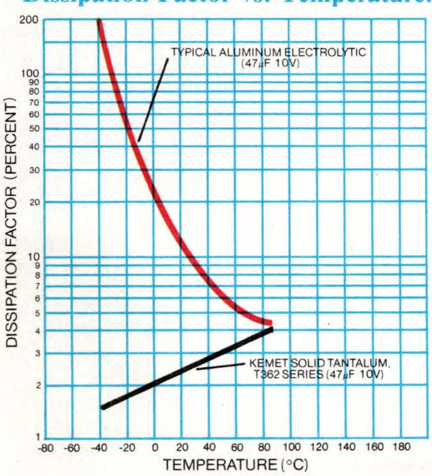
Unlike aluminum electrolytic capacitors which typically exhibit serious capacitance loss at low temperatures, KEMET Solid Tantalum Capacitors test unusually stable. In fact, this advantage may even allow you to lower the nominal design value of a solid tantalum capacitor.

Capacitance Shift vs. Temperature.



Dissipation factors of KEMET Solid Tantalum Capacitors are significantly lower and more stable than aluminum counterparts you may be using. For example, at −40°C, the aluminum electrolytic's 120 Hz DF is typically over one hundred times greater than a KEMET Tantalum.

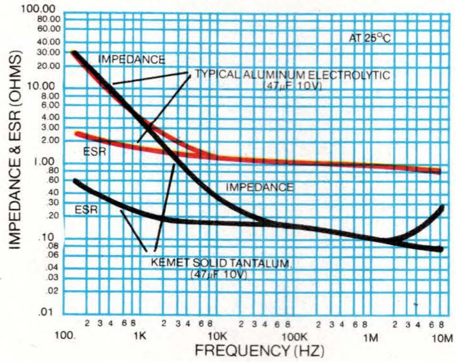
Dissipation Factor vs. Temperature.



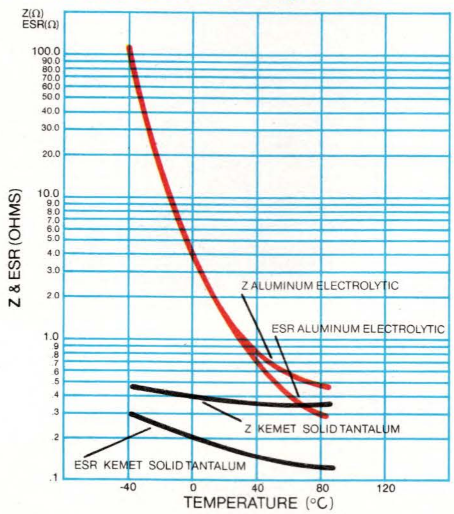
Superior impedance/ESR characteristics.

Tantalums offer superior Z/ESR characteristics over the broad range of frequencies and temperatures necessary for effective filtering in applications requiring low ESR, extended frequency response and wide-range temperature capabilities.

Impedance and ESR vs. Frequency.



Z and ESR vs. Temperature.

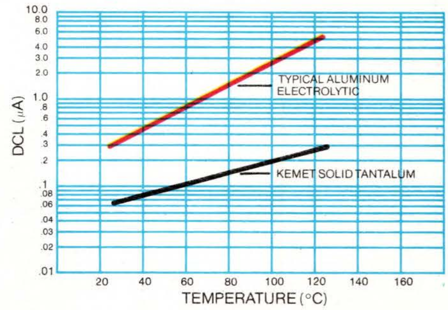


If you're working with power regulation or distribution systems, you've noticed that the unstable Z/ESR characteristics of typical aluminum electrolytics can contribute to ripple in power supply filters and cross coupling in decoupling applications. Such poor performance will also lower the "Q" of tuned circuits and alter the properties of pass band and band stop filters.

Superior D.C. leakage performance.

KEMET Tantalums offer significantly lower D.C. leakage than typical aluminum electrolytics — and maintain excellent leakage stability. You'll appreciate these characteristics especially in bypass/coupling, timing, and circuits requiring low energy drain.

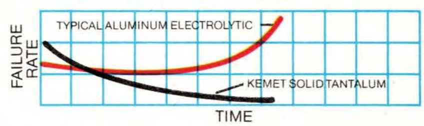
D.C. Leakage Characteristics vs. Temperature.



No wear-out mechanisms.

Aluminum electrolytics tend to degrade during shelf storage — and eventually "wear-out" due to liquid electrolyte loss when operated at elevated temperatures. Solid tantalum capacitors offer you indefinite shelf life and demonstrate a constantly decreasing failure rate during life tests.

Failure Rate vs. Time.



Resistance to solvents.

When present under operating conditions, halogenated hydrocarbon solvents and detergents attack the aluminum foil in aluminum electrolytics. Just a few parts per million of these solvents can cause complete failure of the aluminum electrolytic. KEMET Tantalums? No need to worry — they're not affected by such solvents typically used for flux removal.

The verdict is unanimous: KEMET offers you more.

When you examine the evidence, solid tantalums consistently prove their case against aluminum electrolytics. In reliability. Performance. Stability. That's why, for highest, long-term performance, you can't lose when you specify the quality leader — KEMET Solid Tantalum Capacitors.

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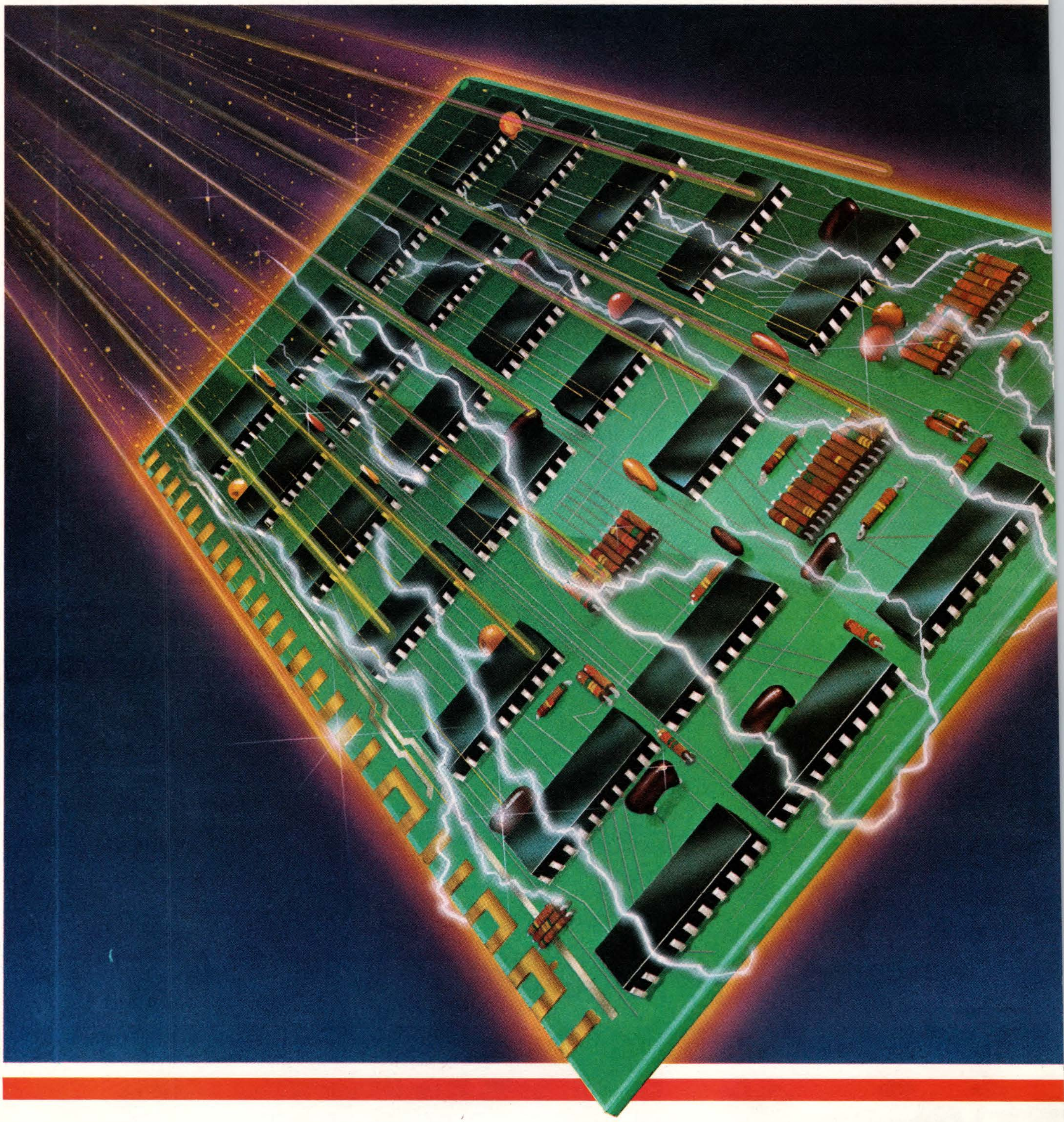
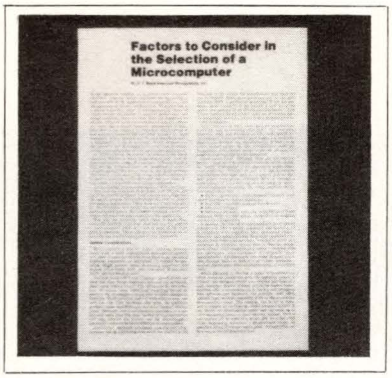
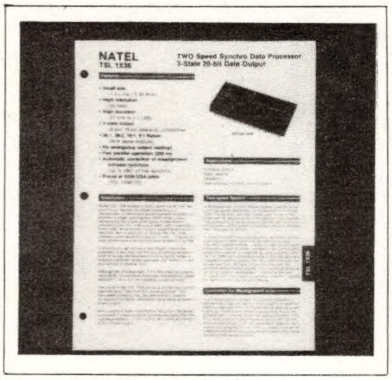


Literature



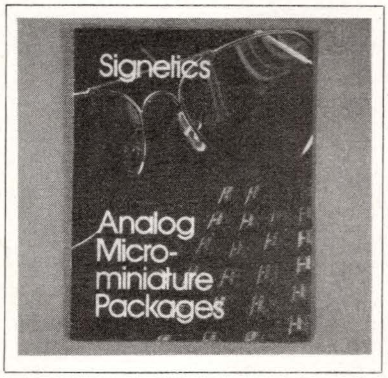
Tips for selecting μCs

"Factors to Consider in the Selection of a Microcomputer" examines how a μC can be used as a controller and to display information. It also discusses a machine's instruction set's suitability for various applications and the significance of second sourcing. It highlights the company's S2000 family, which features direct drive to LED or vacuum-fluorescent displays, keyboard inputs, ac-line synchronization and expandable ROM. **American Microsystems Inc,** 3800 Homestead Rd, Santa Clara, CA 95051. **Circle No 276**



Illustrated data on synchro processor

A 4-pg data sheet provides applications and interfacing information for a compact 2-speed synchro processor with 3-state output. The unit accepts two binary word inputs from a pair of synchro/resolver-to-digital converters and produces a 20-bit binary output representing coarse shaft angle. The data sheet discusses the unit's features, operational theory, specifications, pin designations and ordering information. **Natel Engineering Co Inc,** 8954 Mason Ave, Canoga Park, CA 91306. **Circle No 277**

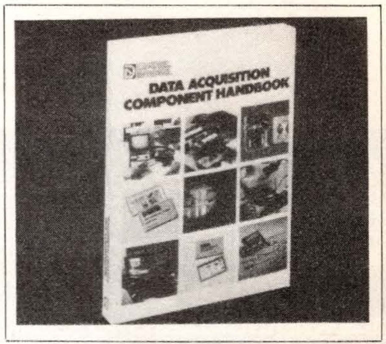


Features of small IC packages

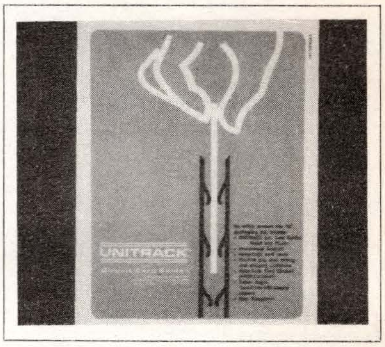
Detailing the evolution and application of the manufacturer's SO (small outline) microminiature package, a 12-pg brochure describes the analog-IC package, which can accept a standard die while reducing finished volume to <25% of that of a standard DIP. Sections cover mounting methods, power dissipation and cost effectiveness as well as 25 analog-IC products. Reliability-evaluation tables conclude the catalog. **Signetics,** Box 409, Sunnyvale, CA 94086. **Circle No 278**

Selecting various data-acquisition units

A 566-pg handbook provides data on monolithic, hybrid and modular products: A/D and D/A converters, data-acquisition systems, sample/holds, operational and instrumentation amplifiers, multiplexers, special-function devices and power supplies. It organizes products into selection tables, categorized by function



and performance. Data sheets for key products and ordering information are included. **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048. **Circle No 279**



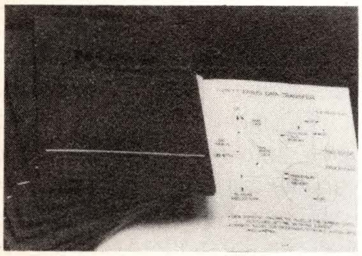
Data for your pc-card-packaging needs

A 24-pg catalog describes card guides, racks, brackets and ejectors for packaging pc cards. It details vibration- and shock-damping guides as well as metal guides for grounding and heat dissipation. Materials and test data are furnished. **Unitrack Div Calabro Industries Inc,** 8738 W Chester Pike, Upper Darby, PA 19082. **Circle No 280**

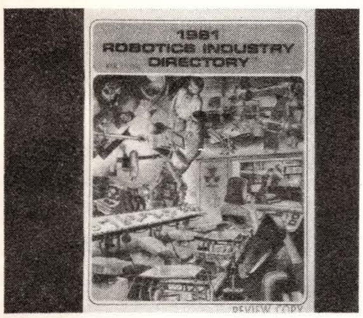
Review of distributed architecture

The F64 Series Technical Description details the manufacturer's distributed-intelligence concept, comparing it with conventional sequential and parallel computer architectures. The volume includes data on the company's Cyblok computing, mass-storage and I/O-

Literature

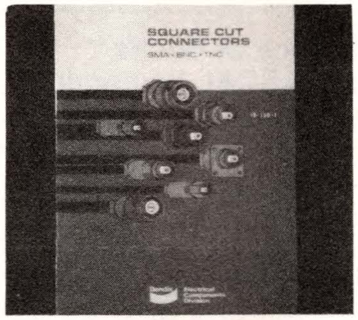


processing building-block modules for use in loosely coupled networks. Flowcharts, graphs and tables explain the switching element, bus structure (Fabus) and operating system (DUMBOS). Summaries of more than 16 modules and accessories are included. $14.95. **Gould Inc,** Functional Automation Div, 3 Graham Dr, Nashua, NH 03060. **INQUIRE DIRECT**



Tracking robotics products

The 70-pg "Robotics Industry Directory" describes robotics products and components and provides technical specs, pricing data and marketing contacts. It also furnishes data on firms offering related services, such as consultation, engineering design, systems integration and custom manufacturing. Its final section describes robotics-related activities of government organizations and university and private research laboratories. $24.95 (US); $26.45 (Canada); $31.45 (other countries). **Robotics Industry Directory,** Box 725, La Canada, CA 91011. **INQUIRE DIRECT**



Square-cut-connector characteristics

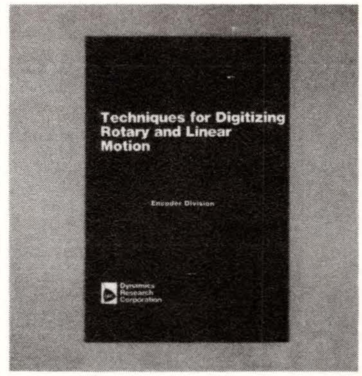
A 24-pg catalog describes Bendix square-cut connectors. It features SMA, BNC and TNC units, including military specs for electrical, mechanical and material features; technical drawings showing dimensions; and charts providing device part numbers by cable, grade and clamp type. Ordering and cable-jack-assembling instructions are also provided. **C Tennant Electronics,** 1051 Blake St, Edwardsville, KS 66113. **Circle No** 281

Computer-graphics terminology reviewed

A 40-pg pocket-sized booklet alphabetically lists computer-graphics terminology, from "absolute vector" to "zoom." It's designed for novice and experienced computer-graphics users. Request on company letterhead or submit a business card. **Megatek Corp,** 3931 Sorrento Valley Blvd, San Diego, CA 92121. **INQUIRE DIRECT**

Digitizing rotary and linear motion

A reference manual discusses rotary and linear-motion digitizing techniques and contrasts available transducers. Explaining encoder operation, it details the major steps of interfacing an encoder to specific types of systems. With eight tables and 68 illustrations, the 150-pg guide



discusses optical incremental encoders, encoder-interface considerations and typical unit applications. **Dynamics Research Corp,** 80 Concord St, Wilmington, MA 01887.
Circle No 282

Devices for precise pressure measurements

A 2-pg product guide compares four solid-state-pressure-transducer families. It examines pressure ranges, device types (absolute, differential and gauge), electrical excitation, full-scale output, amplified output, null and FSO trim and temperature-compensation specs for the piezoresistive devices. **Micro Switch,** 11 W Spring St, Freeport, IL 61032.
Circle No 283

Theory and uses of thermometry

Teaching both the theory and application of precision thermistors, Course No 17525 covers manufacturing processes, thermistor usage and interfacing in electronic circuits. A YSI Thermilinear component and YSI precision thermistor accompany the 20-pg course manual to facilitate designing temperature-circuit configurations. An exam is also provided. $25. **Yellow Springs Instrument Co Inc,** Yellow Springs, OH 45387. **INQUIRE DIRECT**

Literature

For your μC-software needs

Highlighting systems software for LSI-11/2 and -11/23 μCs, an 8-pg brochure describes the RT-11 development operating system and its execute-only subset, RT². It outlines RT² features: memory requirements, modularity, device independence and extendability. RT-11 high-level-language support and program-development utilities are also described, as are support services. **Digital Equipment Corp,** 444 Whitney St, Northboro, MA 01532.

Circle No 288

Aid in tracking down software

A 3-volume directory lists more than 400 Apple-software vendors, categorized by product application. Vol 1 tracks a wide variety of software for business applications, including investment and personal-finance packages, word-processing and graphics programs as well as database systems. Vol 2 organizes recreational-program vendors, encompassing those offering a variety of games, while Vol 3 lists educational software for administrative and teaching applications. $5.95 per volume. **WIDL Video,** 5245 W Diversey Ave, Chicago, IL 60639.

INQUIRE DIRECT

Books

A brace of books for PASCAL beginners

Introduction to PASCAL, *by Rodnay Zaks. xvii+421 pgs; $14.95; Sybex, Berkeley, CA, 1980.*

The PASCAL Handbook, *by Jacques Tiberghien. xix+473 pgs; $14.95; Sybex, Berkeley, CA, 1981.*

If you're familiar with structured programming, PASCAL holds no real surprises for you. The transition to PASCAL programming from BASIC, however, especially from working with a BASIC interpreter, might prove difficult.

Leaping into the information void with how-to-program-in-PASCAL books intended to smooth this transition, Sybex first introduced Rodnay Zaks's *Introduction to PASCAL.* Written for the reader who hasn't much programming experience, it gives a hand up to those who need one.

The difficulty with writing a book that simplifies, though, is that it becomes tempting to either oversimplify or ignore concepts that are a bit tricky to explain fully. Zaks seem to have avoided this temptation. He does, however, forget to explain some simple concepts (such as lexicographic ordering) that are used in the book. No large matter, though—you can figure out the simple concepts on your own. But it proves occasionally annoying.

The PASCAL Handbook does not tell you anything about programming in PASCAL; it's a reference book. It does provide a compendium for each PASCAL symbol, identifier and concept, including a list of the implementations that support each item. The book follows a well-ordered layout that makes for easy use.

Although you might be tempted to think of these two books as two volumes of one work, their styles, information content and even the authors' intentions are dissimilar. Whether or not you need the introductory work to start your programming, if you haven't already gathered all of the information in the handbook on your own, it's one book you'll want to keep on your shelf.—***Ed Teja***

Design and debug 6809 programs

6809 Assembly Language Programming, *by Lance Leventhal. Osborne/McGraw - Hill Inc, Berkeley, CA, 1981.*

This volume extends the set of Osborne/McGraw-Hill "how-to-program" books' coverage to the Motorola 6809. As one of the most powerful 8-bit μPs, the 6809 is enjoying increasing popularity. And its use by Radio Shack in the TRS-80 Color Computer ensures that many inexperienced assembly-language programmers will be needing information on how to work with it. Author Leventhal writes with an approach and scope suitable for these first timers.

The book begins, as do most similar volumes, with a discussion of binary and hexadecimal numbers and ASCII. It also includes sections on machine coding, assemblers and loaders and nicely covers the tradeoffs involved in using assembly or high-level languages. A general discussion of assemblers and their features begins the book's detailed technical part.

The 6809 derives much of its power from its addressing features, so this book begins

Books

describing the μP with a thorough coverage of its addressing modes. The discussion then leads naturally into a summary of the μP's register model and its instruction set.

Because the 6809 represents an evolutionary step from the 6800, the book spells out the differences and similarities between the two devices. And using the tables the author presents, you can readily convert 6800 code to run on the 6809.

The next major section presents a set of example programs. Most of them are very simple, intended more as illustrations than as useful routines. A careful reading, though, provides a good review of the 6809's instruction set, addressing features and other capabilities. A separate chapter in this section covers the 6820 PIA and 6850 ACIA—the most common peripheral components used in 6800/09 systems. The section's final chapter covers interrupts, an area that can cause much confusion for beginners.

A lot of "how-to-program" books would stop here, but nearly half of *6809 Assembly Language Programming* deals with program design and debugging. It leads you through several small design projects and includes a chapter on documentation. Additionally, the discussion of how to properly comment an assembly program as well as the debugging chapter should be required reading for all beginners.

In the latter, Leventhal leads you through several programs that might appear correct but actually have bugs in them. You're practically forced to find the bugs yourself, using the section's step-by-step approach.

A chapter on how to test programs completes this very useful topic, which is so often neglected in "how-to-program" books.

In summary, the book delivers exactly what its title implies—a thorough tutorial on how to write assembly-language programs for the 6809 μP. It's slanted toward beginners, but the reference lists at the end of each chapter could prove a valuable resource for further and more advanced study.

This book continues the Osborne/McGraw-Hill scheme of using boldface type to highlight key points; reading only the boldface passages gives an excellent overview of the material. And the summary appendices furnish about as complete a review of the 6809 instruction set as could be presented. Beginning 6809 programmers need look no further than this volume.—***Robert D Grappel*** *(Hemenway Associates Inc)*

NEXT TIME

EDN's July 22 issue is our 13th semiannual Product Showcase, an invaluable compendium of information on the most noteworthy new-product introductions of the past 6 months. You won't want to be without this fact-filled reference issue, which is organized into six key product areas:

- Components
- Computers and peripherals
- Hardware and interconnect devices
- ICs and semiconductors
- Instruments
- Power sources

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San Jose, CA 95128
(408) 243-8838

EDN

CAREER OPPORTUNITIES
RECRUITMENT ADVERTISING

for space reservation contact:

Sheila Schaeffer,
Eastern Regional Mgr.
617-536-7780

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Western Regional Mgr.
408-243-8838

DESIGN ENGINEERS...

Welcome home to Grass Valley

If you could choose the perfect spot to work and live, the Sierra foothills might well be your first choice.

Grass Valley California offers the ideal combination of a soft, four-season climate, easy access to major cities such as Sacramento, Reno and Lake Tahoe, an unspoiled, uncrowded Western life style and modestly priced homes on large, wooded sites.

This is the setting for our new, fully equipped IC Design Center, where a select number of top-notch engineers are at work designing SSi's next generation of custom integrated circuits.

SSi was recently named as one of the 100 fastest growing small companies in the U.S., and we don't plan to slow down. So if you are a degreed (BSEE) Design Engineer with 3 or more years of experience, with some experience in Bipolar and MOS IC design, welcome home.

For prompt consideration and acknowledgment of your interest, mail your resume to John C. Cornelius, Professional Staffing, 14351 Myford Road, Tustin, CA 92680.

SSi Silicon Systems incorporated

Tustin, CA **Grass Valley, CA**

An equal opportunity employer

Circle No. 5000 (on page 320 of **EDN**)

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Circle No. 5001 (on page 320 of **EDN**)

Career Opportunities

EDN

RECRUITMENT ADVERTISING

Recruitment Reader Service Response

If you are interested in receiving futher information on any recruitment ad running in **Career Opportunities,** we will happily provide this free service to you. Here's how to use it:

1. Circle the number in the box at the right that corresponds with the number at the bottom of the ad that interests you.
2. Fill out the information form and mail to:

EDN
Sheila Schaeffer
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Boston, MA 02116

5000	5001	5002	5003	5004
5005	5006	5007	5008	5009
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5015	5016	5017	5018	5019
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Your response will be held in strictest confidence

6/24

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Advertisers Index

Looking Ahead: Trends and Forecasts

Mini/micro peripherals to increase system share

The market for minicomputers and μC systems will skyrocket from an estimated $6.1 billion last year to $50 billion by 1990. And the percentage of this computer-market segment's revenues going to peripheral devices and integral peripheral components used directly in configuring mini/micro systems will increase from 55 to approximately 60% of total system value. This share translates into a $30 billion mini/micro peripheral market by 1990, according to International Resource Development Inc.

PROJECTED MINI/MICRO PERIPHERAL MARKET
(US SHIPMENTS, $ MILLION)

	1980	1982	1985	1990
DATA-ENTRY EQUIPMENT	240	370	915	1730
PRINTERS	560	780	1010	1185
MEMORY	300	750	1150	1650
DISK/TAPE	1000	1850	2565	2670
GENERAL-PURPOSE TERMINALS	650	1100	1650	3450
DATACOMM EQUIPMENT	370	665	925	1915
SUBTOTAL	3120	5515	8215	12,600
INTEGRAL PERIPHERALS	240	260	2115	17,400
TOTAL	3360	5775	10,330	30,000

SOURCE: INTERNATIONAL RESOURCE DEVELOPMENT INC

Between 1980 and 1990, some $140 billion worth of mini/micro peripherals will be shipped. As the decade progresses, more and more peripheral devices will lose their current identity (shape and size), and certain categories will become integral peripherals contained within multifunction devices.

Report #164 from IRD ($985) contains more information on this market. You can obtain it by contacting the firm at 30 High St, Norwalk, CT; phone (203) 866-6914.

Factory automation to boom

The synergism of several major factors has set the stage for striking growth in the US factory-automation industry, which will achieve sales of $2.3 billion by 1985, according to Creative Strategies International (CSI), San Jose, CA.

Factory automation is a dire necessity for some market segments—particularly the automotive industry. In the face of rising inventories, reduced output plans and this winter's automobile cash-rebate programs, it might be a key tool in the US's race to remain competitive with foreign auto imports.

The machine-tools factory-automation segment is also poised for a boom period, with growth spurred by the consensus that the US must increase productivity—a goal that can only be realized by replacing or updating manufacturing equipment currently in use. In addition to supplying products for the robust factory-automation-product market, the machine-tools industry possesses a healthy backlog of orders from such large clients as the automotive and aerospace industries.

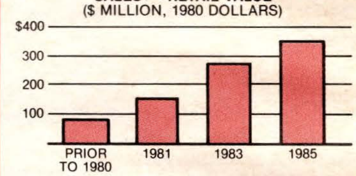
Although CSI attributes the factory-automation industry's 13% compound annual growth to these dominant industries' strength, the outlook isn't uniform for all market components. The most dramatic increases will appear in the markets for miscellaneous industrial equipment and miscellaneous nonelectric machinery, where growth will largely result from the increase of programmable-controller applications, predicts CSI.

The simultaneous coming of age of both the programmable-controller and industrial-robot industries will also have a powerful impact on the automation market. The programmable-controller segment will exhibit a 35% compound annual growth rate during the forecast period. And the late-blooming industrial-robot industry's recent focus on the cost justification of implementing robots in factories will pay off even more handsomely, at a 35% compound annual growth rate for heavy-duty robots and a 70% rate for light-duty industrial robots between now and 1985.

Microcomputers excel in education

Microcomputers are branching out of the hobbyist and small-business environment and moving into academia. Of the 50 companies that market microcomputers in the US, 13 account for 98% of an educational market that last year amounted to $102.1 million in retail value of units shipped, according to Creative Strategies International (San Jose, CA).

US EDUCATIONAL MICROCOMPUTER MARKET SALES — RETAIL VALUE
($ MILLION, 1980 DOLLARS)

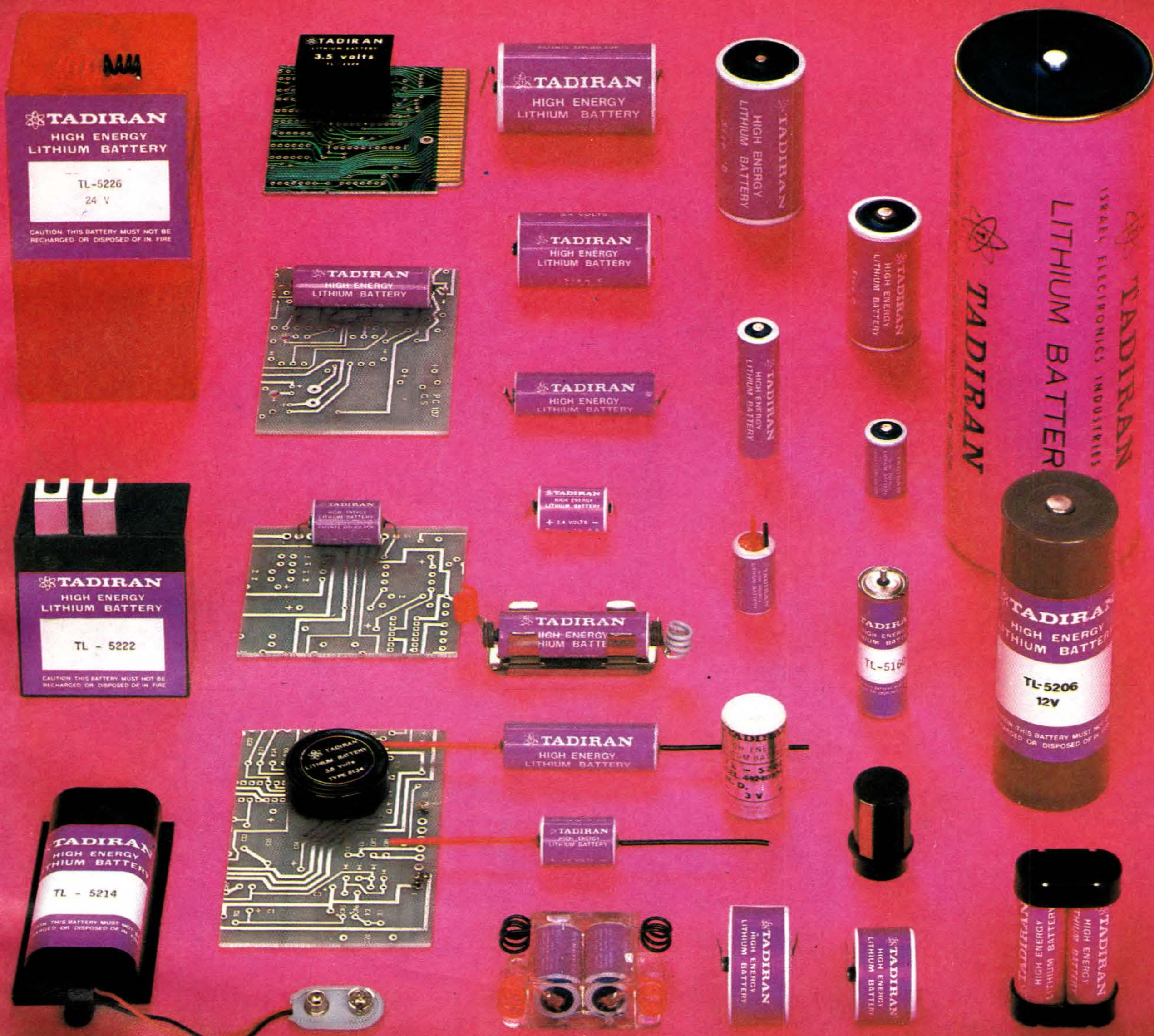


SOURCE: CREATIVE STRATEGIES INTERNATIONAL

Radio Shack, Apple Computer Inc and Commodore Business Machines, in that order, are the three leading suppliers; together they control 85% of the education business for microcomputers, which CSI expects to grow 28% compounded annually to $350.2 million in 1985.

Material for this page developed from *Electronic Business* magazine and other sources by Joan Morrow, Assistant Editor, and Jesse Victor, Assistant/New Products Editor.

Sentence your CMOS-based equipment to a lifetime of hard labor - with a TADIRAN™ lithium inorganic battery.



The Tadiran Lithium Inorganic Battery, with a shelf-life of more than ten years and a very flat discharge curve, can be mounted on a printed circuit board and forgotten. It is the ideal power source for CMOS circuits for applications in advanced telephony equipment, industrial controls, data processing, sensing and monitoring devices, microwave transmission equipment, and portable instrumentation.

Australia: Technico Electronics Ltd., Sydney, Tel. 02-427-3444; **Austria:** Sonnenschein GmbH, Linz, Tel. 0732-55529; **Belgium:** S.E.B. Souriau, Bruxelles, Tel. 02-2423370; **Canada:** CPU Electronic Components Ltd., Point Claire, Quebec, Tel. 514-697-8286; **Denmark:** Erik Westerberg A/S, Herlev, Tel. 02-929-000; **France:** Diode, Fresnes, Tel. 02-666-9801; **Germany:** Accumlatorenfabrik Sonnenschein GmbH, Buedingen, Hessen, Tel. 06042-91; **Italy:** Compelet, Milano, Tel. 02-688-8196; **Japan:** Union Engineering Ltd., Kobe, Tel. 078-331-2270; **Netherlands:** Sonnenschein (Netherland) B.V., Arnhem, Tel. 085-455041; **Norway:** Ingenior Harald Benestad AS, Oslo, Tel. 02-555-190; **Spain:** Diode, Madrid, Tel. 01-455-0139, 01-455-3686; **Sweden:** Mittor AB, Solna, Tel. 03-823-210; **Switzerland:** Metronic AG, Zurich, Tel. 01-418484; **United Kingdom:** Suvicom Ltd., Shirley, Solihull, West Midlands, Tel. 021-745-3251; **USA (East & Midwest):** Plainview Electronics, Plainview, N.Y., Tel. 516-249-6677; **USA (West, Alaska & Hawaii):** Carefree Unlimited, Placentia, Ca., Tel. 213-323-0603, 714-996-9400

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HOW TO IMPROVE THROUGHPUT IN PRODUCTION PROM PROGRAMMING.

Select a PROM programming system designed specifically for production. The new Data I/O production PROM programming system combines a Data Control Unit (DCU) for storing all your production programming data and a production programmer that's easy on the operator.

For high-volume programming, a new Handler UniPak interfaces to an IC handler without any extra software or hardware.

Take advantage of complete programming flexibility. Data I/O's new system adapts to any type of production PROM programming station: MOS or bipolar; moderate or high-volume. Whether you're gang programming, programming small lots with frequent data changes or programming large lots with few data changes, Data I/O's system can help you increase throughput, reduce errors and control data.

What's more, you can buy just what you need, and add to the equipment you already have.

Reduce errors with automated inventory control. Our Data Control Unit replaces master PROMs and paper tapes. You eliminate human errors caused by mistakes in loading data or updating PROM documentation.

The DCU can store enough data on a single diskette to replace 41 master PROMs (2716 type) or 2,000 feet of paper tape. Programs can be assembled in engineering, downloaded from an MDS or computer via RS-232C to a diskette, then sent to manufacturing for controlled production.

Make programming easy. All operator instructions are given in plain English on a 16 character display.

For high-volume throughput with a handler, the operator simply keys in the pattern part number and required quantity for a given job, loads the blank devices and begins the program sequence.

For moderate-volume programming, the operator sets up the machine and each device is programmed with a single keystroke or tap of a foot switch.

Demand programming accuracy. The Data I/O system stops mistakes before they happen—before they cost you time and money.

Every data transfer and command between the Data Control Unit and programmer is double checked. Each device is checked for illegal or unexpected bits before programming and for stuck bits after.

Programming is automatically verified. With the Handler UniPak, continuity testing is done on each device before programming to insure proper contact between socket and PROM.

Buy from a manufacturer who will support your system. Data I/O's production PROM programming system is backed by Data I/O's worldwide network of service technicians and field application engineers.

Data I/O has a solid commitment to keep customers informed about new device technology and programming techniques. If you would like more details about our new production PROM programming system, circle reader service number or contact Data I/O, P.O. Box 308, Issaquah, Washington 98027. Phone TOLL FREE 1-800-426-9016.

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CIRCLE NO 188